Environmentally Stable Transparent Organic/Oxide Hybrid Transistor Based on an Oxide Semiconductor and a Polyimide Gate Insulator

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***Abstract*—We fabricated environmentally stable and transparent organic/oxide hybrid transistor on a glass substrate using the conventional photolithography. The obtained device, which was composed of an In-Ga-Zn-O active layer/soluble polyimide (KSPI) organic insulator, showed a mobility of 6.65 cm^2/Vs, a subthreshold swing slope of 350 mV/decade, a threshold voltage (V_T) of 3.10 V, and an on–off ratio of 3.9×10^9. The transistor also showed good uniformity characteristics and was found to be environmentally stable for 90 days under ambient conditions.**

***Index Terms*—Oxide, sputtering, thin-film transistor (TFT), transparent.**

I. Introduction

FLEXIBLE displays have attracted great attentions because of their rugged and lightweight design and rollable properties [1]. There are many candidates for use as back-plane devices of active matrix flexible displays including a-Si:H, poly-Si, organic thin-film transistors (OTFTs), and oxide TFTs which could be compatible with low-temperature processes. Normally, Si-based TFTs fabricated at low temperature have inferior electrical characteristics compared to the corresponding devices fabricated at high temperature. In addition, Si-based TFTs are expensive to fabricate. Although OTFTs have received much attention largely due to their low-temperature and low-cost fabrication process, they have several critical shortcomings including environmentally unstable characteristics, low mobility, and low on–off ratio. The properties of OTFTs are highly dependent on the characteristics of the organic semiconductors, which are highly sensitive to the oxygen species present in ambient air [2], [3]. However, polymer dielectric materials still have several merits, e.g., they not only exhibit the good insulating properties through the low-temperature process (under 200 °C), but they can also lead to a reduction in costs and processing time. Since the oxide TFTs were reported by Nomura *et al.* in 2003, transparent oxide semiconductors such as ZnO, In-Ga-Zn-O (IGZO), and Zn-Sn-O (ZTO) have also attracted great attention because of their high mobility, good uniformity, and low-temperature process [4]–[6]. These oxide TFTs can meet the requirements for flexible devices, so that the hybridization of organic insulators and oxide semiconductors is very promising for the fabrication of flexible devices with good electrical performance and environmental stability and with a low cost [7], [8]. Although several organic/oxide hybrid transistors have been reported, most of them were fabricated by using a shadow-mask process or by employing very thick inorganic insulators. The resulting hybrid transistors are not only unsuitable for the fabrication of integrated flexible devices with high performance, but there are also no extensive reports regarding their environmental stability and uniformity characteristics [8], [9].

In the present study, we used a photolithography process, with a focus on the chemical resistivity of the organic layer and the use of a very thin oxide protection layer (PL) to fabricate high-performance and transparent organic/oxide transistors on a glass substrate.

II. Experimental

We fabricated transparent hybrid transistors with a staggered structure on glass substrates using sputtered IGZO and soluble polyimide (KSPI), as shown in Fig. 1. An In-Sn-O (ITO) source/drain electrode with a thickness of 150 nm was deposited using radio frequency (RF) magnetron sputter and patterned by means of the wet-etching process. An IGZO target with an atomic ratio of 2:1:2 was supported by Advanced Nano Products [10]. An IGZO active layer with a thickness of 20 nm was deposited at room temperature (RT) using an RF magnetron sputter, and a 9-nm-thick Al_2O_3 PL was grown

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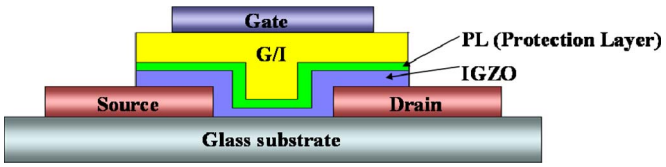

Fig. 1. Side view of a fabricated device with a staggered structure.

by means of atomic layer deposition (ALD) at 200 °C using trimethylaluminum as the Al precursor and H_2O as the oxygen precursor. Then, the PL and the active layer were simultaneously patterned by using the wet-etching process. We have already reported the effect of the PL on the oxide transistors: this layer protects the oxide active layer from solvent and air [11]. A low-temperature processable polyimide (KSPI) was used as the gate insulator (GI) layer. The fully soluble polyimide of KSPI just needs thermal annealing at 160 °C during the film fabrication process, while the polyamic-acid-based PI films generally require high process temperature for imidization [12]. It is a highly desirable characteristic for the fabrication of TFTs on flexible substrates. A KSPI layer with a thickness of 300 nm was spin coated and annealed at 160 °C, thus leading to a transmittance of 91.7% at 550 nm under air reference (data not shown). A metal contact hole was formed by dry etching using the oxygen plasma. Finally, an ITO gate electrode with a thickness of 150 nm was deposited using an RF magnetron sputter and patterned by means of a conventional wet-etching process. Particularly, the permeability of the organic insulator is an important factor for the fabrication of patternable devices. The KSPI showed adequate permeability characteristics during the patterning process, and these are also related to the environmental stability characteristics. All measurements were carried out in a dark box at RT to avoid the effects of light. The double-sweep mode (forward and reverse) was also used to observe the hysteresis characteristics.

III. Results and Discussion

We measured the C–V characteristics of metal-insulator-metal structures at 10 kHz to calculate the dielectric constant of KSPI. A 300-nm-thick KSPI layer showed a dielectric constant of 3.56 and a capacitance of 10.5 nF/cm^2. This value was also used to calculate the saturation mobility and the threshold voltage (V_T) of the units. Fig. 2(a) shows plots of the log I_d (drain current) versus V_G (gate voltage) for the as-fabricated devices. The units exhibiting a width of 320 μm and a length of 20 μm showed a saturation mobility of 6.70 cm^2/Vs, a V_T of -0.97 V, a turn-on voltage $(V_{\rm on})$ of -7.5 V, a subthreshold swing (SS) slope of 460 mV/decade, and an $I_{\rm on}-I_{\rm off}$ ratio of 2.2×10^8. Although the devices show a high mobility and a high on–off ratio, they still have some problems such as a gate leakage current in the range of several picoamperes level, a negatively shifted $V_{\rm on}$ value, and a variation of $V_{\rm on}$ upon increasing V_D [see Fig. 2(a)]. We annealed the devices to optimize the aforementioned electrical characteristics. Fig. 2(b) shows the electrical characteristics of a device annealed at 200 °C. This device shows a saturation mobility of 6.65 cm^2/Vs, $V_T =$ 3.10 V, $V_{\rm on} = -2.5$ V, SS slope = 350 mV/decade, and an $I_{\rm on}-I_{\rm off}$ ratio of 3.9×10^9. It also exhibits negligible hysteresis characteristics, as shown in Fig. 2(b). Through the post annealing process, some changes were observed between the as-fabricated and annealed devices: The $V_{\rm on}$ and V_T values shifted to the near-zero voltage of -2.5 V from -7.05 V, and the SS value decreased, which is better suitable for low-voltage drives. We believe that this result is related to a decrease in both the carrier concentration and the trap density (near conduction band and the active/GI interface) in the IGZO active layer [13]. There are also some remarkable changes in the log I_d–V_G characteristics: The variation in $V_{\rm on}$ upon increasing the V_D was reduced, the gate leakage current decreased to a value below 100 fA, and the $I_{\rm on}-I_{\rm off}$ ratio increased. There is a close relationship between the gate leakage and the drain off current. An increased gate leakage current should be accompanied by an increase drain off current, which is resulting in the decrease of on–off ratio and a change in the switching characteristics.

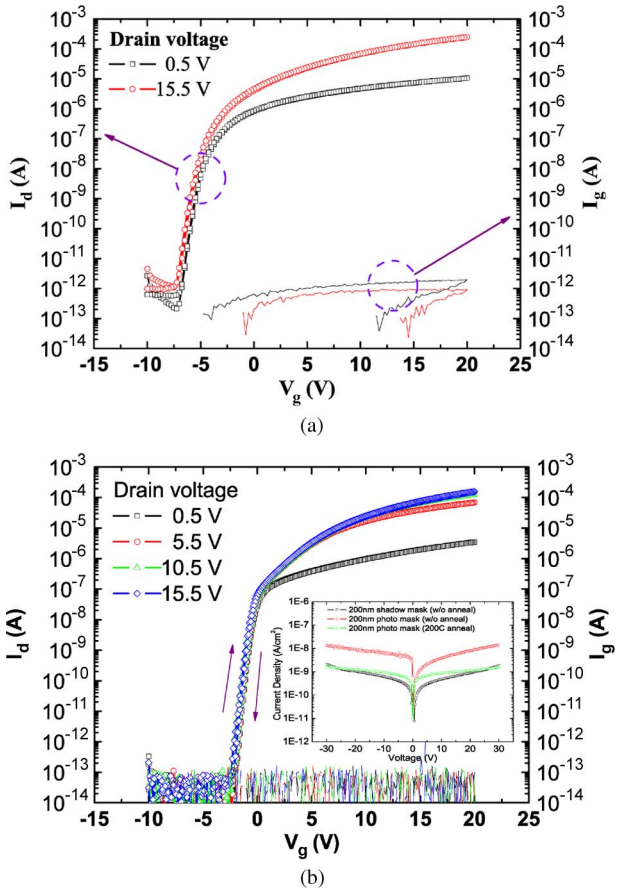

Fig. 2. log I_d–V_G curve of an as-fabricated device. (a) Before anneal. (b) After a 200 °C anneal (width = 320 and length = 20 μm).

Generally, the uniformity characteristics of oxide transistors are affected by several factors including the etching process, the composition of the oxide semiconductors, and the uniformity of the GI. When a soluble organic insulator is used, the uniformity characteristics can be additionally affected by the pinhole, the solvent residue, and the variation of GI thickness determined by the coating method or the solvent. Our device showed a satisfactory behavior with regard to the aforementioned problems. The variation in $V_{\rm on}$, V_T, and the mobility of the 16 transistors were only 0.33 V, 0.5 V, and 0.55 cm^2/Vs, respectively (data not shown). Since the electrical characteristics of oxide

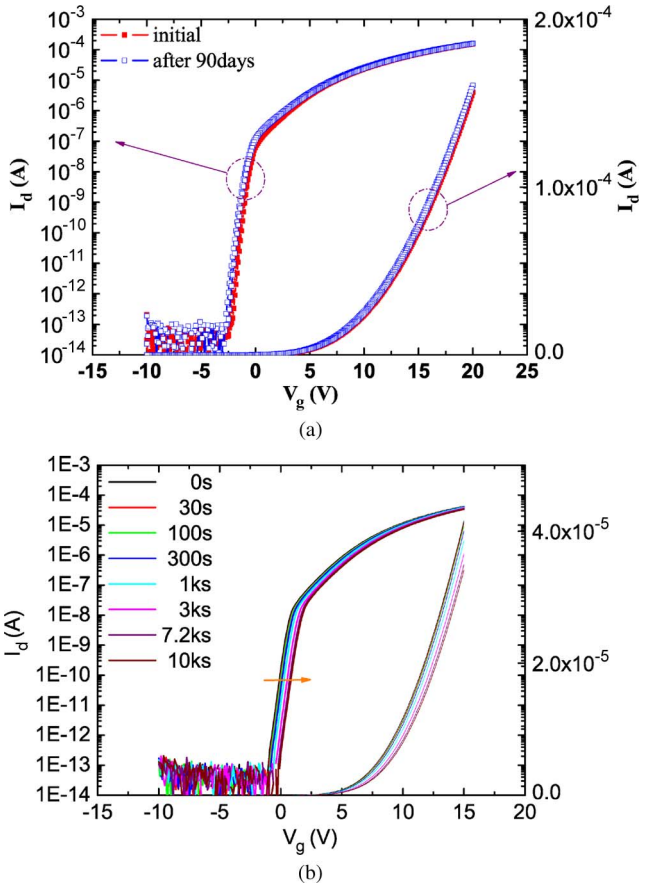

Fig. 3. (a) Environmental stability characteristics measured in 90 days under ambient conditions. (b) Gate bias stability characteristics under $V_G = 10$ V (relative humidity: 30%–65%; temperature: 18 °C–23 °C; $W = 320\ \mu$m; $L = 20\ \mu$m).

semiconductors and organic insulators without passivation layer can be easily changed under ambient conditions by the effect of oxygen or water molecules, we adopt the parylene-C passivation layer to prevent the device [14]. Then, we exposed the device to ambient air (relative humidity is 30%–65%, and temperature is 18 °C to 23 °C) for 90 days. Although water permeability characteristics of organic materials are inferior to that of inorganic layers, our device was barely affected after 90 days, as shown in Fig. 3(a). The variation in V_T and the mobility were 0.11 V and 0.06 cm^2/Vs, respectively. We believe that the ALD-grown PL layer offers sufficient protection against any changes in the stoichiometric ratio of oxygen in the IGZO active layer and that the KSPI organic insulator and parylene-C passivation layer exhibits applicable permeability properties under ambient conditions for 90 days [15]. Fig. 3(b) showed the result of constant gate bias stress of 10 V in air condition. The device showed a parallel V_T shift from 4.37 to 5.36 V (0.99 V) for 10 ks with negligible SS and mobility change. This parallel shift means that electron trapping at the active/GI interface is the main reason of the instability characteristics in our hybrid TFTs [16].

IV. Conclusion

We have manufactured a fully patterned transparent organic/inorganic hybrid transistor on a glass substrate using a soluble polyimide (KSPI) GI and a sputtered IGZO active layer. The fabricated device not only showed high performance, with a saturation mobility of 6.65 cm^2/Vs, an SS slope of 350 mV/decade, and an on–off ratio of 3.9×10^9, but it also exhibit good environmental stability in ambient air and short-range uniformity. The soluble polyimide (KSPI) GI showed acceptable chemical resistivity and permeability characteristics during the wet process and air ambient and also exhibited good insulation properties at low temperatures. The fabricated device with organic passivation layer also showed good environmental and constant gate bias stability characteristics in air and RT conditions.

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