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# Bilayered Etch-Stop Layer of $Al_2O_3/SiO_2$ for High-Mobility In–Ga–Zn–O Thin-Film Transistors

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We proposed a bilayered etch-stop layer (BiESL) composed of $Al_2O_3/SiO_2$ for the high-mobility oxide thin-film transistor (TFT) fabricated with low-resistivity Cu electrodes. The In–Ga–Zn–O TFT employing the BiESL showed no marked degradation in its high mobility and transfer characteristics even after the conventional passivation process using $SiN_x$ film, which causes hydrogen incorporation into the active channel. Excellent barrier properties of atomic-layer-deposited $Al_2O_3$ film could provide the feasibility for the direct deposition of organic planarization film without the need for an extra passivation layer. The proposed BiESL structure was also suggested to be compatible with the simple patterning process of Cu electrodes. © 2013 The Japan Society of Applied Physics

Full mass production of flat panel displays (FPD) employing oxide thin-film transistor (TFT) backplanes is coming into full swing.[1–3] Sharp (Japan) has just released liquid crystal display (LCD) panels for high-resolution television (TV) sets and low-power smartphone applications.[4] LG Display (Korea) has also unveiled its first 55-in. full-high-definition (FHD) organic light emitting diode (OLED) TV using an In–Ga–Zn–O (IGZO) TFT active matrix.[5] These movements in the industry are based on the strong demand for high-performance state-of-the-art display panels. Furthermore, such keywords as higher resolution, larger size, and lower power are expected to strongly characterize the next-generation FPDs. In order to successfully satisfy the above-mentioned requirements, high field-effect mobility of the TFT and low resistivity of the interconnection line must be achieved. Although the various channel materials of oxide semiconductors[6–10] and Cu electrodes[11–13] have been aggressively researched and developed for high-mobility TFTs and low-resistivity electrodes, respectively, we must consider the full fabrication processes to secure the device reliability and uniformity issues. The first concern is that the passivation process, which is generally carried out to protect the oxide TFTs from the ambient, has critical impact on the performances of the TFT and panels, because the hydrogen may undesirably be doped during the plasma-enhanced chemical vapor deposition (PECVD) of the $SiN_x$ layer. What is worse, this hydrogen doping effect was found to be more sensitively activated for the TFT using a high-mobility channel having a high carrier concentration.[14] We reported a double-layered passivation film structure for stably guaranteeing the device performance of IGZO TFTs with a high mobility in a previous publication.[14] The second concern is related to the fact that the Cu electrode process necessarily requires the formation of stacked structures including the capping and diffusion barrier layers to prevent surface oxidation and interdiffusion. The PECVD-grown $SiO_2$, which was proposed as an alternative to $SiN_x$ to prevent hydrogen doping, may induce the surface oxidation of Cu electrodes when the deposition temperature is higher than 200 °C. However, this complicated stacked electrode structure causes a serious problem in patterning electrodes by wet etching. From these comprehensive viewpoints, an etch-stop layer structure devised to prevent hydrogen doping into the active channel can simultaneously have the beneficial effect of preventing the surface oxidation of the Cu electrode. In this work, we propose $Al_2O_3/SiO_2$ bilayered etch-stop layer (BiESL) structure, in which a thin and dense $Al_2O_3$ film prepared by atomic layer deposition (ALD) is deposited on the PECVD $SiO_2$ layer. This approach enables us to widen the process windows in choosing the passivation process and to provide strong feasibility of achieving large-sized high-resolution FPDs.

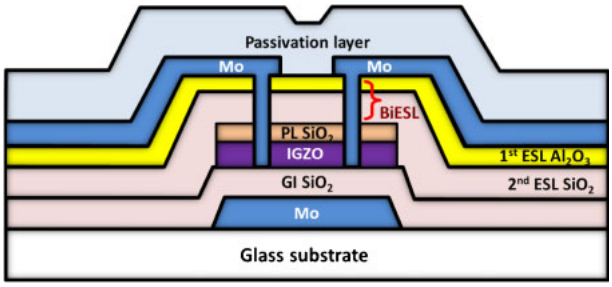


**Fig. 1.** (Color online) Schematic cross-sectional diagram of the proposed device with BiESL composed of ALD-grown $Al_2O_3$ and PECVD-grown $SiO_2$ films.

A bottom-gate IGZO TFT with the proposed BiESL was fabricated as schematically shown in Fig. 1. A molybdenum (Mo) layer with a thickness of 150 nm was patterned on a glass substrate as a gate electrode. A 200-nm-thick $SiO_2$ layer was deposited by PECVD using $SiH_4$ and $N_2O$ at 380 °C to form the gate insulator. An IGZO active layer (25 nm) and a $SiO_2$ protection layer (PL, 50 nm) were deposited by RF sputtering and PECVD, respectively. After the patterning of the PL and the active layer, the proposed BiESL was prepared with the stacked structure of a $SiO_2$ layer deposited by PECVD and a $Al_2O_3$ layer deposited by ALD. The thicknesses of the $SiO_2$ and $Al_2O_3$ layers were chosen to be 100 and 40 nm, respectively. For comparison, a control device employing only a single ESL of $SiO_2$ was also fabricated. Contact vias for the source/drain (S/D) regions and gate electrode pads were opened, followed by the deposition of Mo electrodes by sputtering and patterning by wet chemical etching. Two types of passivation films of $SiN_x$ or organic planarization layers were prepared. A 200-nm-thick $SiN_x$ passivation layer was deposited by PECVD at 300 °C. The thickness of the spin-coated organic planarization layer (produced by DongWoo Fine-Chem) was 2.6 μm, which was an acrylate-based polymer. The final annealing process for the fabricated devices was performed at 350 °C for 2 h in a vacuum.

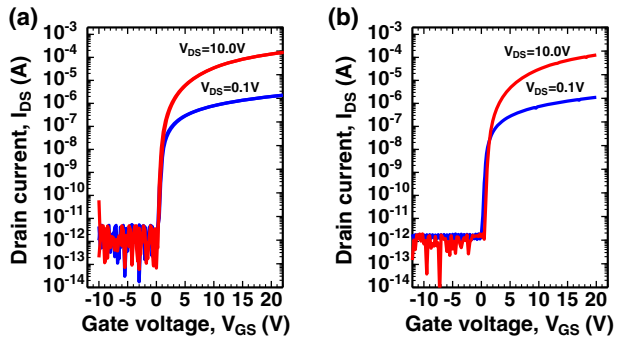


**Fig. 2.** (Color online) $I_{DS}$–$V_{GS}$ characteristics of the IGZO TFTs employing the BiESL (a) before and (b) after the passivation process using PECVD $SiN_x$. The measurements were performed in a double sweep mode of $V_{GS}$ at $V_{DS}$ of 0.1 and 10.0 V.

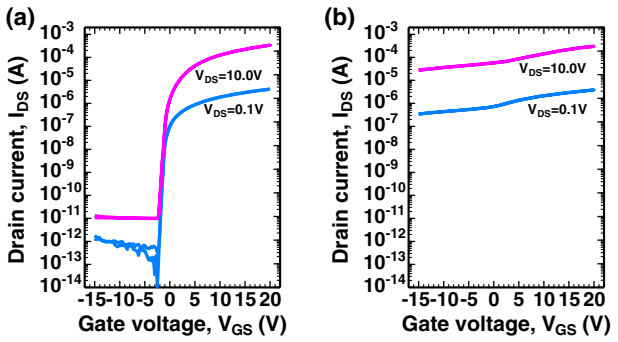


**Fig. 3.** (Color online) $I_{DS}$–$V_{GS}$ characteristics of the control device employing the single ESL of PECVD $SiO_2$ (a) before and (a) after the passivation process using PECVD $SiN_x$.

The device characteristics of the fabricated IGZO TFTs with and without the proposed BiESL were measured and compared using a semiconductor parameter analyzer (Agilent B1500A) in a dark box at room temperature. In order to investigate the barrier performance of the BiESL over a long time, shelf tests were carried out for 93 days for the TFTs with and without the organic planarization layer.

The two layers of $Al_2O_3$ and $SiO_2$ composing the proposed BiESL each play a significant role. The $Al_2O_3$ thin film prepared by ALD is known to have excellent barrier properties against oxygen and water molecules. This superior barrier property of the $Al_2O_3$ film as a passivation layer has been verified by the high performance of the OLED[15] or oxide TFT.[7,8,14] The first ESL of $Al_2O_3$ can be expected to act as an effective protection layer against hydrogen incorporation during the following passivation process. The $SiO_2$ layer, the second ESL, is introduced to provide etch selectivity between the $Al_2O_3$ and active channel layer during the formation of contacts via dry etching, as shown in Fig. 1.

Figures 2(a) and 2(b) show the drain current–gate voltage ($I_{DS}$–$V_{GS}$) transfer characteristics of the proposed device with the BiESL before and after the passivation process, respectively. The measurements were successively performed at drain voltages ($V_{DS}$) of 0.1 and 10.0 V at forward and reverse sweeps of $V_{GS}$ for each device with a gate width ($W$) and length ($L$) of 40 and 20 μm, respectively. Before the passivation process, the threshold voltage ($V_{th}$), field-effect mobility ($\mu_{fe}$), and subthreshold swing (SS) of the IGZO TFT were estimated to be 1.17 V, 29.1 $cm^2\,V^{-1}\,s^{-1}$, and 0.21 V/dec in the saturation region at $V_{DS}$ of 10.0 V, respectively. The $\mu_{fe}$ was derived by calculating the maximum value of transconductance in the plots of $(I_{DS})^{1/2}$ as a function of $V_{GS}$. These device characteristics should be confirmed to show no marked variation and/or degradation even after the PECVD $SiN_x$ passivation process. If a large amount of hydrogen was incorporated into the active channel during this process, the device might exhibit drastic changes in its performance. The values of $V_{th}$, $\mu_{fe}$, and SS for the passivated device were evaluated to be 1.0 V, 24.7 $cm^2\,V^{-1}\,s^{-1}$, and 0.17 V/dec in the saturation region, respectively. Almost the same turn-on voltage ($V_{on}$) and negligible hysteretic behaviors in the trace of $I_{DS}$ were also verified. These results suggest that the BiESL proposed in this work can be very effectively applied even for the TFT having a $\mu_{fe}$ higher than 20 $cm^2\,V^{-1}\,s^{-1}$.

In order to clearly demonstrate the potential of the BiESL structure, we investigated the device characteristics of the TFT using the same composition of IGZO and single-ESL structure of $SiO_2$ without the $Al_2O_3$ layer. As shown in Fig. 3(a), the single-ESL device exhibited sufficiently good transfer characteristics before the passivation process. The values of $\mu_{fe}$ and SS for the passivated device were 28.0 $cm^2\,V^{-1}\,s^{-1}$ and 0.21 V/dec, respectively. However, it was found that the $SiN_x$ passivation process caused a large difference in the device behaviors, as shown in Fig. 3(b). The IGZO active channel became completely conductive and the on/off switch operation of the TFT was fatally degraded. Here, we recall that the transfer curve of the oxide TFT with higher mobility was very sensitively influenced (negatively shifted) even by the incorporation of a small amount of hydrogen.[14] Consequently, the BiESL can be greatly effective in realizing a high-mobility oxide TFT protected by an $SiN_x$ passivation layer having an excellent barrier property by a conventional PECVD process.

A surface planarization prior to the pixel process is another concern of high-mobility oxide TFTs fabricated with a thick Cu S/D electrode stack. However, the conventional passivation process using an inorganic $SiN_x$ or $SiO_2$ layer is not very appropriate for planarizing the surface of TFT backplanes. The proposed BiESL also has strong potential to eliminate the sophisticated passivation layer and to combine the functions of both the ESL and the ambient barrier layer. In order to investigate the barrier property of the BiESL, a series of shelf tests was carried out for longer than 90 days, in which the test devices were naturally kept in an air ambient at room temperature. Figure 4(a) showed the variations in the transfer curves of the IGZO TFT fabricated with the BiESL without passivation. We could confirm the high sustainability of the IGZO TFT with a high mobility by the 93 day shelf test, in which the $V_{th}$ shift was negligible. This encouraging result is promising for the use of an organic planarization layer, which has been used for commercial TFT-LCDs, on the oxide TFT backplanes fabricated by a simple coating process. The variations in the transfer characteristics of the IGZO TFT coated with the organic planarization layer were also investigated with the evaluation time of 93 days,

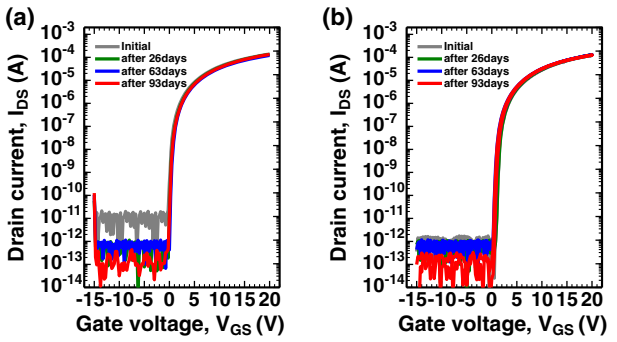


**Fig. 4.** (Color online) Variations in the $I_{DS}$–$V_{GS}$ transfer characteristics of the IGZO TFTs employing the BiESL (a) without any passivation layer and (b) coated with an organic planarization layer in shelf tests after 26, 63, and 93 days.

as shown in Fig. 4(b). The changes in $V_{th}$ and $\mu_{fe}$ were measured to be as small as $-0.45$ V and $0.05\,cm^2\,V^{-1}\,s^{-1}$. As a result, the proposed oxide TFT structure with the BiESL allows us to prepare an organic planarization film without the need for an additional passivation film thanks to the excellent barrier ability of the first ESL of ALD-grown $Al_2O_3$. The physical origins of the decrease in the off-current of the TFTs with shelf test time and the differences in the initial current level between the TFTs were not completely elucidated. A probable scenario and its reproducibility will be investigated.

A novel bilayered etch-stop layer composed of $Al_2O_3$/$SiO_2$ was proposed for the full production of oxide TFT backplanes with high mobility and Cu electrodes. Good barrier properties of ALD-grown $Al_2O_3$ that prevent hydrogen incorporation and the excellent device characteristics of the IGZO TFT fabricated to have a high mobility were verified. Consequently, with the introduction of the proposed BiESL, we can provide the following three solutions to the realization of next-generation oxide TFT backplanes for FPDs. (1) The BiESL process makes it possible to employ the conventional passivation process using PECVD $SiN_x$ film without any degradation of the device performance including the high mobility. (2) The high barrier properties of $Al_2O_3$ film can provide the feasibility of direct preparation of planarization film on the oxide TFT backplane without the need for an extra passivation layer. (3) A simple structure of the Cu electrode without any capping layer, which can be easily patterned by a single wet etching process, can also be applied thanks to the hydrogen barrier capability of $Al_2O_3$. Thus, it can be concluded that this BiESL structure would be particularly suitable for the fabrication of large-sized and high-resolution AMOLEDs, even though the oxide TFT with a bottom-gate ESL structure typically has rather large overlap capacitance compared with those of back-etch type or self-aligned devices. Furthermore, the double-layered passivation structure or gate insulator including the $Al_2O_3$ can be effectively employed for the back-channel etch gate structure or for the self-aligned top gate structure, respectively.

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