# Nondestructive Readout Operation of Oxide-Thin-Film-Transistor-Based 2T-Type Nonvolatile Memory Cell

Sung-Min Yoon, Chun-Won Byun, Shinhyuk Yang, Sang-Hee Ko Park, Doo-Hee Cho, Soon-Won Jung, Seung-Youl Kang, and Chi-Sun Hwang

***Abstract*—A two-transistor-type nonvolatile memory cell composed of one-access and one-memory thin-film transistors (TFTs) was demonstrated. ZnO and poly(vinylidene fluoride-trifluoroethylene) were employed as semiconducting channels for both TFTs and ferroelectric-gate insulator for memory TFT, respectively, in which the cell structures and fabrication procedures were so carefully designed and optimized as to effectively incorporate both TFTs on the same glass substrate without any critical process damage even below 200 °C. The fabricated memory cell successfully showed the *write* and nondestructive *readout* operations.**

***Index Terms*—Nonvolatile memory (NVM), oxide semiconductor, polymeric ferroelectric, thin-film transistor (TFT).**

## I. Introduction

EMBEDDABLE nonvolatile memories (NVMs) onto glass and plastic substrates are strongly demanded to realize multifunctional transparent and flexible electronics such as radio frequency identification tags [1], [2], sensor arrays [3], [4], "see-through" displays [5], [6], and sheet-type communication system [7]. Thin-film transistors (TFTs) using organic semiconductor (active channel) and ferroelectric copolymer [gate insulator (GI)] have been proposed as promising elements for these applications, owing to their mechanical flexibility and solution process compatibility [8], [9]. However, their small memory margin and low field-effect mobility may critically restrict the applicable scopes. On the other hand, the use of oxide semiconductor such as ZnO and In–Ga–Zn–O as an active channel layer can be another good choice because the oxide-based TFTs have been reported to typically show higher mobility and better stability in device behaviors [10], [11]. Therefore, the NVM devices composed of inorganic–organic hybrid-type gate structure can be expected to provide higher performances, as well as low-temperature process compatibility [12], [13]. Because the oxide channels are patterned into only small gate areas on the substrate, the brittleness of oxide film will no longer be a fatal problem for flexible electronic devices. The transparency in visible range is another benefit of expanding the application to the transparent devices.

The next consideration is to integrate the memory device with driver devices or logic circuitry, which will be great advances in the developments of the NVM-embeddable flexible and transparent electronic systems. Similar approaches using all-organic [7] or all-inorganic material [14] systems were introduced to build an NVM cell composed of access and memory TFTs (MTFTs). However, they are not suitable for both flexible and transparent devices. In this letter, we propose a two-transistor (2T)-type NVM cell incorporating polymeric ferroelectric-gate MTFT and oxide-based access TFT (OxTFT). This approach is very promising to realize the fully transparent NVM with high performances, such as low-power and high-speed operation at a process temperature of below 200 °C, even though several cell structures composed of 2T, including a ferroelectric-gate transistor, have been previously claimed [15], [16]. The integration process was carefully optimized, and the *write*/*readout* operations of the memory cell were successfully demonstrated for the first time.

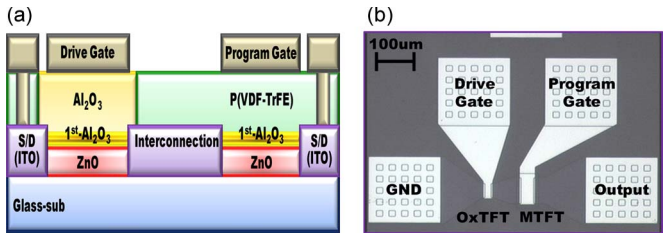


Fig. 1. (Color online) (a) Schematic cross-sectional diagram and (b) photograph of the fabricated 2T-type NVM cell integrated with OxTFT and MTFT. The gate widths and lengths ($W/L$) of OxTFT and MTFT were 40/20 and 80/40 $\mu$m, respectively.

## II. Memory Cell Fabrication

Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] was chosen as the ferroelectric copolymer for the MTFT, which has been mainly employed for these kinds of applications [8], [9], [17], [18]. The composition of P(VDF-TrFE) employed in this letter was 70/30 mol%. The oxide semiconducting channel of ZnO was prepared by the atomic layer deposition (ALD) method for both MTFT and OxTFT. Fig. 1(a) shows the cross-sectional schematic diagram of the 2T-type memory cell. In designing the cell structure and integration process, three important strategies were mapped out. The first one is to introduce

Manuscript received October 2, 2009; revised October 22, 2009. First published December 15, 2009; current version published January 27, 2010. This work was supported by the IT R&D Program of MKE/KEIT (2006-S079-04, Smart window with transparent electronic devices). The review of this letter was arranged by Editor T. Wang.

The authors are with the Convergence Components and Material Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea (e-mail: sungmin@etri.re.kr; cwbyun@etri.re.kr; ysh@etri.re.kr; shkp@etri.re.kr; chodh@etri.re.kr; jungsoonwon@etri.re.kr; kang2476@etri.re.kr; hwang-cs@etri.re.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2036137

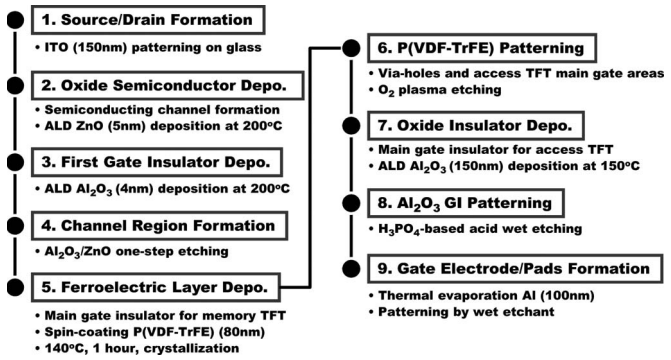


Fig. 2. Flowchart of full fabrication procedures for the proposed memory cell, which were designed to be prepared with five-photomask steps. All processes were carried out below 200 °C.

a thin first GI layer of $Al_2O_3$ between ZnO and P(VDF-TrFE) or main GI for the MTFT or OxTFT, respectively. This first GI protects the ZnO during the lithography process for the formation of channel region. It is also effective for maintaining the ZnO during the spin-coating and etching processes of P(VDF-TrFE). The solvent of P(VDF-TrFE) (dimethylformamide in this letter) and $O_2$ plasma might critically degrade the electrical natures of ZnO channel. The second one is to optimize the thickness of the ZnO and first GI–$Al_2O_3$ layers, which is closely related to the device behaviors and programming voltages for the MTFT [19]. In this letter, the thicknesses of ZnO and the first GI–$Al_2O_3$ were determined to be 5 and 4 nm, respectively. The third one is to employ the ALD-grown $Al_2O_3$ as the main GI for the OxTFT. After defining the P(VDF-TrFE) layer, the process temperatures and deposition methods for following procedures should pay very careful attention, because the higher temperature than 160 °C and/or the plasma-induced process fatally deteriorate the physical and chemical properties of P(VDF-TrFE). The melting temperature of the P(VDF-TrFE) with a molar ratio of 70/30 was reported to be approximately 155 °C [20]. The detailed fabrication procedures and process conditions can be referred to Fig. 2. A photograph of the fabricated memory cell was shown in Fig. 1(b). Although this planar-type cell structure may be undesirable in the viewpoint of cell scaling, the cell size issue is not so critical for the transparent and/or flexible electronics where this kind of memory cell would be mainly utilized. Further reduction of cell size can be achieved by building the memory cell in a vertical direction. The device and cell characteristics were evaluated using a semiconductor parameter analyzer (Agilent 4156C) and a programmable pulse generator (HP81110A) at room temperature in a dark box.

## III. Memory Cell Operation

In advance, the basic ferroelectric properties of 80-nm-thick P(VDF-TrFE) film prepared on a Pt substrate were confirmed. The remnant polarization and coercive field were typically measured to be approximately 9.5 $\mu$C/cm$^2$ and 800 kV/cm, respectively, at a frequency of 1 kHz. Fig. 3(a) and (b) shows the drain-current–gate-voltage ($I_D$–$V_G$) transfer curves and the gate leakage currents ($I_G$) for the fabricated OxTFT and MTFT, respectively, which were measured in a double-sweep mode at a drain voltage ($V_D$) of 1.0 V. It was confirmed that both

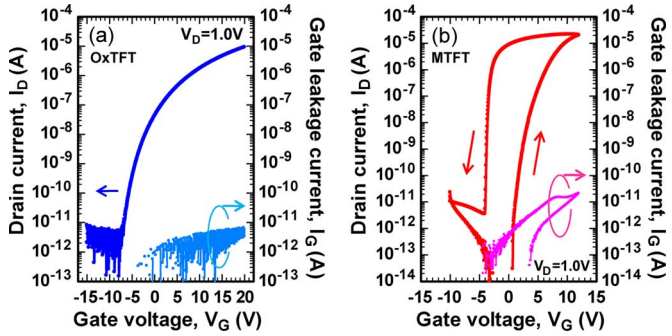


Fig. 3. $I_D$–$V_G$ transfer curves and gate leakage currents of the fabricated (a) OxTFT and (b) MTFT. The measurements were performed in a double-sweep mode of $V_G$ at a $V_D$ of 1.0 V.

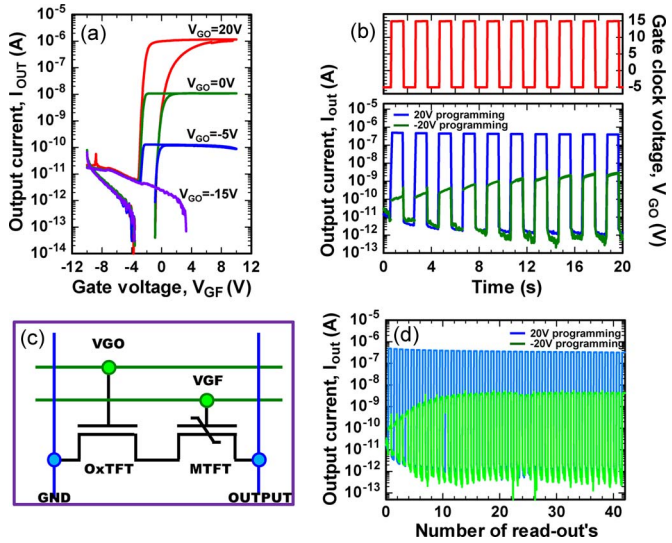


Fig. 4. (a) Sets of $I_{\rm out}$–$V_{\rm GF}$ transfer curves for the fabricated memory cell, when the $V_{\rm GO}$ was varied from −15 to 20 V. (b) Variations in $I_{\rm out}$'s of the memory cell with the time evolution when the gate clock voltage signal was continuously applied to the $V_{\rm GO}$, which was switched from −5 to 15 V with a duration of 1 s, as described by the red line. The programming events for ON and OFF were previously performed by applying *write* voltages of 20 and −20 V, respectively. (c) Schematic circuit diagram of the proposed 2T-type memory cell composed of one OxTFT and one MTFT, in which $V_{\rm GO}$ and $V_{\rm GF}$ correspond to the drive gate of OxTFT and the program gate of MTFT, respectively. (d) Example of NDROs for the ON and OFF memory states, which were measured with an interval of 1 s by applying the gate clock signal shown in (b).

TFTs exhibited good transistor behaviors, such as the *on/off* $I_D$ ratio of more than $1 \times 10^7$ and the $I_G$ as low as $10^{-11}$ A. The field-effect mobilities at the linear regime ($\mu_{\rm lin}$) and the subthreshold swings of OxTFT and MTFT were obtained to be 11.9 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$, 1.3 V/dec, 31.2 cm$^2 \cdot$ V$^{-1} \cdot$ s$^{-1}$, and 0.53 V/dec, respectively. For the case of MTFT, the counter-clockwise direction of transfer curves was clearly observed, which were originated from the ferroelectric nature of P(VDF-TrFE). The memory window was obtained to be approximately 6.2 V with a $V_G$ sweep from −10 to 12 V. These obtained results suggest that both TFTs composing the memory cell were successfully fabricated without any critical damages even after the full integration processes.

The *write* and *readout* operations of the 2T-type memory cell were evaluated. The schematic circuit diagram of the memory cell is shown in Fig. 4(c). The $V_{\rm GO}$ of OxTFT and the $V_{\rm GF}$ of

MTFT play the roles of drive and programming gates for the memory cell, respectively. Fig. 4(a) shows the transfer characteristics of the memory cell as a function of $V_{\rm GF}$, when the $V_{\rm GO}$ was varied from $-15$ to 20 V. The output currents ($I_{\rm out}$'s) of the memory cell were continuously modulated with the control of $V_{\rm GO}$, owing to the change in the channel resistance of OxTFT, which is serially connected to the MTFT. The standby current level of memory cell can be sufficiently suppressed by applying a $V_{\rm GO}$ of less than $-5$ V. Fig. 4(b) shows the *readout* operation of the memory cell. The memory states of ON and OFF were programmed by applying voltage pulses of 20 and $-20$ V to the $V_{\rm GF}$ terminal, respectively, setting the bias of output terminal to be ground. When the clock voltage signals applied to the $V_{\rm GO}$ were switched from $-5$ to 15 V and the output terminal was biased to be 1 V, the programmed $I_{\rm out}$ could be successfully read out for each memory state. However, for the disturb-free programming operation in the memory array, the cell structure should be suitably modified, and the corresponding bias conditions should be carefully controlled as future works. Repetitive nondestructive *readout* operations (NDROs) were also well confirmed, as shown in Fig. 4(d). Although a relatively long clock signal with a duration of 1 s was used to evidently show the *readout* operations for the programmed states, a higher speed NDRO, as high as tens of megahertz, can be sufficiently expected, owing to the excellent field-effect mobilities obtained for both TFTs. The $I_{\rm out}$'s of ON and OFF states were observed to be approximately $10^{-7}$ and $10^{-10}$ A, respectively. A gradually increasing trend for the $I_{\rm out}$ in the OFF state, shown in the *readout* operations, is related to the data retention behavior of the programmed state. The employed bias condition of $V_{\rm GF}$ (0 V) during the retention period might be harsher for the OFF state than for the ON state, because the MTFT operated in a depletion mode [Fig. 3(b)]. However, the *on*/*off* ratio of more than 100 could be ensured even after the 40 times repetitive *readout* operations. The voltage amplitudes of clock and programming signals can be reduced by optimizing the device performances of both TFTs. It is also interesting to note that the multilevel memory functions can be feasible for this memory cell, as shown in Fig. 4(a). For the reliable multilevel operations, the *on*/*off* ratio between each state should be extended and optimized as future works.

## IV. Conclusion

We have demonstrated a 2T-type NVM cell composed of one-access and one-memory transistors using an oxide semiconductor as a channel layer, in which ferroelectric copolymer P(VDF-TrFE) was employed as GI for the MTFT. The memory cell fabricated by using the proposed processes has shown successful *write* and *readout* operations. The obtained results have suggested that the proposed memory cell is suitable for realizing NVMs embeddable into the next-generation transparent and flexible electronic system applications.

## Acknowledgment

The authors would like thank Prof. H. Ishiwara of Tokyo Institute of Technology, Tokyo, Japan, for his help in using the electrical evaluation systems.

## References

[1] S. R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," *Nature*, vol. 428, no. 6986, pp. 911–918, Apr. 2004.

[2] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, "Pentacene-based radio-frequency identification circuitry," *Appl. Phys. Lett.*, vol. 82, no. 22, pp. 3964–3966, Jun. 2003.

[3] T. Someya, Y. Kato, S. Iba, Y. Noguchi, T. Sekitani, H. Kawaguchi, and T. Sakurai, "Integration of organic FETs with organic photodiodes for a large area, flexible, and lightweight sheet image scanners," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2502–2511, Nov. 2005.

[4] K. L. Lin and K. Jain, "Design and fabrication of stretchable multilayer self-aligned interconnects for flexible electronics and large-area sensor arrays using excimer laser photoablation," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 14–16, Jan. 2009.

[5] J. S. Park, T. W. Kim, D. Stryakhilev, J. S. Lee, S. G. An, Y. S. Pyo, D. B. Lee, Y. G. Mo, D. U. Jin, and H. K. Chung, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, p. 013503, Jan. 2009.

[6] P. Görrn, M. Sander, J. Meyer, M. Kröger, E. Becker, H. H. Johannes, W. Kowalsky, and T. Riedl, "Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes," *Adv. Mater.*, vol. 18, no. 6, pp. 738–741, Mar. 2006.

[7] T. Sekitani, K. Zaitsu, Y. Noguchi, K. Ishibe, M. Takamiya, T. Sakurai, and T. Someya, "Printed nonvolatile memory for a sheet-type communication system," *IEEE Trans. Electron Device*, vol. 56, no. 5, pp. 1027–1035, May 2009.

[8] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. de Leeuw, "High performance solution processed polymer ferroelectric field-effect transistors," *Nat. Mater.*, vol. 4, no. 3, pp. 243–248, Mar. 2005.

[9] S. J. Kang, I. Bae, Y. J. Park, T. H. Park, J. Sung, S. C. Yoon, K. H. Kim, D. H. Choi, and C. Park, "Nonvolatile ferroelectric poly(vinylidene fluoride-trifluoroethylene) memory based on a single-crystalline triisopropylsilyethynyl pentacene field-effect transistor," *Adv. Funct. Mater.*, vol. 19, no. 10, pp. 1609–1616, May 2009.

[10] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[11] S. H. K. Park, C. S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J. I. Lee, K. Lee, M. S. Oh, and S. Im, "Transparent and photo-stable ZnO thin-film transistors to drive an active matrix organic-light-emitting-diode display panel," *Adv. Mater.*, vol. 21, no. 6, pp. 678–682, Feb. 2009.

[12] S. H. Noh, W. Choi, M. S. Oh, D. K. Hwang, K. Lee, S. Im, S. Jang, and K. Kim, "ZnO-based nonvolatile memory thin-film transistors with polymer dielectric/ferroelectric double gate insulators," *Appl. Phys. Lett.*, vol. 90, no. 25, p. 253 504, Jun. 2007.

[13] K. H. Lee, G. Lee, K. Lee, M. S. Oh, S. Im, and S. M. Yoon, "High-mobility nonvolatile memory thin-film transistors with ferroelectric polymer interfacing ZnO and pentacene channels," *Adv. Mater.*, vol. 21, no. 42, pp. 4287–4291, Nov. 2009.

[14] Y. Kaneko, H. Tanaka, and Y. Kato, "First demonstration of a NOR-type memory cell incorporating a ferroelectric-gate FET memory and a ZnO-TFT selector," *Jpn. J. Appl. Phys.*, vol. 48, no. 9B, p. 09KA19, 2009.

[15] J. J. Lee and S. T. Hsu, "Two transistor ferroelectric memory," U.S. Patent 6 510 073, Jan. 21, 2003.

[16] Z. Chen, V. Joshi, M. Lim, C. A. Paz de Arauzo, and L. D. McMillan, "Ferroelectric memory and method of operating same," 6 373 743, Apr. 16, 2002.

[17] K. H. Lee, G. Lee, K. Lee, M. S. Oh, and S. Im, "Flexible low voltage nonvolatile memory transistors with pentacene channel and ferroelectric polymer," *Appl. Phys. Lett.*, vol. 94, no. 9, p. 093 304, Mar. 2009.

[18] Z. Hu, M. Tian, B. Nysten, and A. M. Jonas, "Regular arrays of highly ordered ferroelectric polymer nanostructures for non-volatile low-voltage memories," *Nat. Mater.*, vol. 8, no. 1, pp. 62–67, Jan. 2009.

[19] S. M. Yoon, S. Yang, S. H. Ko Park, S. W. Jung, C. W. Byun, D. H. Cho, S. Y. Kang, C. S. Hwang, and B. G. Yu, "Device design schemes and electrical characterization of nonvolatile memory thin-film transistors with the gate structure of Al/P(VDF-TrFE)/ $Al_2O_3$/ZnO," *Ext. Abst. Solid-State Mater. Devices*, pp. 280–281, 2009.

[20] K. Koga and H. Ohigashi, "Piezoelectricity and related properties of vinylidene fluoride and trifluoroethylene copolymers," *J. Appl. Phys.*, vol. 59, no. 6, pp. 2142–2150, Mar. 1986.