Inverters Using Only N-Type Indium Gallium Zinc Oxide Thin Film Transistors for Flat Panel Display Applications

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Inverters Using Only N-Type Indium Gallium Zinc Oxide Thin Film Transistors for Flat Panel Display Applications

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Two inverter architectures are proposed to be integrated on panels for flat panel display applications using only n-type amorphous indium gallium zinc oxide (IGZO) thin film transistors (TFTs). The proposed cross-coupled (CC) inverter uses the positive feedback effect of its CC structure to reduce the static current and increase the output voltage swing when using depletion mode n-type amorphous IGZO TFTs. The other proposed cross-coupled and bootstrapping (CCB) inverter also uses the cross-coupled structure and includes a capacitor for the bootstrapping effect to increase the operating frequency. The measured results show that the output voltage swing of the proposed CC inverter is from 0 to 14.50 V and that of the CCB inverter is from 0.15 to 14.57 V when V_{DD} is 15 V at 20 kHz and the load capacitance is 103.0 pF. The power consumption of the CC and CCB inverters are 1.4 and 2.5 mW, respectively, which are 29.3 and 53.4% of the power consumption of the ratioed inverter.

1. Introduction

Indium gallium zinc oxide (IGZO) thin film transistors (TFTs) are able to replace hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) TFTs as a backplane for active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode (AMOLED) displays owing to their relatively higher mobility from 1 to 30 $cm^2/(V \cdot s)$, on/off ratio, and electrical stability under a constant current stress than a-Si:H TFTs.[1–3] IGZO TFTs are applicable to large displays owing to their low cost process. IGZO TFTs do not require a crystallization process using laser annealing that poly-Si TFTs need. IGZO TFTs are also applicable to flexible displays because they can be fabricated on plastic substrates using a low-temperature process less than 200 °C.[1,2] Furthermore, IGZO TFTs can realize transparent displays because their 3.3 eV energy band gaps allow a high optical transmittance in the visible light region.[1,2]

Driver circuits using IGZO TFTs should be integrated on display panels for a low-cost, thin and light display system that uses the system-on-panel (SoP) technology.[4–8] An inverter is a basic element of driver circuits because it is used as a buffer to drive switching TFTs in the pixels on display panels and to drive clock lines of driver circuits. However, IGZO TFTs can use only n-type TFTs of depletion-mode-like ZnO TFTs in which their native defects, such as zinc interstitials and oxygen vacancies, become donor states.[9] Inverters with only n-type TFTs have poor pull-up devices because n-type TFTs have difficulty in transferring V_{DD}. Inverters designed with depletion-mode TFTs consume a high power owing to a large static current. Therefore, to solve the problems of poor output voltage swing and high power consumption, new inverter schemes should be applied to driver circuits using IGZO TFTs.

In this paper, new inverter schemes using IGZO TFTs are proposed to be integrated on display panels. The proposed cross-coupled (CC) inverter uses the positive feedback effect of the cross-coupled structure to reduce power consumption and to increase output voltage swing. The proposed cross-coupled and bootstrapping (CCB) inverter includes a bootstrapping capacitor in the cross-coupled structure to increase the maximum operating frequency. Two inverter architectures overcome design issues of inverter circuits using oxide TFTs, which are only n-type and depletion-mode TFTs.

2. Proposed Cross-Coupled Inverter

The proposed cross-coupled (CC) inverter consists of six TFTs and one input signal, as shown in Fig. 1(a). N1, N3, and N5 are pull-down devices, and N2, N4, and N6 are pull-up devices. N2 and N4 form the cross-coupled structure for the positive feedback loop and N6 operates as a buffer with N5. The timing diagram of the inverter is shown in Fig. 1(b) and its operation is divided in phases 1 and 2 when IN is V_{DD} and V_{SS}. In phase 1 when IN is V_{DD}, the pull-down devices, N1, N3 and N5, turn on. The gate nodes of the pull-up devices are discharged to V_{SS}, and OUT also becomes V_{SS}. In phase 2 when IN is V_{SS}, the pull-down devices turn off and the source voltages of N2 and N4 are more reduced than their gate voltages by the coupling effect of IN. The gate–source voltages (V_{GS}) of N2 and N4 increase and the current flows through N2 and N4. The gates of N2 and N4 are charged by their current, and their gate voltages increase to V_{DD} owing to the positive feedback. Therefore, the voltage signal is transferred to the buffer and OUT becomes V_{DD}. The output voltage swing of the proposed CC inverter can be nearly full using the positive feedback.

3. Proposed Cross-Coupled and Bootstrapping Inverter

The proposed cross-coupled and bootstrapping (CCB) inverter consists of seven TFTs, one capacitor, one input signal, one output signal, and one bias voltage, as shown in Fig. 2(a). To use the bootstrapping effect with the positive feedback effect of the cross-coupled structure, N1 and C1 are added to the cross-coupled structure of the inverter. V_{BIAS} is connected to the gate voltage of N1, which controls the charge on C1. N2, N4, and N6 are pull-down devices, and N3, N5, and N7 are pull-up devices. The cross-coupled structure consists of N3, N5, and C1. N6 and N7 operate as the buffer of the inverter.

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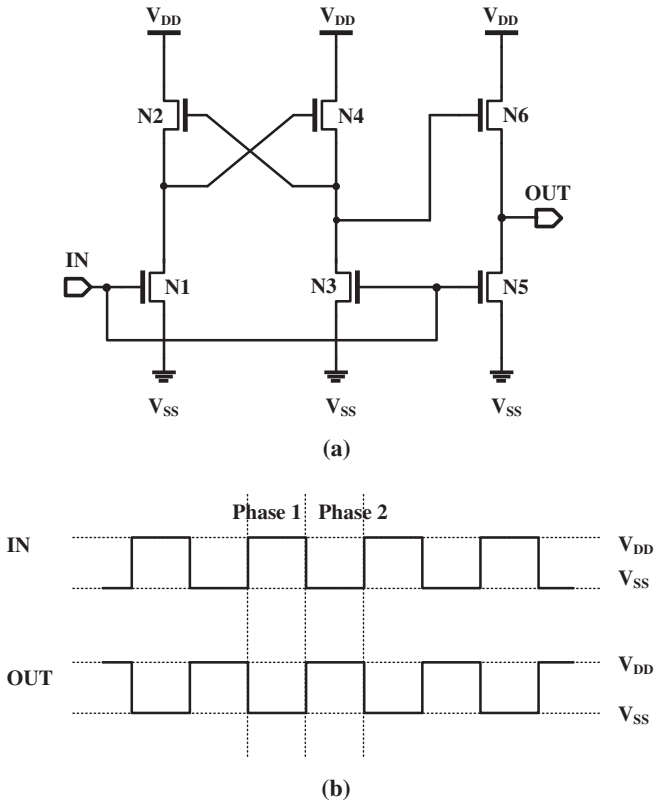

Fig. 1. (a) Schematic and (b) timing diagrams of the proposed cross-coupled inverter.

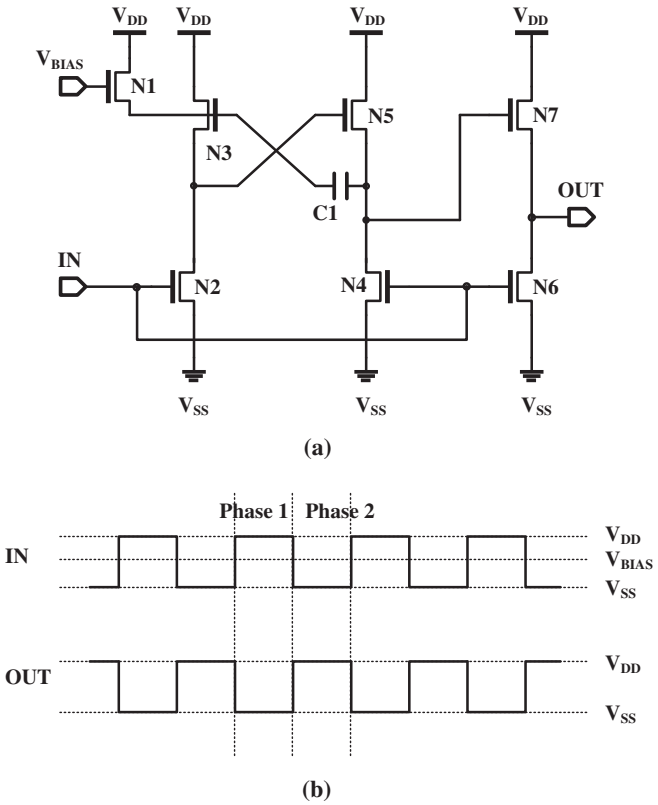

Fig. 2. (a) Schematic and (b) timing diagrams of the proposed cross-coupled and bootstrapping inverter.

Figure 2(b) represents the timing diagram of the proposed CCB inverter and its operation is divided in phases 1 and 2 when IN is V_{DD} and V_{SS}. In phase 1 when IN is V_{DD}, N2, N4, and N6 turn on and the gates of N3, N5, and N7 are discharged. OUT decreases to V_{SS}. In phase 2 when IN is V_{SS}, N2, N4, and N6 turn off. The gate voltage of N5 increases owing to the drain source current of N3 and the gate voltages of N3 and N5 increase to V_{DD} owing to the positive feedback effect. The V_{GS} of the TFTs in the cross-coupled structure is higher than that of the CC inverter because C1 maintains the V_{GS} of N3. As a result, the CCB inverter operates faster than the CC inverter. The charge on C1 is determined by V_{BIAS} and the maximum frequency of the CCB inverter is changed by C1. By V_{BIAS}, its maximum frequency is controlled.

4. Measurement Results

The proposed inverters were fabricated using amorphous IGZO TFTs as an inverse coplanar-type bottom gate structure on nonalkaline glass as a substrate. The active layer of TFTs is a 25-nm-thick IGZO layer, which is deposited by sputtering of an In_2O_3–Ga_2O_3–ZnO target with a RF magnetron sputter when the chamber pressure was 0.1 Pa of the atmosphere of 90% Ar and 10% O_2 mixed gas.[10] The source, drain, and gate electrodes of the TFTs are 150-nm-thick indium tin oxide (ITO). The gate insulator is 185-nm-thick Al_2O_3, which was fabricated by the atomic layer deposition (ALD) method at 150 °C.[10] Postannealing was conducted in vacuum using electric ovens. Figures 3(a) and 3(b) show the micrograph of the proposed CC and CCB inverters, respectively. The channel dimensions of each TFT in the proposed inverters are shown in Table I.

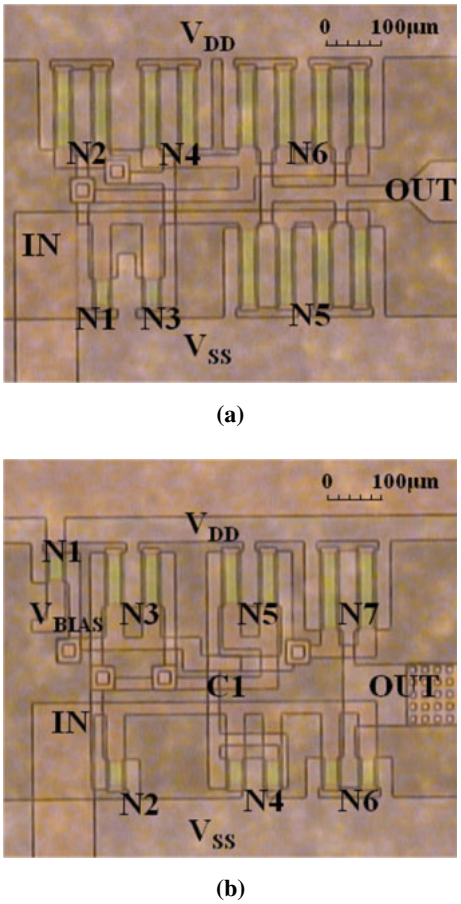

Fig. 3. (Color online) Micrographs of (a) the proposed cross-coupled inverter and (b) the proposed cross-coupled and bootstrapping inverter.

Table I. Dimensions of each TFT in the proposed inverters.

TFTs		Channel width (μm)	Channel length (μm)	Gate overlap (μm)
CC	N1	40	20	5
	N2	240	20	5
	N3	40	20	5
	N4	240	20	5
	N5	480	20	5
	N6	480	20	5
CCB	N1	40	20	5
	N2	40	20	5
	N3	160	20	5
	N4	40	20	5
	N5	160	20	5
	N6	80	20	5
	N7	240	20	5

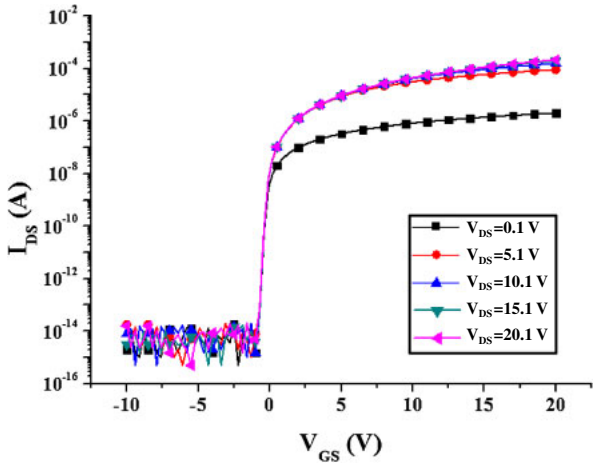

Fig. 4. (Color online) I_{DS}–V_{GS} characteristic curve of the IGZO TFT with channel width of 40 μm and channel length of 20 μm.

The electrical characteristics of the IGZO TFT whose channel width and length are 40 and 20 μm, respectively, are shown in Fig. 4. The field-effect-mobility, subthreshold slope, and on–off current ratio of the IGZO TFTs are 12.5 $cm^2/(V \cdot s)$, 168 mV/dec, and 10^9, respectively. The turn-on voltage is defined as the voltage when the drain current of the TFT is 100 pA and its value is −0.86 V.

Figures 5(a) and 5(b) show the measured results of the CC and CCB inverters, respectively, when the circuits are measured at V_{DD} of 15 V and, in the case of the CCB inverter, V_{BIAS} is 5 V. The input signal is a 20 kHz clock signal and its voltage swing is from 0 to 15 V. Figure 6 represents the voltage swing of OUT with respect to the operating frequencies of the CC inverter, the CCB inverter, and ratioed inverter that consists of a diode-connected TFT as a load and another TFT as a pull-down device.[11] The output voltage swings of the CC and CCB inverters are larger than that of the ratioed inverter which is fabricated in the same area as the proposed inverters. In the measured results, the output voltage swing of the CC inverter is from 0 to 14.50 V, that of the CCB inverter is from 0.15 to 14.57 V, and that of the ratioed inverter is from 1.38 to 13.60 V when V_{DD} is 15 V and the operating frequency is 20 kHz. The low

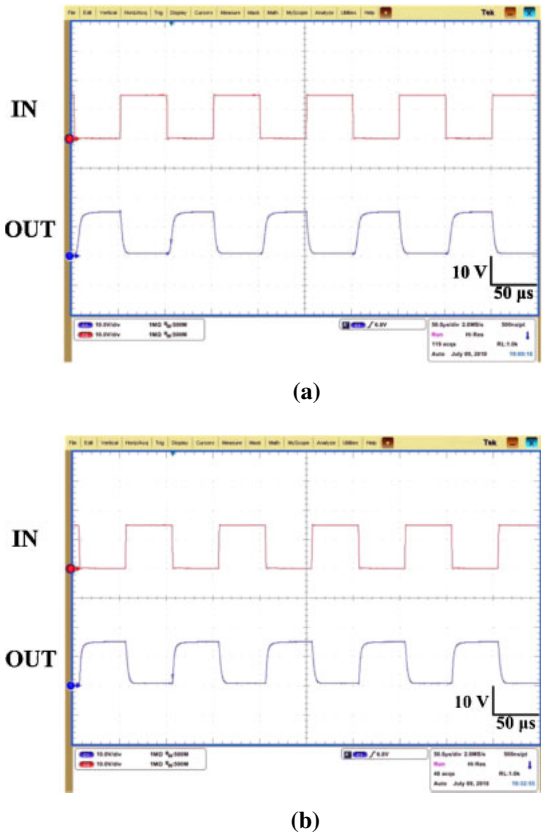

Fig. 5. (Color online) Measured results of (a) the proposed cross-coupled inverter and (b) the proposed cross-coupled and bootstrapping inverter, when V_{DD} is 15 V, the operating frequency is 20 kHz, and the load capacitance is 103.0 pF.

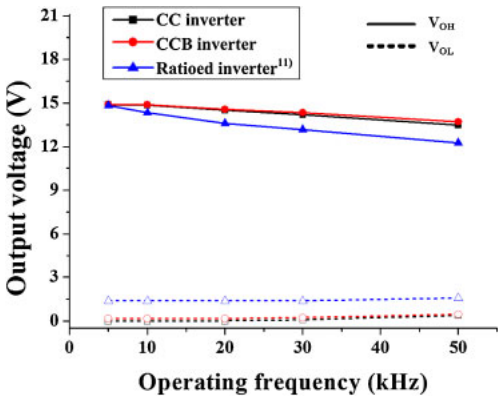

Fig. 6. (Color online) V_{OL} and V_{OH} with respect to the operating frequencies of the cross-coupled inverter, the cross-coupled and bootstrapping inverter, and the ratioed inverter.[11]

output voltage (V_{OL}) of the proposed inverters is lower than that of the ratioed inverter because the V_{GS} of the pull-up device in the proposed inverters is V_{SS} and the V_{GS} of the pull-up devices in the ratioed inverter is V_{DD}. The V_{OL} of the CCB inverter can be higher than that of the CC inverter because the remaining charge on the bootstrapping capacitor increases the short circuit currents of N2 and N3 of the CCB inverter. In the case of the ratioed inverter, its pull-down device should be designed larger than its pull-up devices to lower V_{OL}. However, when using depletion-mode TFTs, its high output voltage (V_{OH}) can be reduced by increasing the

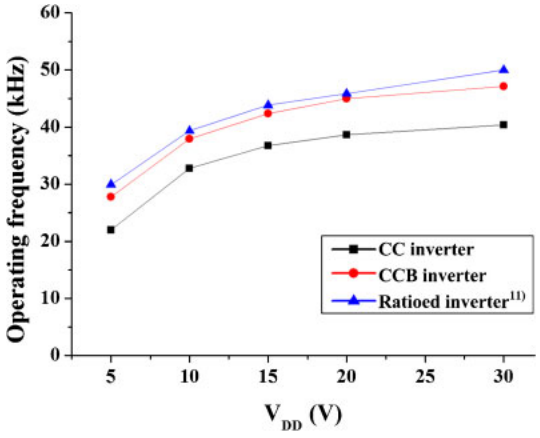

Fig. 7. (Color online) Maximum operating frequency with respect to V_{DD} values of the cross-coupled inverter, the cross-coupled and bootstrapping inverter, and the ratioed inverter.

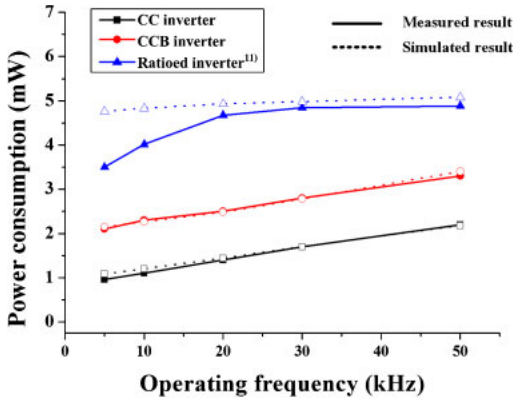

Fig. 8. (Color online) Measured and simulated power consumptions with respect to the operation frequencies of the cross-coupled inverter, the cross-coupled and bootstrapping inverter, and the ratioed inverter.[11)]

current of the pull-down devices with zero V_{GS}. Therefore, the proposed inverters have a larger output voltage swing than the ratioed inverter.

The maximum operating frequencies of the CC, CCB, and ratioed inverters with respect to V_{DD} are shown in Fig. 7. They are 32.7, 37.9, and 39.4 kHz, respectively, when V_{DD} is 15 V and the load capacitance is 103.0 pF. The CCB inverter can adjust its maximum operating frequency by controlling V_{BIAS}. Figure 8 shows the measured and simulated power consumptions of the inverters with respect to the operating frequency. The measured results show that the CC, CCB, and ratioed inverters consume 1.41, 2.53, and 4.67 mW, respectively, when V_{DD} is 15 V, V_{BIAS} is 5 V, the operating frequency is 20 kHz, and the load capacitance is 103.0 pF. The simulation results show that the power consumptions of the CC, CCB, and ratioed inverters are 1.44, 2.48, and 4.93 mW under the same conditions as those for the measured results. The simulated results are reliable because the error between the simulated and measured results is less than 7%. The power consumption of the CCB inverter is controlled by V_{BAIS} from V_{DD} to V_{SS}. When V_{BIAS} is V_{DD}, the power consumption of the CCB inverter is the same as that of the ratioed inverter and, when V_{BIAS} is V_{SS}, it is the same as that of the CC inverter. Furthermore, between V_{DD} and V_{SS}, V_{BIAS} is adjustable and power consumption is controlled between that of the CC inverter and the ratioed inverters. The CC and CCB inverters are efficient circuits because their maximum operating frequencies are 88 and 96%, respectively, of that of the ratioed inverter even though they consume about 29.3 and 53.4% of the power consumption of the ratioed inverter.

5. Conclusions

Two types of inverters using amorphous IGZO TFTs are proposed to integrate driving circuits on display panels. To overcome limitations such as the high static current and narrow swing output voltage caused in inverters using only n-type amorphous IGZO TFTs of the depletion-mode, the proposed CC and CCB inverters use the cross-coupled structure for the positive feedback effect. The CCB inverter includes a capacitor and a TFT in its cross-coupled structure to increase the maximum operating frequency. When the supply voltage is 15 V, the operating frequency is 20 kHz, and the load capacitance is 103.0 pF, the measurement results show that the maximum operating frequencies of the CC and CCB inverters are 32.7 and 37.9 kHz, respectively. Furthermore, the CC and CCB inverters consume 1.4 and 2.5 mW, respectively, which are 29.3 and 53.4% of the power consumption of the ratioed inverter. The output voltage swing of the CC inverter is from 0 to 14.50 V and that of the CCB inverter is from 0.15 to 14.57 V. The measured results of the inverters verified that they can be applied to driving circuits for FPDs of the VGA resolution format with a 60 Hz frame rate.

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