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Beneficial effect of hydrogen in aluminum oxide deposited through the atomic layer deposition method on the electrical properties of an indium–gallium–zinc oxide thin-film transistor

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ABSTRACT
Described herein is the role of hydrogen in aluminum oxide (Al_2O_3) gate dielectrics in amorphous indium–gallium–zinc oxide (a-InGaZnO or a-IGZO) thin-film transistors (TFTs). Compared to a-IGZO TFTs with a low-temperature (150°C) Al_2O_3 gate dielectric, a-IGZO devices with a high-temperature (250–300°C) Al_2O_3 gate dielectric exhibit poor transistor characteristics, such as low mobility, a high subthreshold slope, and huge hysteresis. Through DC and short-pulsed current–voltage (*I*–*V*) measurements, it was revealed that the degradation of the transistor performance stems from the charging and discharging phenomenon at the interface traps located in the interface between the a-IGZO semiconductor and the Al_2O_3 gate insulator. It was found that the low-temperature Al_2O_3 atomic layer deposition processed film contains a higher density of hydrogen atoms compared to high-deposition-temperature films. The study results show that a high concentration of hydrogen atoms can passivate the defect sites in the interface and bulk, which produces excellent transistor characteristics. This study demonstrated that hydrogen has a beneficial effect on the defect passivation for oxide TFTs.

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KEYWORDS
Oxide thin-film transistor; atomic layer deposition; aluminum oxide gate dielectric; hydrogen effect; IGZO

1. Introduction

Oxide thin-film transistors (TFTs) have been intensively studied for the switching and driving elements of a display device. To achieve a high resolution and high-speed operation of the display, the oxide TFTs must have a high degree of mobility. In addition, as the threshold voltage (V_{th}) determines the transfer behavior of TFTs, the V_{th} should be precisely controlled. In this context, it is important to understand the origin of V_{th} degradation and what is needed to prevent V_{th} instability.

In oxide TFTs, active layers with a higher carrier concentration are preferred because the mobility is proportional to the carrier concentration [1], but V_{th} control difficulty simultaneously occurs [2]. The oxygen vacancy and hydrogen in oxide semiconductors are mainly regarded as sources of charge carrier. The oxygen vacancy can be controlled through various methods, such as by increasing the oxygen partial pressure during the active sputtering, by annealing in an oxygen atmosphere, and through plasma treatment [3,4].

In terms of hydrogen, due to the high electronegativity of oxygen in the ionic bonding of oxide semiconductors, H incorporation in the oxide semiconductor is unavoidable. It is known that the hydrogen in an oxide semiconductor acts as a shallow donor by ionizing and bonding with oxygen to form –OH bonds [5–8]. As a result, it makes an oxide TFT very conductive and causes it not to show an on/off property.

The source of hydrogen in the active layer can be any of the following: (1) ambient atmosphere; (2) incorporation during the deposition of an active layer, such as the gate insulator or passivation layer; and (3) diffusion from the adjacent layers with an active layer during post-annealing. The first can be negligible when a passivation layer is adopted, but the other sources occur very often during the fabrication of oxide TFTs. Hydrogen is incorporated from the residuals in the chamber and the target surface even in a high-vacuum condition [9]. In addition, the incorporation of hydrogen into the active layer is inevitable during the deposition of

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the adjoining layers, such as the gate insulator, passivation, etch-stop, and inter-dielectric layers. These layers are normally formed using the chemical vapour deposition (CVD) and atomic layer deposition (ALD) methods, and they provide a large number of hydrogen atoms [10]. After fabrication, the post-annealing process also leads to the diffusion of hydrogen into the active layer. As a result, hydrogen can be readily incorporated into the front and/or back channel during deposition and/or post-annealing.

For V_{th} control, the hydrogen atoms that generate extra carriers and cause a negative V_{th} shift need to be controlled; as such, they are not incorporated into the active layer [11]. Various studies, however, recently reported the different roles of hydrogen in oxide semiconductors. Nomura *et al.* reported that the hydrogen atoms incorporated during the deposition process could be inactive even if they formed a hydroxyl group. In this case, the generated free electrons are compensated for by the excess oxygen [12]. In addition, the role of hydrogen in the passivation of the defects in oxide semiconductors was also reported for amorphous indium–gallium–zinc oxide (a-IGZO) TFTs [13–15]. Such papers reported that hydrogen atoms passivate defects such as electron trap sites which results in some degree of improvement of the electrical properties. The effects of hydrogen, however, have not been clearly examined so far, and further studies for this are necessary.

In this study, the role of hydrogen in determining the characteristics of oxide TFTs was examined by changing the amount of hydrogen in the gate insulator. An aluminum oxide (Al_2O_3) layer was deposited using the ALD method, and the deposition temperature was varied to control the hydrogen concentration. As a result, the Al_2O_3 gate dielectric with more hydrogen had better electrical properties in terms of hysteresis, subthreshold swing, and mobility. The hydrogen from the gate insulator could passivate not only the interfacial defects but also the oxygen-related state in the channel layer, and produced good effects in the oxide TFTs.

2. Experimental design

A bottom-gate coplanar indium–gallium–zinc oxide (IGZO) TFT was fabricated. A 150-nm-thick indium–tin–oxide (ITO)-coated glass was used as the substrate. The ITO gate electrode was patterned through a wet etching process, and then the gate dielectric layer (Al_2O_3) was deposited through the ALD, utilizing trimethylaluminum (TMA) and water as the Al and O sources, respectively. The deposition temperatures were 150, 250, and 300°C, with the same total number of process cycles (1500). Here, the Al_2O_3 layers deposited at 150, 250, and 300°C are denoted as GI-150, GI-250, and GI-300, respectively. After the wet etching of the Al_2O_3 layer for the gate electrode contact, the source/drain electrode (ITO) was sputtered and annealed at 250°C in vacuum, followed by wet etching. The 40-nm-thick IGZO film consisting of 1:1:2.5 metal elements was deposited via sputtering at room temperature for the active layer. The patterned active channel was formed through wet etching with a 40 μm width and a 20 μm length, respectively. Then a 100-nm-thick silicon dioxide (SiO_2) passivation layer was deposited through plasma-enhanced chemical vapor deposition (PECVD) at 300°C. After the whole process, the fabricated TFT was post-annealed at 300°C for 2 h in vacuum. The schematic structure and cross-sectional field emission transmission electron microscopy (FETEM, JEM-2100F, JEOL Ltd.) image of the fabricated TFT are shown in Figure 1(a) and (b), respectively.

Elemental analyses were performed using secondary ion mass spectroscopy (magnetic-sector SIMS, IMS 7f, CAMECA) with a Cs^+ primary ion source (4 kV, 15 nA). The pulsed *I*–*V* measurements were performed using a pulse generator (B1104A) and an oscilloscope unit. The electrical properties of the TFTs were measured with an Agilent B1500A semiconductor parameter analyzer.

3. Results and discussion

SIMS analysis was performed to confirm the effect of the change of the decomposition temperature on the Al_2O_3

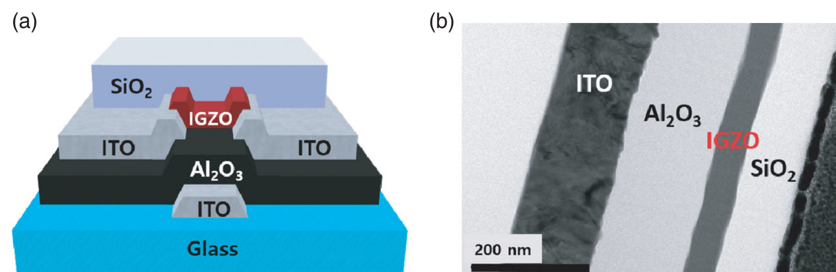

Figure 1. (a) Schematic structure of a bottom-gate coplanar TFT. (b) TEM image of the fabricated IGZO TFTs.

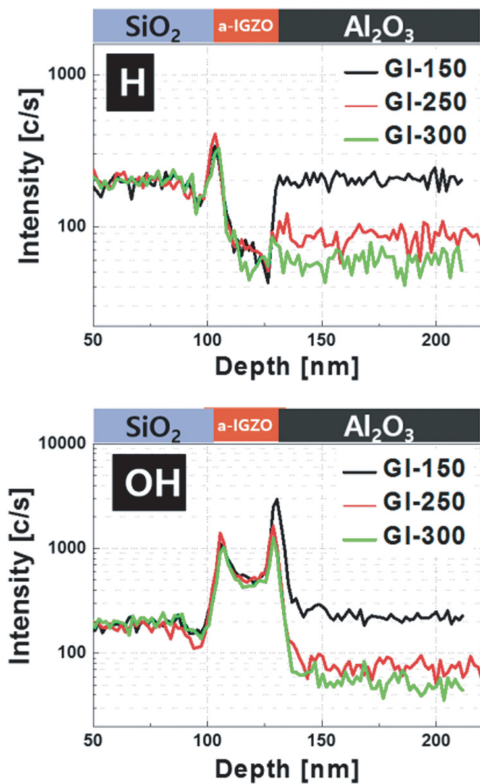

Figure 2. Results of the SIMS depth profile for hydrogen and hydroxide for the Al_2O_3 layer according to the different deposition temperatures after post-annealing at 300°C. A SiO_2/a-IGZO/Al_2O_3 structure that was the same as the TFT was prepared.

layer. SIMS samples of a SiO_2/IGZO/Al_2O_3 stack mimicking a TFT structure were prepared, and they were annealed at 300°C. The silicon in the passivation layer (SiO_2) was used to calibrate and compare the relative concentration of each element. The depth profile of the metal elements (results not shown) revealed clearly defined boundaries between the layers. The SIMS results for hydrogen and hydroxide (Figure 2) show noticeable differences according to the deposition temperature. With a lower Al_2O_3 deposition temperature, there was more hydrogen and hydroxide in the bulk region of the Al_2O_3 layer. The GI-150 film had three times higher hydrogen and hydroxide intensity than the GI-300 film. In addition, at the IGZO/Al_2O_3 interface, more hydroxide groups were indicated in the GI-150 film than in the others. The hydrogen atoms in the Al_2O_3 layer were mainly due to the steric effect and the incomplete reaction/purge during the ALD process [10]. The deposition of Al_2O_3 through the ALD method using trimethylaluminum (TMA) and water was made up of sequential reactions in terms of the adsorption of the precursors, surface reaction, and desorption of the residual species at the surface. The low deposition temperature of the Al_2O_3 film discouraged the surface reaction and desorption of residuals, which corresponds to the incomplete reaction and high-hydrogen-related species.

Figure 3 shows the transfer characteristics of the as-fabricated and post-annealed IGZO TFTs with the GI-150, GI-250, and GI-300 Al_2O_3 gate dielectrics. The final electrical properties are summarized in Table 1. Before post-annealing (Figure 3(a)–(c)), all the TFTs showed poor transfer characteristics, such as large hysteresis. The IGZO TFT with the GI-150 layer, which contained a higher amount of hydrogen, exhibited smaller hysteresis. After post-annealing, the GI-150 TFT was greatly improved and showed the best transfer behavior, with a turn-on voltage (V_{ON}) of −0.75 V, a subthreshold swing (SS) of 0.12 V/dec, and a field effect mobility (μ_{lin}) of 17.8 cm^2/Vs in the linear region. In addition, there was no hysteresis during the forward and reverse sweeps. On the other hand, as the deposition temperature increased, the TFTs still exhibited deteriorated electrical properties. Huge hystereses of 7 and 11.25 V with clockwise behavior were observed in the GI-250 and GI-300 TFTs, respectively. The mobility also decreased to 8.5 and 2.1 cm^2/Vs for the GI-250 and GI-300 TFTs, respectively. In addition, the SS increased with a higher deposition temperature of the Al_2O_3 film. In other words, the TFT with an Al_2O_3 gate insulator with more hydrogen had much improved transfer characteristics during the post-annealing process.

To understand the evolution of the TFT properties, a short-pulsed I–V measurement technique was employed [16]. Figure 4(a) shows the scheme of the pulsed I–V measurement conditions. At first, the gate voltage (V_{GS}) rose for a short time to 10 μs to avoid charge trapping with the rise in V_{GS}. Then V_{GS} remained constant for a pulse width of 2 ms, where the TFTs were turned on. When there were electron trap sites, some of the accumulated carriers in the channel were trapped, resulting in a drop of the current (I_{DS}). The amount of charge trapping at the interface and/or bulk region of a semiconductor can be compared with the drop of I_{DS} during the pulse width modulation (PWM) [17–19]. In contrast, in the case of DC I–V measurement, the charge carriers are continuously trapped during the rise in V_{GS}, which causes a lower I_{DS} compared to that in the pulsed I–V measurement.

Figure 4(b) shows the pulsed and DC I–V measurement results for the IGZO TFTs according to the Al_2O_3 decomposition temperature. As the Al_2O_3 process temperature increased, the highest current level (I_{DS}) decreased. In addition, the GI-250 and GI-300 TFTs exhibited significant I_{DS} degradation and hysteresis during PWM (i.e. the holding of the gate voltage). This result implies that the huge hysteresis of the GI-250 and GI-300 TFTs originated from the charge trapping at the trap

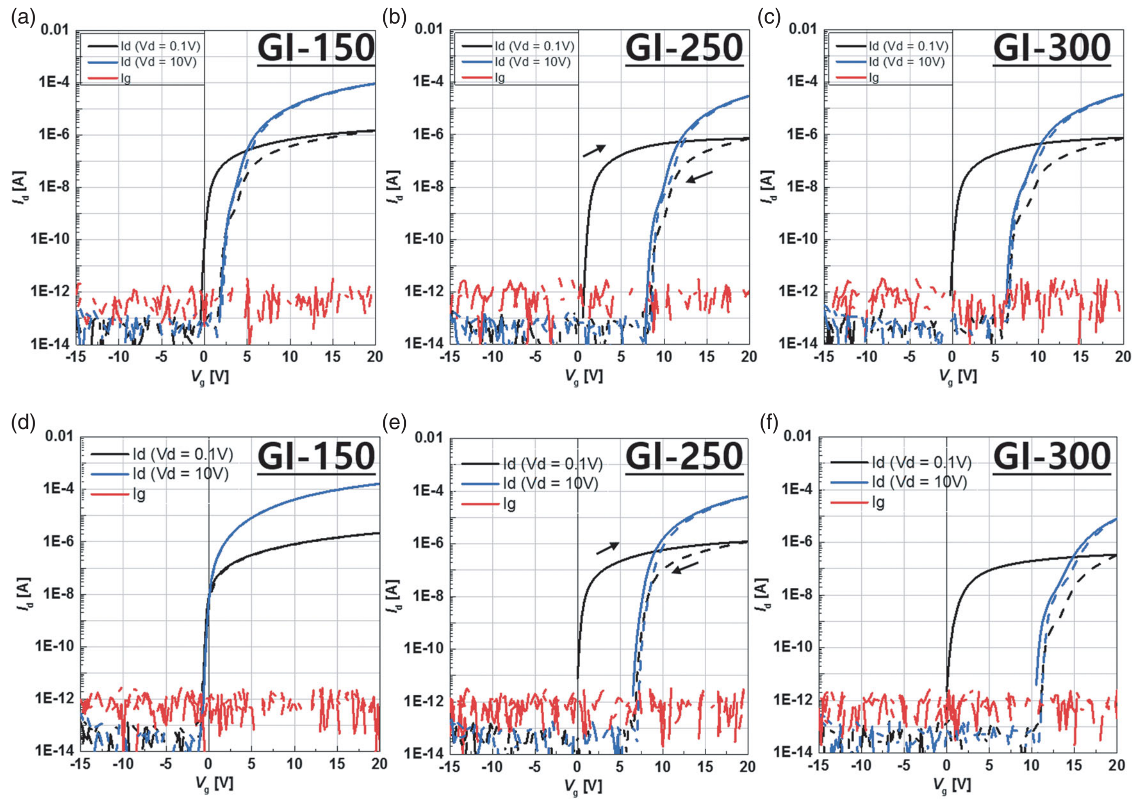

Figure 3. Transfer curves ($V_D = 0.1$ and 10 V) of the IGZO TFTs according to the various Al_2O_3 deposition temperatures (150, 250, and 300°C) before [(a)–(c)] and after [(d)–(f)] post-annealing. The post-annealing was performed at 300°C for 2 h in a vacuum.

Table 1. Summary of the electrical properties of IGZO TFTs with Al_2O_3 gate dielectrics deposited at 150, 250, and 300°C.

GI deposition temperature (°C)	V_{on} (V)	S.S (V/dec)	u_lin[a] (cm^2/V.s)	u_sat[b] (cm^2/V.s)	Hysteresis (V) @V_{ds} = 0.1 V
150°C, GI-150	−0.75	0.12	17.8	11.6	0
250°C, GI-250	0	0.17	8.5	10.6	7
300°C, GI-300	0	0.22	2.1	3.9	11.25

a = linear mobility.
b = saturation mobility.

site located at the interface and/or bulk region of the semiconductor. In contrast, the GI-150 TFT showed negligible I_{DS} degradation during PWM, and no difference between the pulse and DC I–V measurement results, which indicates that there was no shallow charge trapping at the interface [17]. As all the TFTs were fabricated using identical processes, with only the Al_2O_3 deposition temperature being different, there should be a similar defect density at the interface. From these results, it can be speculated that the generated defects of the GI-150 TFT no

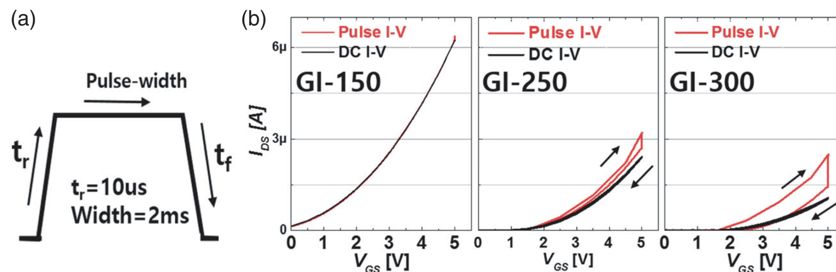

Figure 4. (a) Scheme of the pulsed I–V measurement conditions. (b) Pulsed I–V data of the IGZO TFTs with an Al_2O_3 gate dielectric deposited at 150, 250, and 300°C.

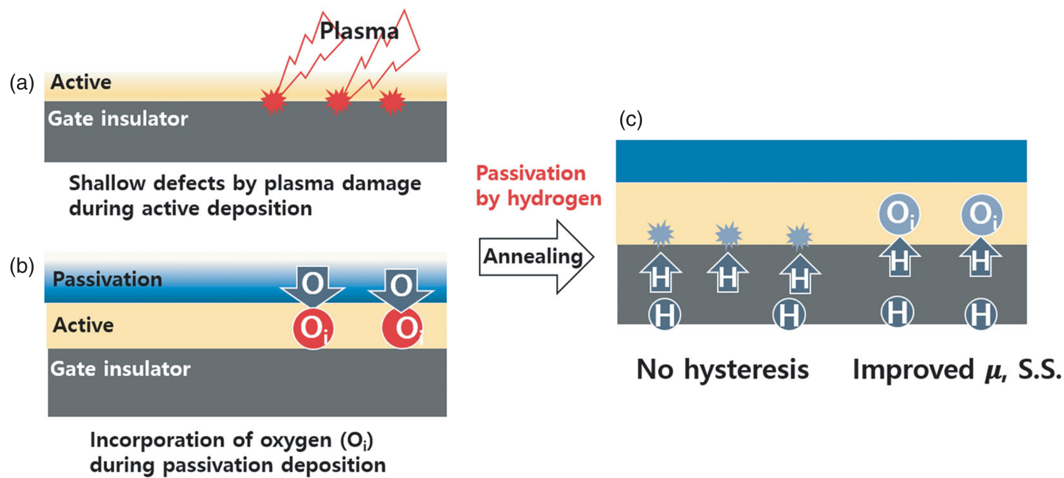

Figure 5. Schemes for the (a) generation of shallow traps during active deposition by plasma damage and (b) formation of oxygen-interstitial-(O_i)-related states during passivation deposition. (c) Passivation effect of those defects by hydrogen diffused from a gate insulator after post-annealing.

longer acted as trap sites for some reason, and that the electrical properties therefore improved.

From the above results, it can be speculated that the increased hydrogen atoms in the GI-150 TFT passivate the defect states in the active layer after post-annealing, resulting in the reduction of the trap sites and the improvement of the TFTs. Considering the TFT structure, it can be concluded that the trap sites mentioned above mainly came from the plasma damage (see Figure 5(a)). During the fabrication of the bottom-gate coplanar TFT, the active layer was directly deposited via sputtering on top of the gate dielectric. Therefore, the surface of the gate dielectric where the front channel was formed was critically damaged from the plasma [20]. The plasma damage left a large density of defects at the interface between the dielectric and the active layer. Such defects readily acted as shallow trap sites of the carrier, resulting in hysteresis. The large number of hydrogen atoms in the GI-150 TFT, however, could have easily diffused toward the active layer during post-annealing to passivate the plasma-induced traps located at the interface (Figure 5(c)). The reduction of the trap sites by passivation produced no hysteresis of the GI-150 TFT. Unlike the GI-150 TFT, the GI-250, and GI-300 TFTs contained less hydrogen, and the generated defects could not be passivated by hydrogen. Thus, huge hysteresis occurred.

In addition to the plasma damage, the degradation of the IGZO TFTs can also be ascribed to the oxygen-interstitial (O_i)-related states, as shown in Figure 5(b). During the PECVD process for the passivation layer (SiO_2), some excess oxygen can be incorporated into the active layer. Those states can act as acceptor states to degrade the mobility and SS value of the TFTs in devices with GI-250 and GI-300 layers [21]. When the gate insulator contains a high amount of hydrogen; however, as in the GI-150 TFT, those states can be passivated by the hydrogen atoms diffused from the gate insulator during post-annealing (Figure 5(c)).

In the case of the GI-300 IGZO TFT, the hysteresis increased after post-annealing. Such result, compared to the GI-150 and GI-250 TFTs, can be understood from the annealing and deposition temperature. As the deposition temperature of the GI-300 TFT was identical to the post-annealing temperature (300°C), the effect of hydrogen diffusion could not be dominant below this temperature. It is speculated that a higher annealing temperature than deposition temperature is needed for hydrogen diffusion and passivation. When the GI-300 TFT was annealed at 350°C, for instance, it also showed improvements such as less hysteresis and higher mobility (results not shown). The further understanding of the relation with the annealing temperature is under investigation.

The effect of hydrogen diffusion into the active layer from the gate dielectric is also indicated in the hall measurement results, as given in Table 2. The hall measurements were performed after the annealing of the IGZO/Al_2O_3 samples at 300°C. Note that these measurements were performed without a passivation layer. The as-deposited IGZO films with GI-150, GI-250, and GI-300 layers are too resistive to measure due to their low conductivity. After vacuum annealing at 300°C, however, the conductivities of all the films were high enough for data collection. The samples with more hydrogen had a higher carrier concentration and higher hall mobility. These results suggest that hydrogen atoms act as shallow donors when they are diffused into the active layer, as in other reports [5,7,22]. Here, it should be mentioned that the various existing tools (e.g., XPS, SIMS, and FTIR)

Table 2. Hall measurement results for the IGZO/Al_2O_3 structure after annealing at 300°C in a vacuum.

	Resistivity (Ω-cm)	Mobility (cm^2/Vs)	Carrier concentration (cm^{-3})
GI-150	0.35	14.6	1.2×10^{18}
GI-250	5.72	7.02	1.6×10^{17}
GI-300	21.44	6.6	4.4×10^{16}

cannot detect any evidence of hydrogen diffusion after annealing even though there is a significant change in the electrical properties. This confirms that an undetectable small amount of hydrogen may result in a noticeable change of the electrical properties.

The generation of defects during sputtering and/or the PECVD process and the degradation of properties from these are unavoidable in oxide TFT fabrication. Such degraded characteristics, however, can be improved by passivating the defects with hydrogen after post-annealing. These results suggest that the hydrogen in the oxide TFT films can produce not only a bad effect in terms of carrier generation but also a beneficial effect in terms of defect passivation.

4. Conclusions

The effect of hydrogen on the electrical properties of indium–gallium–zinc oxide thin-film transistors (IGZO TFTs) in terms of defect state passivation was investigated. In the bottom-gate coplanar IGZO TFTs with an atomic layer deposition (ALD)-processed aluminum oxide (Al_2O_3) gate dielectric, defects were generated during IGZO and/or silicon dioxide (SiO_2) deposition. In the IGZO TFTs with Al_2O_3 deposited at a temperature higher than 250°C, the defects led to the deteriorated performance of charge trapping at the interface between the active layer and the gate dielectric and in the bulk of the active layer. In contrast, the TFTs with an Al_2O_3 gate dielectric deposited at 150°C showed improved properties corresponding to non-charge trapping. It is believed that hydrogen with a high concentration in 150°C Al_2O_3 is diffused into the active layer and passivates the generated defects.

Disclosure statement

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