

High-Performance Hybrid Complementary Logic Inverter through Monolithic Integration of a MEMS Switch and an Oxide TFT

Yong-Ha Song, Sang-Joon Kenny Ahn, Min-Wu Kim, Jeong-Oen Lee, Chi-Sun Hwang, Jae-Eun Pi, Seung-Deok Ko, Kwang-Wook Choi, Sang-Hee Ko Park,* and Jun-Bo Yoon*

The development of micro/nano switching devices on the basis of low temperature processes has recently received a great deal of attention,^[1–3] and thereby most efforts to date have focused on thin film transistors (TFTs). In particular, TFTs based on oxide semiconductors have provided impressive progress in flat panel displays (FPDs) and flexible electronics, thanks to their relatively large mobility ($>10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), high on/off ratio, and transmission advantage.^[3–10]

While the oxide TFTs have received attention as a promising switching device, it is still challenging to exploit p-type oxide TFTs in low power integrated circuits in comparison to their n-type counterparts.^[11–25] This stems from their unacceptably poor mobility and high leakage current (low on/off current ratio), which pose critical obstacles in their practical use in low power electronics. To address these problems, many efforts have thus far been focused on utilizing Cu and Sn-based semiconductors as a p-type active layer, and corresponding fabrication methods such as evaporation,^[11–14] sputtering,^[15–19] and pulsed laser deposition^[20–25] have been continuously investigated. Nevertheless, a complementary oxide TFT circuit with reasonable performance under low fabrication temperature has not yet been demonstrated,

because controlling the hole density is tremendously difficult at the channel region of the TFTs.^[15] Thus, to realize an oxide semiconductor-based complementary circuit for ultralow power integrated circuits, the current approaches of changing the materials of the active channel layer are extremely challenging.

Here, we newly report a high-performance hybrid complementary logic inverter utilizing a MEMS switch with outstanding characteristics ranging from high on-state conduction^[26] and quasi-zero leakage current^[27] to perfectly abrupt switching behavior^[28] as a promising alternative for the p-type oxide TFT, together with an n-type oxide TFT. These two heterogeneous micro-devices are monolithically integrated together with a maximum process temperature of $250 \text{ }^\circ\text{C}$, to our knowledge, substantiating fabrication compatibility between the MEMS and oxide-based electronic devices for the first time. Being mainly attributed to the incorporation of the MEMS switch with low operation voltage (3.1 V), negligibly low off-state leakage (10^{-13} – 10^{-14} A), and high on/off current ratio ($\sim 10^9$), the hybrid complementary logic gate showed superior characteristics including a unique voltage transfer characteristic (VTC), extremely low static leakage current ($\sim 10^{-12}$ A), and large voltage gain up to 80, which are very suitable for ultralow power integrated circuits.

Figure 1a shows a conceptual illustration of the hybrid complementary logic inverter consisting of the MEMS switch and n-type oxide TFT. The MEMS switching device is operated through a three-terminal configuration similar to the oxide TFT, and electrostatically actuated by moving a suspended (conducting) electrode in contrast to the oxide TFT device which has operated by modulating the conductivity of a semiconducting channel. As illustrated in Figure 1a, the MEMS switch is vertically stacked on top of the n-type oxide TFT. Here, $1\text{-}\mu\text{m}$ thick benzocyclobutene (BCB) is utilized to electrically isolate these two electrical devices and perfectly passivate the oxide TFT during the MEMS switch fabrication (BCB is a soft and thermally stable polymer and can be easily formed by spin-coating, followed by curing at $250 \text{ }^\circ\text{C}$ ^[29]). Indeed, the fabrication method of stacking the two different devices 3-dimensionally yields both small footprint and easy fabrication compatibility.^[30] Also, through via holes in the BCB layer, a drain and gate electrodes of the MEMS switch

Dr. Y.-H. Song, S.-J. K. Ahn, Dr. M.-W. Kim, Dr. J.-O. Lee, S.-D. Ko, K.-W. Choi, Prof. J.-B. Yoon
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
291 Daehak-ro, Yuseong-gu, Daejeon
305-701, Republic of Korea
E-mail: jbyoon@ee.kaist.ac.kr

Prof. S.-H. K. Park
Department of Materials Science and Engineering
Korea Advanced Institute of Science and Technology (KAIST)
291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea
E-mail: shkp@kaist.ac.kr

Dr. C.-S. Hwang, J.-E. Pi
Oxide TFT Research Team
Electronics and Telecommunications Research Institute
138 Gajeongno, Yuseong-gu, Daejeon 305-700,
Republic of Korea

DOI: 10.1002/sml.201402841



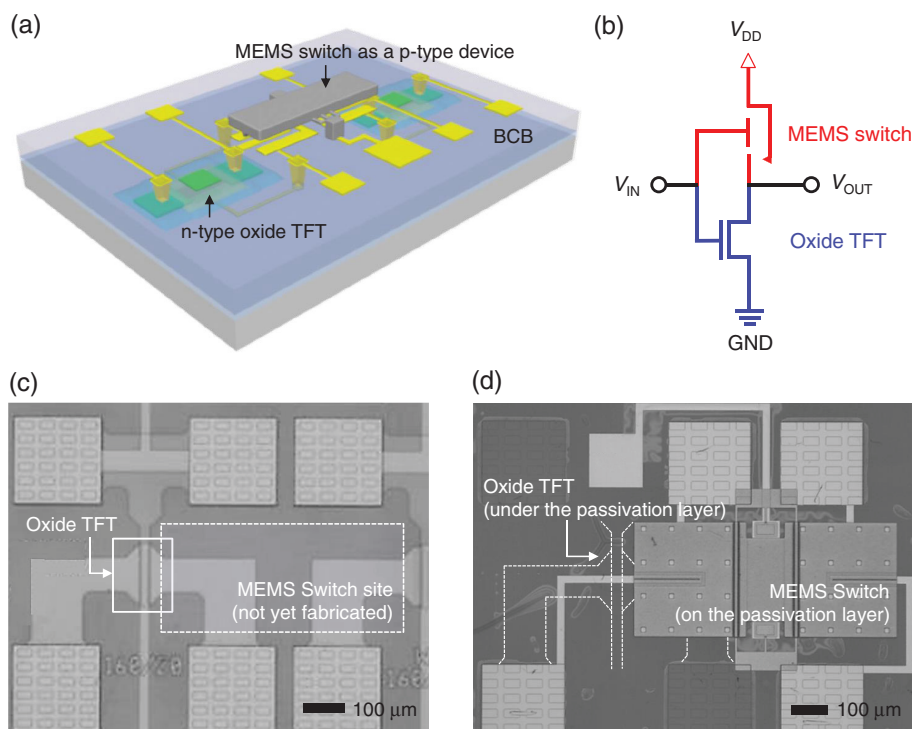


Figure 1. Proposed hybrid complementary logic inverter. (a) Schematic of the monolithically integrated hybrid logic gate with the MEMS switch and n-type oxide TFT. (b) Diagram of the suggested inverter circuit. The MEMS switch replaces the p-type oxide TFT as a “pull-up” switching component in the complementary logic inverter. Microscopic views of (c) device immediately after oxide TFT fabrication (without the MEMS switch) and (d) overall device after monolithic fabrication of the two switching components.

are electrically connected with those of the underlying oxide TFT, completing a complementary logic inverter.

By adopting the MEMS switch as a “pull-up” device in the hybrid logic inverter (Figure 1b), its mechanical features can bring about desired functionalities and significantly enhanced performance relative to that of the semiconductor switch, thus providing several attractive achievements. A typical oxide TFT logic inverter has unacceptably high static power consumption, which primarily stems from the leakage current of the p-type oxide TFT during the output logic state “0”.^[31] However, owing to the mechanical separation between the drain and suspended source electrodes of the MEMS switch at the off-state, the static power consumption can be tremendously reduced. The mechanical movement of a metal structure (conducting electrode) with high conductivity also yields perfectly abrupt switching behavior and a high on/off current ratio, and thereby high voltage gain is expected in this configuration. Furthermore, given that typical MEMS switches using surface micromachining techniques can be stably formed under a maximum temperature of 250 °C,^[32,33] the suggested hybrid logic inverter can be exploited in numerous applications such as flexible electronics where low temperature process is imperative. Actually, a complementary logic gate composed only with the mechanical switches can also be a promising candidate for low power integrated circuits, however the proposed hybrid logic inverter can possess the equivalent performance (ultralow power consumption) of the mechanical logic inverter while achieving additional advantages including small footprint, fast operation, and high current controllability.

Optical micrographs of the monolithically fabricated hybrid logic inverting device are presented in Figure 1c (before fabricating the MEMS switch; only the oxide TFT) and 1d (after fabricating the MEMS switch on the oxide TFT). It is noteworthy that monolithic integration of the MEMS and oxide-based electronic devices on a single wafer was successfully demonstrated for the first time and this result is attributed to the effective “MEMS above IC” technique^[34,35] with an appropriate passivation layer, BCB. The detailed experimental conditions in the fabrication process of the entire hybrid logic inverter are described in the Experimental Section, and the full fabrication process is illustrated in Supporting Information.

To favorably exploit the MEMS switch as a promising alternative for the hybrid logic inverter being used in ultra-low power integrated circuits, the mechanical switch must have singularly low operating voltage so as to reduce the supply voltage (V_{DD}), a task that has provided exceedingly challenging in electrostatically actuated MEMS devices (the typical turn-on voltage in conventional MEMS switches is on a scale of several tens of volts^[36,37]). As depicted in Figure 2a, the suggested MEMS switch consists of a flat beam (electrically, a source electrode) suspended by two torsional hinges, a gate and a drain electrode located in a plane area under one side of the flat beam. Note that the torsional hinge-type structure is deliberately designed as a spring of the MEMS device to reduce the operating voltage because its mechanical stiffness is significantly lower than that of the conventional cantilever-type spring^[38] (here, the calculated spring torque coefficient is as low as 6×10^{-10} N·m). Thanks to this

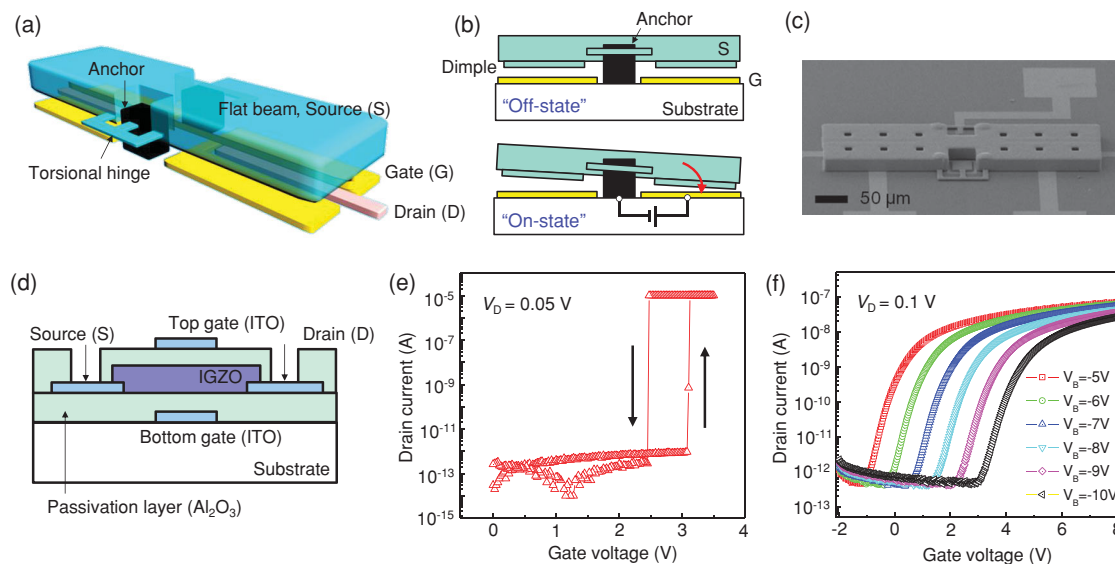


Figure 2. Structures and characteristics of the individual switching devices. (a) Schematic of the MEMS switch with the torsional hinge spring for low operation voltage. (b) Actuation mechanism at both OFF and ON states. The suspended flat beam tilts to make contact at the ON state. (c) Scanning electron microscopy (SEM) image of the fabricated MEMS switch (d) Schematic of the n-type *a*-IGZO oxide TFT with the dual-gate scheme (top and bottom gates). (e) I–V characteristics of the MEMS switch. The device provides an extremely high on/off switching ratio of 10^8 to 10^9 and has ideally-zero leakage current during the off state. (f) I–V characteristic of the n-type oxide TFT with various bias voltages applied to the top gate. The turn-on voltage is freely controlled by changing the bias voltages.

hinge-type spring with torsional movement, the flat beam is only rotated (not bent) and effectively establishes a mechanical contact with the drain electrode that is surrounded by the gate electrode (“pull-in” phenomenon) with sufficiently low bias voltage (Figure 2b). Note that the symmetric “see-saw” structure of the proposed mechanical switch can also overcome the adhesion force that is responsible for permanent contact stiction.^[39] Resonance frequency of the MEMS switch is 5.97 kHz, which is obtained from the 3D finite-element simulation. A corresponding scanning electron microscopy (SEM) image of the fabricated device is presented in Figure 2c. All detailed geometric parameters and dimensions of the MEMS switch are listed in the Supporting Information. As shown in Figure 2d, the n-type oxide TFT was designed to contain dual gates (top and bottom) so as to control its turn-on voltage freely.^[40] Here, amorphous In-Ga-Zn-O (*a*-IGZO), which is one of the primary candidates among amorphous oxide semiconductor materials, was employed for the n-type oxide TFT.^[6–8] The dimensions of the measured TFT device were 160 μm and 20 μm in channel length and width, respectively.

Figures 2e and f present the individual I–V behaviors of the fabricated MEMS switch and n-type *a*-IGZO oxide TFT, respectively. As expected, the MEMS switch showed extremely low operating voltage (i.e. pull-in voltage) of 3.1 V, which is the smallest level reported to date for an electrically-actuated micro-mechanical switch. Moreover, in comparison to solid-state switching devices, the MEMS device presented an abrupt switching behavior (sudden current increase/decrease at on/off switching transitions), remarkably high on-state conduction owing to the Au-to-Au metal contact and Ni-based beam structure, and significantly low leakage current of 10^{-13} – 10^{-14} A (below the noise level

of the parameter analyzer), thus leading to an outstanding on/off current ratio of 10^8 to 10^9 at 0.05 V drain voltage. Note that without current compliance (10 μA), the on/off current ratio can be further increased. It is readily apparent that these superior switching characteristics are mainly responsible for the enhanced power consumption and voltage gain of the hybrid logic inverter. Interestingly, the MEMS switch provided unique voltage hysteresis, caused by the nonlinear forces generated at the actuation part^[41] and adhesion force between two contact surfaces, and the corresponding detaching voltage (i.e. pull-out voltage) was about 2.5 V. This is different from the pull-in voltage of 3.1 V, thus affecting the noise margin, as explained later. Also, in terms of the n-type oxide TFT, we easily controlled the turn-on voltage by varying the bias voltage of the top gate electrode (Figure 2f). As the bias voltage applied to the top gate became more negative (from –5 V to –10 V), the turn-on voltage of the n-type oxide TFT increased (from –1 V to 3 V) due to the reduction of electrons to be depleted in the channel region.^[42] The n-type oxide TFT showed leakage current of 10^{-13} A and an on/off current ratio of 10^5 at 0.1 V drain voltage. After measuring each device’s characteristics, we found that the switching characteristics of the n-type oxide TFT were not changed during consecutive MEMS switch integration.

To evaluate the new hybrid complementary logic inverter, a voltage transfer characteristic (VTC) curve (upper part of **Figure 3**) was investigated, and at the same time the ground current (I_{GND}), which indicates the current flow from the voltage source (V_{DD}) to ground, was monitored in an air ambient (bottom part of Figure 3). In an attempt to avoid condition where both switches simultaneously turn on, we applied –10 V bias voltage to the top electrode of the n-type oxide TFT. During a single sweep of the input voltage from

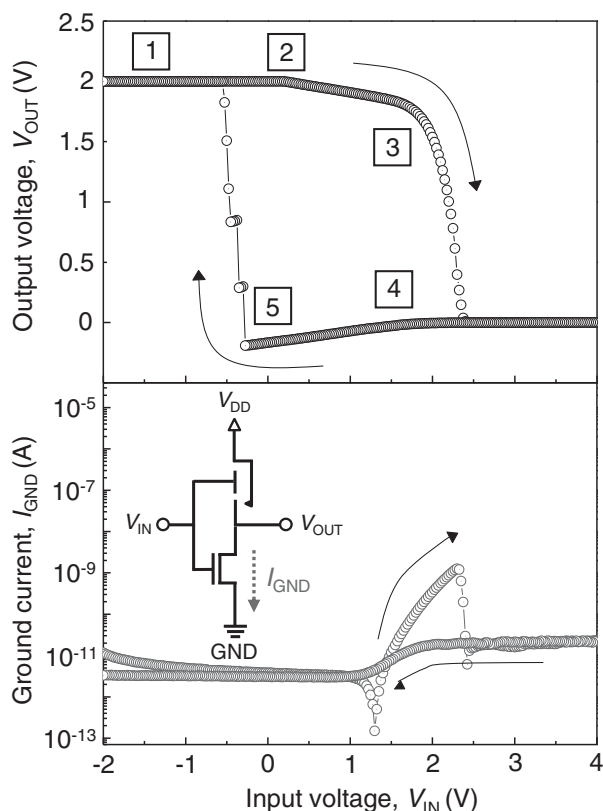


Figure 3. Voltage transfer characteristic of the hybrid complementary logic inverter and ground current (I_{GND}) that flows from V_{DD} to ground.

–2 V to 4 V, the source electrode of the MEMS switch was biased to V_{DD} (2 V) and that of the oxide TFT was electrically grounded. First, when the hybrid inverter input was close to –2 V, due to the voltage difference between the source and gate electrodes, the MEMS switch turned on, causing the output voltage to be V_{DD} (output logic state “1”): state (1). As the input voltage increased and when the voltage difference reached the pull-out voltage of the MEMS switch, the mechanical switch was detached from the output electrode (in this case, V_{DD} became “electrically floating-like” because the n-type oxide TFT remained turned off): state (2). As the input voltage increased further to a voltage where the oxide TFT becomes an active region, the output voltage gradually decreased and finally became 0 V (output logic state “0”): state (3). At this point, a peak of the ground current (I_{GND}) was observed, because charges that were confined in the output parasitic capacitor during the MEMS switch turned on began to discharge and moved to the ground. As the input voltage was then swept back to negative voltage, the n-type oxide TFT was completely turned off and the output voltage became “electrically floating-like” again: state (4). Finally, as the input voltage decreased to a level close to the initial point, –2 V, the MEMS switch was re-attached, causing the output voltage to be V_{DD} (output logic state “1”): state (5). We believe that the gradual increase of the output voltage in stage (5) can be further improved (to be abrupt) by removing and piercing thin insulating layer (for example, hydrocarbon-based contamination layer or native metal oxide film^[43,44])

deposited in the MEMS switch contact area, which is mainly responsible for the unstable contact property.^[45] Here, unlike a typical oxide TFT logic inverter, a unique voltage hysteresis behavior, which stems from the property of the MEMS switch, was observed in the VTC curve. Although it can only affect the noise margin,^[46,47] inverting operation is fundamentally the same as that of the oxide TFT logic inverter.

As shown in the bottom part of Figure 3, it is very encouraging to see that, in the output logic state “1”, the measured ground current (leakage current) was extremely negligible (10^{-12} – 10^{-11} A, noise signal level of the parameter analyzer), in comparison to other reported oxide TFT logic inverters incorporating p-type oxide TFTs with seriously high leakage current. It is therefore reasonable to conclude that this hybrid logic device could result in a significant reduction of static power consumption, and this result is mainly attributed to ideally zero-leakage current of the MEMS switch at the OFF state. Furthermore, short circuit current from V_{DD} to ground is not observed in the bottom part of Figure 3, and this also supports the ultra-low power aspect of the hybrid logic inverter.^[48] Together with these advantages, abrupt switching behavior of the mechanical switch led to an outstanding characteristic in voltage gain up to 80 (Supporting Information); this can primarily bring about a large noise margin by controlling the pull-in/out hysteresis of the MEMS switch.

We performed dynamic operation of the hybrid complementary logic inverter (Figure 4a). With $V_{DD} = 2$ V and a switching frequency (f_s) of 4 Hz, the logic gate showed a perfect inversion property, substantiating that the device can be a logic inverter candidate. Figures 4b and c present the transition times of the hybrid complementary inverter. When the output voltage was changed from logic “0” to logic “1”, the transition delay was about 100 μ s. This is mainly attributed to the mechanical delay of the suspended flat beam of the MEMS switch during the contact “closing”, since the resistance and capacitance from the MEMS switch itself are negligible. Although this delay must be further enhanced, it is noteworthy that extensive studies with respect to optimizing switch design,^[49] scaling device dimension,^[50] and adopting an advanced circuit design^[51] may present significant reductions in the turn-on delay of the mechanical switches in the near future. The transition delay when the output voltage change from logic state “1” to logic state “0” was determined by the discharge time of the confined charge in the output capacitor (electrical RC delay), and thus can be sufficiently controlled (in this case, the mechanical delay is not an important factor because mechanical detachment from the output electrode occurs instantly).

In conclusion, we have demonstrated a hybrid complementary logic inverter consisting of MEMS and oxide-based switching devices for the first time. Thanks to the introduction of the MEMS switch with outstanding switching characteristics, the resulting logic device displayed a distinctive VTC curve with 5-stages, very low static leakage of 10^{-12} A, zero-short circuit current, and exceedingly high voltage gain of 80. These measures can have significant impacts on the performance of a complementary logic inverter. Furthermore, both electrical and mechanical switches were

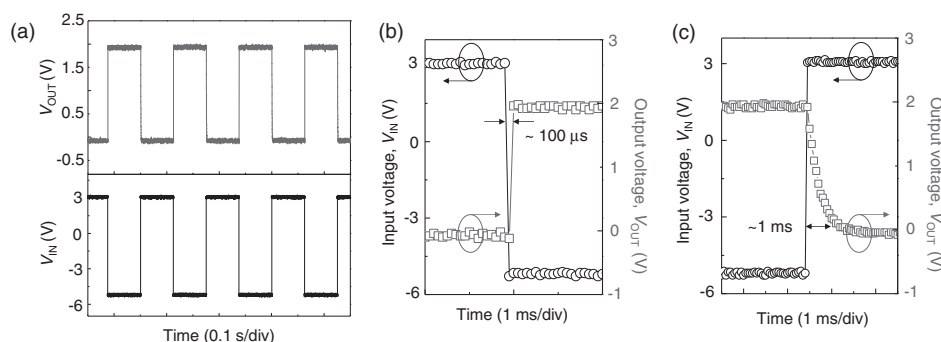


Figure 4. Dynamic operation of the inverter circuit. (a) The inverting signals with input voltage of a 4 Hz square wave. The hybrid device with the MEMS switch and oxide TFT successfully operated as a new complementary logic inverter. Transition delays when the output voltage changes to (b) logic state “1” from “0” and (c) logic state “0” from “1”.

monolithically fabricated using a low temperature (<250 °C) 3D stacking method. From these results, we believe that the mechanical switch is an excellent alternative to performance-limiting p-type oxide TFTs. We also anticipate that the suggested hybrid inverter can potentially be utilized in various applications such as ultra-low-power portable systems and flexible electronics.

Experimental Section

Full Fabrication Process: The fabrication starts with the formation of the oxide TFT's bottom gate electrode with ITO (Indium Tin Oxide) of 1500 Å thickness on a glass substrate. Next, a 1750 Å-thick alumina (Al₂O₃) layer for a gate insulator was formed by the atomic layer deposition (ALD) method at 150 °C, followed by deposition of ITO (1500 Å) for the drain and source electrodes. An active layer (*a*-IGZO, 300 Å) of the n-type oxide TFT was then deposited and patterned. An additional 1750 Å alumina layer was formed to passivate the n-type oxide TFT, and the top gate electrode was fabricated using ITO with the same thickness as the bottom gate electrode: the fabrication of the n-type oxide TFT ends at this point. Before the MEMS switch fabrication began, a 1 μm-thick insulating layer (BCB) between the n-type oxide TFT and the MEMS switch was coated, cured at temperature of up to 250 °C, and patterned with a polymer etcher to define a probe pad. Next, a 1700 Å-thick layer of Cr/Au as the bottom (gate and drain) electrodes of the MEMS switch was thermally evaporated and patterned on the cured BCB layer. Here, the Cr/Au layer was designed to have sufficient thickness for connecting the bottom layer of the MEMS switch with the TFT's electrodes electrically. After deposition of diffusion layer of Ti (1000 Å) to avoid Au/Cu alloy formation, we deposited a 4000 Å Cu sacrificial layer and patterned a dimple that mechanically makes contact with the drain electrode in switching operations. Subsequently, another sacrificial layer, Cu (4000 Å)/Ti (1000 Å), was formed to define an air gap between the bottom electrode and the suspended beam and the anchor was patterned. A 1000 Å thick Au seed layer was deposited for nickel electroplating and also to serve as a contact material. Next, a torsional hinge (5 μm) and flat beam (10 μm) were sequentially fabricated by nickel electroplating in the presence of a thick photo-resist mold. Note that it is crucial to keep the hinge thickness uniform because the thickness of the hinge significantly

affects the actuation voltage of the MEMS switch. All unnecessary seed and sacrificial layers were selectively removed and the MEMS switch was released using critical point drying to prevent stiction.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Y.-H.S. and S.-J.K.A contributed equally to this work. This work was supported in part by a Korean Science and Engineering Foundation grant and in part by the Smart IT Convergence System Research Center funded by the Korean Ministry of Education, Science and Technology under Grant R11-2007-045-03003-0.

- [1] B. D. Gates, *Science* **2009**, *323*, 1566.
- [2] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, *Nat. Mater.* **2011**, *10*, 45.
- [3] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.
- [4] P. T. Liu, Y. T. Chou, L. F. Teng, *Appl. Phys. Lett.* **2009**, *95*, 233504.
- [5] B. Yaglioglu, H. Y. Yeom, R. Beresford, D. C. Painea, *Appl. Phys. Lett.* **2006**, *89*, 062103.
- [6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, *432*, 488.
- [7] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C. H. Park, D. A. Keszler, *J. Appl. Phys.* **2005**, *97*, 064505.
- [8] P. T. Liu, Y. T. Chou, L. F. Teng, C. S. Fuh, *Appl. Phys. Lett.* **2010**, *97*, 083505.
- [9] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo, H. D. Kim, *Appl. Phys. Lett.* **2007**, *91*, 113505.
- [10] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, D. a. Keszler, *Appl. Phys. Lett.* **2005**, *86*, 013503.
- [11] C. W. Ou, Z. Y. Ho, Y. C. Chuang, S. S. Cheng, M. C. Wu, K. C. Ho, C. W. Chu, *Appl. Phys. Lett.* **2008**, *92*, 122113.
- [12] C. W. Chu, C. W. Ou, M. C. Wu, Z. Y. Ho, K. C. Ho, S. W. Lee, *Appl. Phys. Lett.* **2008**, *92*, 232103.

- [13] H. N. Lee, H. J. Kim, C. K. Kim, *Jpn. J. Appl. Phys.* **2010**, *49*, 020202.
- [14] L. Y. Liang, Z. M. Liu, H. T. Cao, Z. Yu, Y. Y. Shi, A. H. Chen, H. Z. Zhang, Y. Q. Fang, X. L. Fang, X. L. Sun, *J. Electrochem. Soc.* **2010**, *157*, H598.
- [15] E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Goncalves, S. H. K. Park, C. S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, *96*, 192102.
- [16] S. Y. Sung, S. Y. Kim, K. M. Jo, J. H. Lee, J. J. Kim, S. G. Kim, K. H. Chai, S. J. Pearton, D. P. Norton, Y. W. Heo, *Appl. Phys. Lett.* **2010**, *97*, 222109.
- [17] E. Fortunato, R. Barros, P. Barquinha, V. Figueiredo, S. H. K. Park, C. S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, *97*, 052105.
- [18] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2010**, *97*, 72111.
- [19] E. Fortunato, R. Martins, *Phys. Status Solidi – Rapid Res. Lett.* **2011**, *5*, 336.
- [20] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, *93*, 032113.
- [21] K. Nomura, T. Kamiya, H. Hosono, *Adv. Mater.* **2011**, *23*, 3431.
- [22] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, *93*, 202107.
- [23] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Phys. Status Solidi A* **2009**, *206*, 2192.
- [24] X. A. Zou, G. J. Fang, L. Y. Yuan, M. Y. Li, W. J. Guan, X. Z. Zhao, *IEEE Electron Device Lett.* **2010**, *31*, 827.
- [25] X. A. Zou, G. J. Fang, J. Wan, X. He, H. Wang, N. Liu, H. Long, X. Z. Zhao, *IEEE Electron Device Lett.* **2011**, *58*, 2003.
- [26] Y.-H. Song, D.-H. Choi, H.-H. Yang, J.-B. Yoon, *J. Microelectromech. Syst.* **2011**, *20*, 1.
- [27] J. W. Choi, J.-I. Lee, Y. K. Eun, M.-O. Kim, J. Kim, *Adv. Mater.* **2011**, *23*, 19.
- [28] M. Spenser, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. K. Liu, D. Markovic, E. Alon, V. Stojanovic, *IEEE J. Solid-State Circuits* **2011**, *46*, 1.
- [29] G. F. Meyers, M. T. Dineen, E. O. Shaffer, II, T. Stokick, Jr., J. H. Im, *Macromol. Symp.* **2001**, *167*, 1.
- [30] P. V. Cicek, Q. Zhang, T. Saha, S. Mahdavi, K. Allidina, F. Nabki, M. E. Gamai, *J. Micromech. Microeng.* **2013**, *23*, 065013.
- [31] H. Ozaki, T. Kawamura, H. Wakana, T. Yamazoe, H. Uchiyama, *Symposium on VLSI Circuits*, Honolulu HI, June **2011**.
- [32] H. A. C. Tilmans, H. Ziad, H. Jansen, O. D. Monaco, A. Jourdain, W. D. Raedt, X. Rottenberg, E. D. Backer, A. Decaussemaeker, K. Baert, *IEEE Int. Electron Devices Meeting*, Washington USA, Dec **2011**.
- [33] C. Chang, P. Chang, *Sens. Actuators A, Phys.* **2000**, *79*, 1.
- [34] D. Saias, P. Robert, S. Boret, C. Billard, G. Bouche, D. Belot, P. Ancey, *IEEE J. Solid-State Circuits* **2003**, *38*, 12.
- [35] J. Bryzek, A. Flannery, D. Skurnik, *IEEE Instrum. Meas. Mag* **2004**, *7*, 2.
- [36] Radant MEMS <http://www.radantmems.com/radantmems/switchperformance.html>, accessed: Oct, 2014.
- [37] Y.-H. Song, M.-W. Kim, M.-H. Seo, J.-B. Yoon, *J. Microelectromech. Syst.* **2014**, *23*, 3.
- [38] Y.-H. Song, C.-H. Han, M.-W. Kim, J. O. Lee, J.-B. Yoon, *J. Microelectromech. Syst.* **2012**, *21*, 5.
- [39] M.-W. Kim, Y.-H. Song, H.-H. Yang, J.-B. Yoon, *J. Micromech. Microeng.* **2013**, *23*, 4.
- [40] T.-H. Hwang, I.-S. Yang, O.-K. Kwon, M.-K. Ryu, C.-W. Byun, C.-S. Hwang, S.-H. Park, *Jpn. J. Appl. Phys.* **2011**, *50*, 03CB06–1–03CB06–4.
- [41] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology*, 1st ed., Wiley, Hoboken, NJ, 2003, Ch. 2.6, pp.36–38.
- [42] K. Takechi, M. Nakata, K. Azuma, H. Yamaguchi, S. Kaneko, *IEEE Transactions on Electron Devices* **2009**, *56*, 9.
- [43] D. Hyman, M. Mehregany, *IEEE Trans. Comp. Pack. Technol.* **1999**, *22*, 357.
- [44] S. T. Patton, J. S. Zabinski, *Tribol. Lett.* **2005**, *18*, 215.
- [45] O. Rezvanian, M. Zikry, C. Brown, J. Krim, *J. Micromech. Microeng.* **2007**, doi: 10.1088/0960–1317/17/10/012.
- [46] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.-S. P. Wong, *IEEE IEDM Tech. Dig.* **Dec 2007**.
- [47] V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, T. J. K. Liu. *Proc. IEEE* **2010**, *98*, 2076.
- [48] S. Chakraborty, T. K. Bhattacharyya, *J. Micromech. Microeng.* **2010**, *20*, 105026.
- [49] M.-W. Kim, Y.-H. Song, J.-B. Yoon, *J. Micromech. Microeng.* **2011**, *21*, 115009.
- [50] J. O. Lee, Y.-H. Song, M.-W. Kim, M.-H. Kang, J.-S. Oh, H.-H. Yang, J.-B. Yoon, *Nat. Nanotechnol.* **2013**, *8*, 36.
- [51] F. Chen, H. Kam, D. Markovic, T.-J. K. Liu, V. Stojanovic, E. Alon, *IEEE ICCAD Tech. Dig* **Dec 2008**.

Received: September 23, 2014

Revised: October 15, 2014

Published online: November 22, 2014