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Letter

A simple shift register circuit for depletion-mode oxide TFTs

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ABSTRACT

We report the simplest shift register circuit compatible with metal-oxide thin-film transistors (TFTs). Since the oxide TFT often exhibits depletion-mode characteristic, it is impossible to guarantee stable operation of the shift register when we resort to conventional circuit scheme. In order to resolve this problem, we employed two different low-voltage levels for the clock signals. As a result, we could turn off the depletion-mode oxide TFTs completely with sufficient voltage margin. According to the simulation results, the new shift register composed of only 6 TFTs operates properly over the threshold voltage (V_T) range of −5–+9 V. The fabricated circuit also worked successfully even though V_T of the TFTs ranged from −5 V to −3 V.

1. Introduction

As the frame frequency and the resolution of the active-matrix liquid–crystal display (AMLCD) are enhanced, the on-current of the thin film transistor (TFT) should be improved as well as the signal line conductance to deliver the data signal to each pixel within limited switch-on time [1,2]. Accordingly the prevailing amorphous silicon (a-Si) TFT is no more suitable for higher performance AMLCDs. Although the polycrystalline silicon (poly-Si) TFT meets the requirements, the high process cost of poly-Si TFT is still a critical obstacle to mid- to large-area displays. TFTs employing metal–oxide semiconductors such as In–Ga–Zn–O (IGZO) have attracted much attention in recent years because they exhibit high carrier mobility and low process cost [3,4]. The oxide TFT is also expected to be used in the active-matrix organic light-emitting diode (AMOLED) display because it is more stable than the a-Si TFT and has better short-range uniformity than the laser-annealed poly-Si TFT [5–7].

However the oxide TFT often exhibits depletion-mode characteristics by process fluctuation and external influences such as illumination and bias stress [8,9]. Accordingly a considerable amount of current flows at zero gate-to-source bias (V_{GS}). Due to the possible negative threshold voltage (V_T) of the oxide TFTs, it is not desirable to utilize conventional circuit scheme when we integrate driving circuitry on a display panel. Kim and Kang have reported new shift register circuits that are suitable for the depletion-mode oxide TFTs [10,11]. However these circuits need too many TFTs. In this paper, we propose a simple 6-TFT shift register circuit which operates properly with the depletion-mode oxide TFTs by employing two different low voltage levels for the clock signals. This circuit is more useful in reducing the bezel width of the display panel than the previous ones especially when it is used for the mobile displays where the size of the buffer TFT is not so large due to the high mobility of the oxide TFT and the small gate line load because the number of TFTs are reduced to half.

2. Operation of the new shift register

Each stage of the new shift register is composed of only six TFTs and one capacitor as shown in Fig. 1a. This is the simplest oxide-TFT-based shift register circuit that has been ever reported. TFT M1 admits the output of previous stage. TFT M3 transfers CLK_A signal to the output with the aid of bootstrapping when current stage has received high level of OUT[N-1]. Capacitor C_b facilitates the bootstrapping effect. M4 keeps OUT[N] low when OUT[N] should be low. M4 is controlled by PD node that is maintained at high level as long as OUT[N] does not go high. When OUT[N] becomes high, M6 is turned on and the voltage of PD node goes low. In this case, the pull-down TFT M4 is only slightly turned on and OUT[N] reaches similar high level of CLK_A. In the following phases, M2 pulls down F node periodically and M5 pulls up PD node, which keep the two nodes F and OUT[N] at low level.

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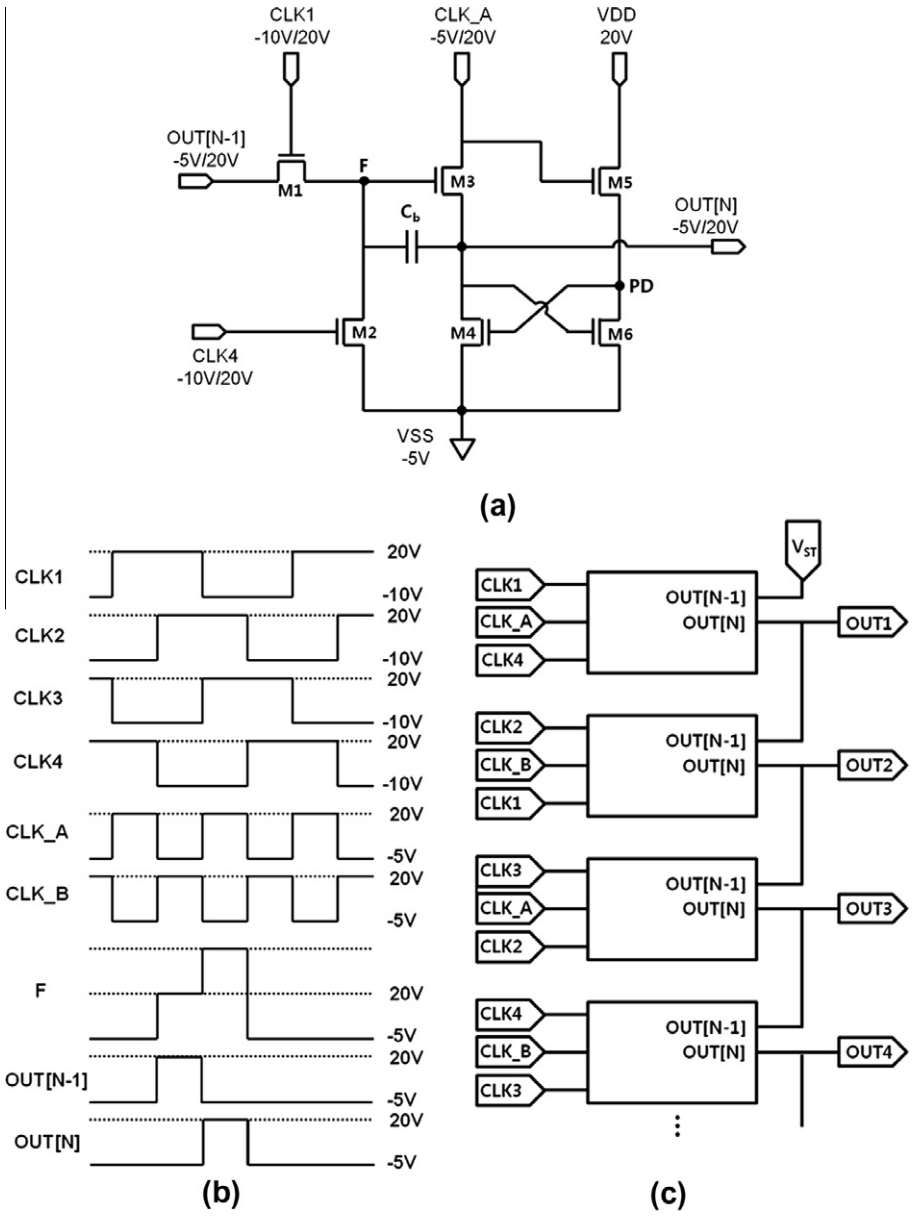

Fig. 1. (a) Single stage of proposed shift register compatible with depletion-mode oxide TFTs. (b) Timing diagram of input and output signals. (c) Block diagram showing signal connections.

In order to guarantee proper operation, the floating node F should be isolated during the bootstrapping phase. In order to turn off the switch TFTs M1 and M2 completely during this period even though they have negative V_Ts, we employed CLK1 ~ 4 that have more negative low-level than CLK_A and CLK_B that are used as the output pulses. One example of the swing ranges of the clock signals are illustrated in Fig. 1b. In this example, −10 V of CLK1 and CLK4 are applied to the gates of M1 and M2 respectively where the source voltages are −5 V. Therefore M1 and M2 have approximately −5 V of turn-off V_{GS} margin. The connection of the clock signals for the first four stages are shown in Fig. 1c and it is repeated every four stages.

The other TFTs (M3–M6) can also be slightly turned on since they have "zero" V_{GS}s as an off-state bias. However this does not lead to severe abnormal operation because even if M3 becomes slightly conducting with negative V_T, the pull-down TFT M4 maintains the output at low level whenever CLK_A is high since the voltage of PD node is raised enough by M5 during this time even

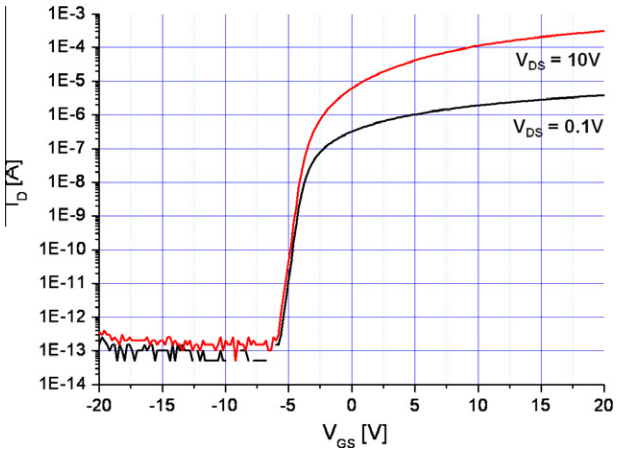

Fig. 2. Measured characteristics of typical IGZO TFT. W/L = 50/20 μm, V_T = −2.3 V.

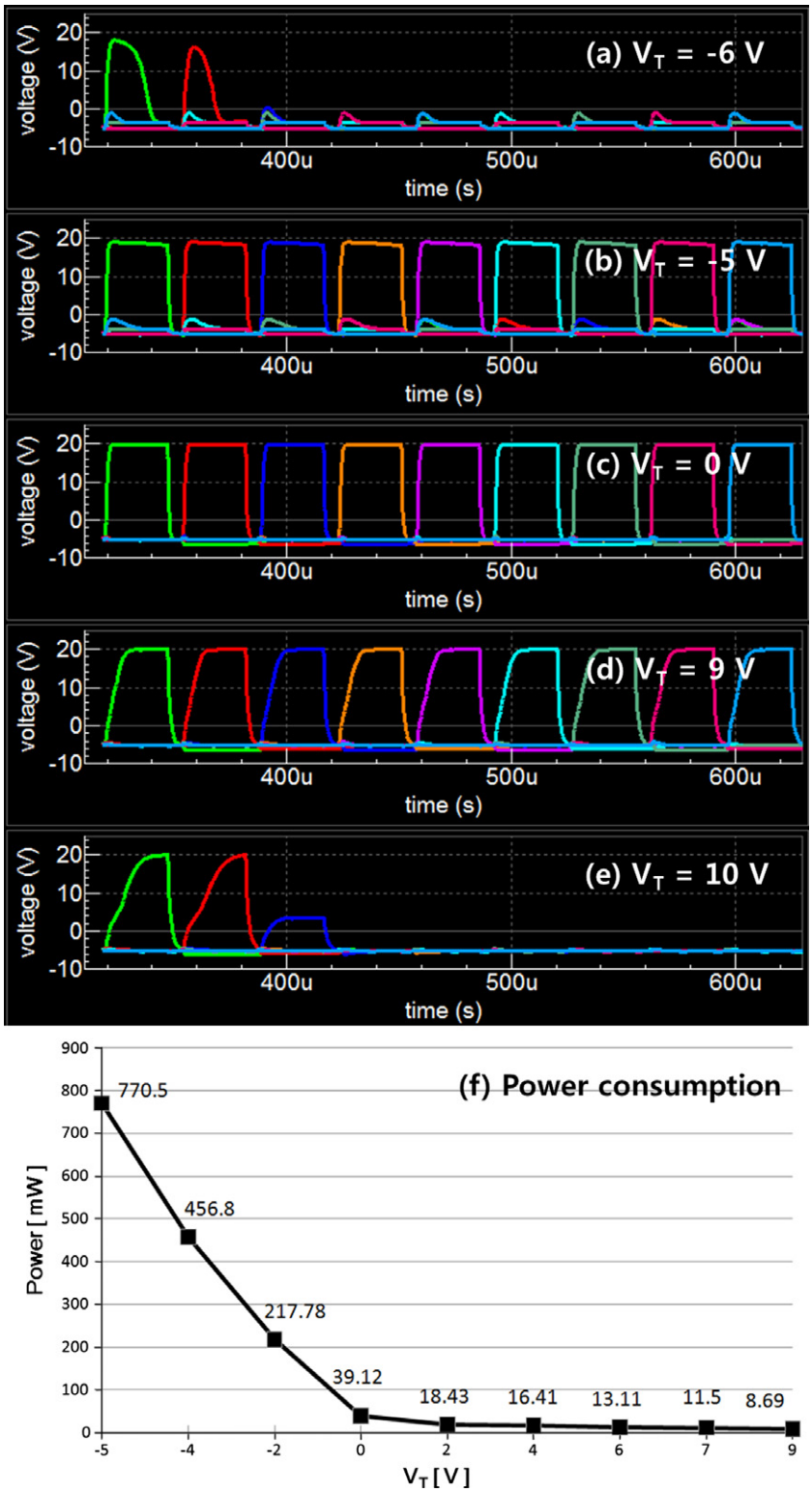

Fig. 3. Simulated waveforms of output signals with IGZO TFT models of (a) $V_T = -6$ V, (b) $V_T = -5$ V, (c) $V_T = 0$ V, (d) $V_T = 9$ V, and (e) $V_T = 10$ V. (f) Power consumption versus TFT V_T for VGA (640 × 480) AMLCD driving. Frame rate is 60 Hz.

though M5 and M6 have negative V_Ts. In addition, it becomes easier to turn on M4 when it has negative V_T. When CLK_A is low, OUT[N] is kept low even if the PD node is pulled down by the leaky M6, because there is no source to raise the output voltage. On the other hand when bootstrapping occurs in node F, although M4 may be slightly turned on, fully-conducting M3 pulls up OUT[N] very close to 20 V.

3. Results

We used SmartSpice to verify the operation of the new shift register circuit. We made a TFT model by fitting the measured IGZO TFT characteristics shown in Fig. 2. The channel width and length of the TFT are 50 μm and 20 μm respectively. Then we generated many models with different V_Ts by parallel shift of the original model.

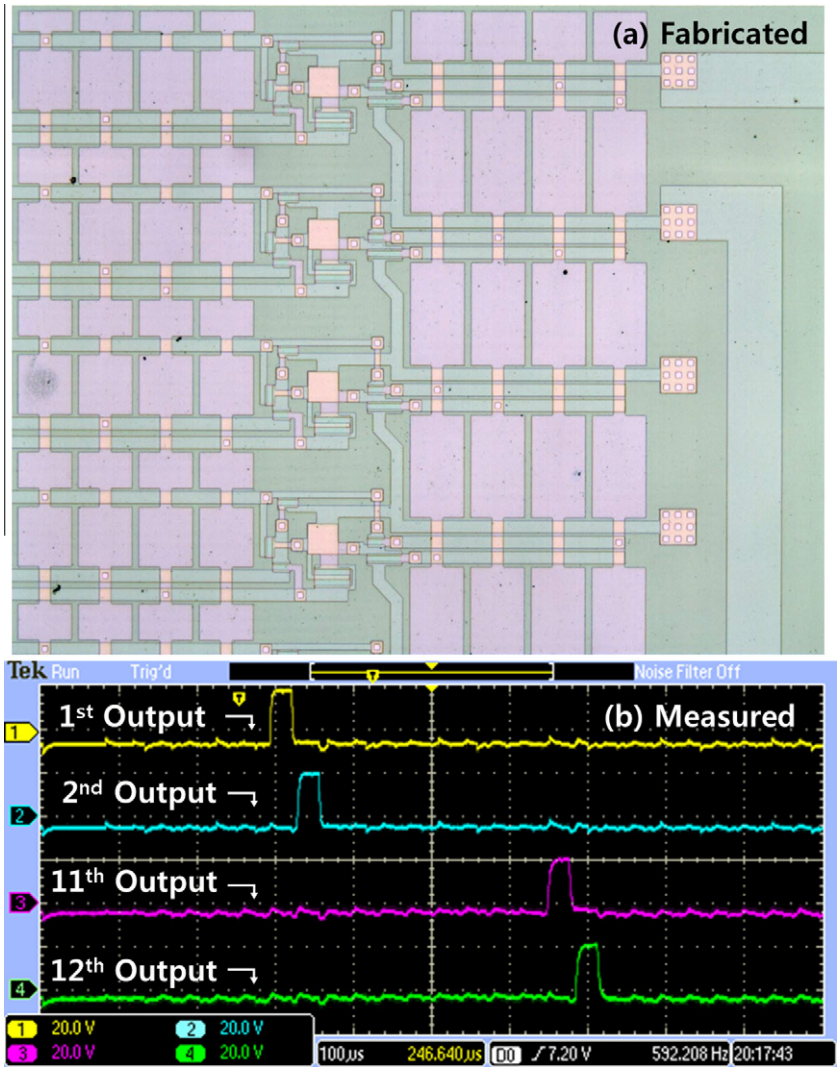

Fig. 4. (a) First 4 stages of fabricated shift register. (b) Measured output waveforms of fabricated shift register with 12 stages.

We assumed a VGA (640 × 480) resolution AMLCD panel with the frame rate of 60 Hz and used the new shift register circuit as a gate driver. In order to emulate the gate line load, 5 kΩ resistor and 50 pF capacitor were attached to each output node. The channel widths of M1–M6 are 150 μm, 40 μm, 200 μm, 50 μm, 40 μm, and 50 μm respectively and the channel lengths are all 20 μm. The capacitance of C_b is 4 pF. The frequency of CK_A/B is 14.4 kHz and that of CK1 ~ 4 is 7.2 kHz since the frame rate is 60 Hz and the number of gate lines is 480. Fig. 3a–e shows the simulated voltage waveforms in the load capacitances of the first nine stages. When V_Ts of the TFTs are all −6 V, only the first two stages generate small pulses (Fig. 3a). As the V_Ts of the TFTs are increased to −5 V, the circuit operates properly. In this case, small fluctuations of the output nodes are observed because M3 is slightly turned on (Fig. 3b). For $V_T = 0$ V, the circuit exhibits ideal operation (Fig. 3c). As V_T increases to around 9 V, it is difficult to charge the load capacitance (Fig. 3d). Accordingly the circuit does not work for $V_T = 10$ V (Fig. 3e).

Fig. 3f shows simulated power consumption of the new shift register with 480 stages. The power consumption is similar to that of the conventional shift register when V_T is positive. However it increases considerably as V_T shifts negatively because the currents through M3 and M6 gradually increase when CLK_A is high and the output is low. It is desirable to reduce the power consumption for future development.

Fig. 4a is the microscope photograph of the fabricated shift register. Only first four stages are shown. We adopted the staggered top-gate TFT structure that has the source/drain electrodes beneath the active layer. Fig. 4b shows the measured output waveforms of the fabricated shift register with 12 stages. The TFTs were made of IGZO active layer and Al_2O_3 gate insulator on a glass substrate. V_Ts of the TFTs around the circuit ranged from −5 V to −3 V. It is clearly shown that the output waveforms swing from −5 V to +20 V as expected. This indicates that the new shift register works successfully with the depletion-mode oxide TFTs. The power consumption of the fabricated circuit with 12 stages ranged from 200 mW to 300 mW.

4. Conclusion

The simplest shift register circuit compatible with the metal-oxide TFT having negative V_T has been developed. The shift register is composed of only six TFTs and employs two different voltage levels, i.e. −5 V and −10 V for the clock signals. This makes two important switch TFTs turned off completely even though they

have negative V_Ts. The SmartSpice simulation results show that the shift register works successfully over wide V_T range of −5–+9 V. And the fabrication result indicates that the new circuit works stably with the depletion-mode oxide TFTs.

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