Applied Physics Letters

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Cite as: Appl. Phys. Lett. **95**, 173508 (2009); https://doi.org/10.1063/1.3257726
Submitted: 15 August 2009 . Accepted: 10 October 2009 . Published Online: 29 October 2009

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Impact of Sn/Zn ratio on the gate bias and temperature-induced instability of Zn-In-Sn-O thin film transistors

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(Received 15 August 2009; accepted 10 October 2009; published online 29 October 2009)

We investigated the effect of the Sn/Zn ratio in the amorphous Zn-In-Sn-O (ZITO) system on the gate voltage stress-induced stability of the resulting thin film transistors (TFTs). The device stability of the TFTs with a composition channel of Zn:In:Sn=0.35:0.20:0.45 (device C) was dramatically improved, while those of the devices with Zn:In:Sn=0.45:0.20:0.35 and 0.40:0.20:0.40 suffered from deep level trap creation in the channel and charge trapping, respectively. The stability enhancement of device C can be attributed to its having the lowest total trap density, which was corroborated by the superior temperature stability of the subthreshold current region in the temperature range from 298 to 398 K. Therefore, the Sn atoms are believed to act as a stabilizer of the amorphous ZITO network, which is similar to the role of Ga in the In-Ga-Zn-O system. © *2009 American Institute of Physics*. [doi:10.1063/1.3257726]

Zn-based oxide semiconductors have attracted a tremendous amount of attention as the active channel material of emerging electronic devices including the thin film transistors (TFTs) backplanes for flexible displays or transparent active matrix organic light-emitting diode displays, because they offer high performance parameters, such as a high mobility, low gate subthreshold swing, and excellent uniformity as well as the advantages of good transparency to visible light and low temperature process capability compared with amorphous Si and polycrystalline Si TFTs.[1–6]

However, the instability of the threshold voltage (V_{th}) of Zn-based oxide TFTs under gate voltage stress is one of the most crucial problems remaining to be resolved before oxide TFTs can be integrated into commercial electronic products. Several groups attributed the positive V_{th} shift under positive gate voltage stress (PGVS) for oxide TFTs to charge trapping at or near the Zn-based oxide channel and gate dielectric, based on the amorphous silicon framework.[7–10] It should be noted, however, that almost all of the devices that were studied were bottom gate oxide TFTs in which the channel layer was directly exposed to the ambient atmosphere (i.e., unpassivated devices). Because the electrical properties of ZnO and SnO_2 semiconductors are extremely affected by the presence of an ambient atmosphere (oxygen, water, and hydrogen), the interaction between these channel layer and ambient molecules cannot be neglected during the stability evaluation of oxide TFTs.[11–14] Indeed, one of the authors recently asserted that the V_{th} instability of oxide TFTs under gate voltage stress comes from the gate-field-induced molecular adsorption/desorption of oxygen, hydrogen, or water on the back channel surface, rather than the aforementioned charge trapping phenomena.[15] This complexity of the oxide TFT system have prevented unambiguous and in-depth studies from being conducted to determine the exact relationship between the channel material properties (channel composition, and film density) and the resulting transistor instability.

In this letter, we chose the bottom gate and bottom contact device configuration, in which a 20-nm-thick Al_2O_3 protection layer and 20-nm-thick Al_2O_3 passivation layer deposited by atomic layer deposition (ALD) were formed on the Zn-In-Sn-O (ZITO) semiconductor film. Al_2O_3 thin film was used as a passivation layer, because ALD-derived Al_2O_3 layers are known to act as an efficient diffusion barrier against the penetration of oxygen or water.[16–18] Therefore, the gate voltage stress-dependent device instabilities can be attributed to the charge trapping or the channel degradation rather than the ambient-related deterioration, which renders the interpretation of the device instability mechanism more obvious. It was found that the Sn/Zn ratio greatly affected not only the device performance but also the dc and temperature instability of the ZITO transistors. The extremely low trap density of the devices, including the interfacial trap density and semiconductor bulk trap density is closely related to their excellent dc and temperature stability.

Lithographically patterned ITO (150nm) on an alkali free-glass (E2000, Samsung Corning Inc.) substrate with a surface area of 100×100 mm^2 was used as the gate electrode for the bottom gate TFT. Al_2O_3 (185nm) film as a gate dielectric was deposited by ALD at 150 °C. The ITO electrode used as a source/drain electrode was deposited by the conventional sputtering method and then patterned using photolithography and wet etching. The a-ZITO film with a thickness of 25nm was grown by the cosputtering of ZnO, SnO_2, and ITO (In_2O_3, 90 wt %) targets. A schematic diagram of the target-substrate arrangement in the cosputtering system is shown in Fig. 1(a). Then, the 20-nm-thick Al_2O_3 film as a protection layer was deposited by plasma enhanced ALD at 150 °C. After patterning the active channel and protection layer using photolithograph and subsequent wet etching, a second Al_2O_3 (20 nm) film was formed as a passivation layer by ALD at 150 °C. Finally, the fabricated devices were subjected to thermal annealing at 300 °C for 2 hrs under an O_2 atmosphere. A schematic cross-section of the fab-

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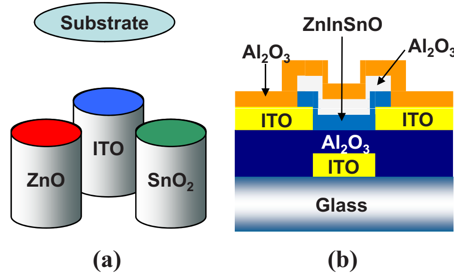

FIG. 1. (Color online) (a) Schematic diagram of the target-substrate arrangement in the cosputtering system. (b) Schematic cross-section of the fabricated ZITO TFTs with a bottom gate and bottom contact structure ($W/L=40/20$ μm).

ricated ZITO TFTs is depicted in Fig. 1(b). The IV characteristics of the ZITO devices were measured at various temperatures ranging from 298 to 398 K with an Agilent 4156C precision semiconductor parameter analyzer.

In the ternary system of ZnO-In_2O_3-SnO_2, the In_2O_3 fraction is the most significant component determining the field-effect mobility. However, a higher In content results in the deterioration of the threshold voltage.[19] Thus, the indium composition was fixed at an atomic ratio of $In/(Zn+In+Sn)$ of 0.20. Sn and Zn compositions of 0.35 and 0.45 (device A), 0.40 and 0.40 (device B), and 0.45 and 0.35 (device C) were employed, respectively. The field-effect mobilities (μ_{FE}) for devices A (24.1 cm^2/V s) and B (24.6 cm^2/V s) were comparable to each other while the subthreshold gate swing (SS, 0.23 V/decade) of device B was better that (0.15 V/decade) of device A. On the other hand, device C exhibited a slightly reduced μ_{FE} (15.1 cm^2/V s) and the best SS value of 0.11 V/decade. However, it should be noted that these device parameters correspond to the state-of-the-art characteristics for any Zn-based oxide TFT. Figures 2(a)–2(c) show the evolution of the transfer curves as a function of the applied stress time for devices A, B, and C, respectively. The devices were stressed

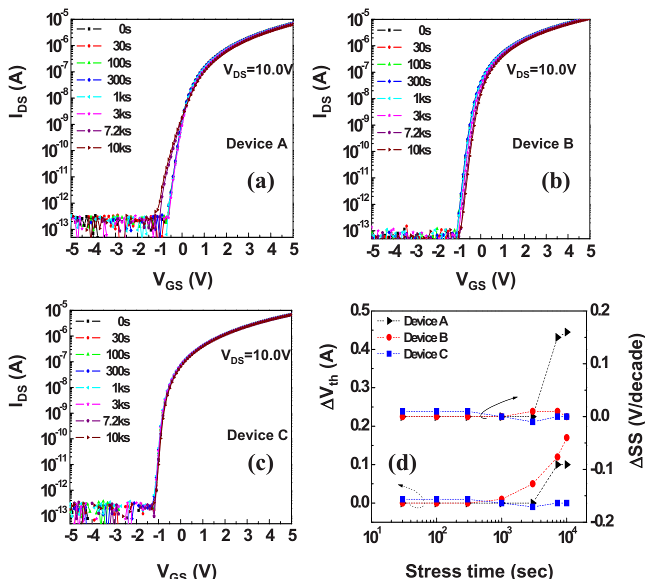

FIG. 2. (Color online) The evolution of the transfer curves for devices (a) A, (b) B, and (c) C with a top gate and bottom contact structure ($W/L=40/20$ μm). (d) The variations in the ΔV_{th} shift and ΔSS value for devices A, B, and C.

under the following conditions: the V_{GS} was set to 10.0 V and V_{DS} was fixed at 0 V. The maximum stress duration was 10 000 sec. It can be seen that while device A shows a significant deterioration in its S value as well as a positive V_{th} shift ($\sim$0.1 V) with increasing stress time, device B did not suffer from any change of the S value and exhibited only a parallel positive V_{th} shift as shown in Fig. 2(d). The increase ($\Delta SS=0.16$ V/decade) in the subthreshold swing for device A after a PGVS of 10^4 sec can be attributed to the creation of deep-level defects ($\sim 6.3\times 10^{11}/cm^2$) in the ZITO channel layer during the application of the gate voltage stress.[20] In contrast, device B exhibited typical behavior i.e., a positive V_{th} shift ($\sim$0.17 V) after a the PVGS of 10^4 sec, indicating that charge trapping occurred at the interface between the ZITO channel and Al_2O_3 gate dielectric. It is noted that the fast recovery of the V_{th} value occurred without any thermal annealing after one day indicating that the activation energy for detrapping at the charge trapping site injection is comparable to or less than the thermal energy (approximately 0.025 eV) at room temperature. Thus, we excluded the possibility of charge injection into the Al_2O_3 dielectric layer. Finally, device C showed excellent stability against the gate voltage stress. There was no degradation of the μ_{FE} and SS values, nor any shift in the V_{th} value during application of the PGVS for 10^4 sec. The absence of charge trapping after the PGVS might be related to the fact that the interfacial traps density (N_{it}) of device C is lower than those of devices A and B. The maximum N_{it} value can be estimated from the SS value $[N_{it}=[SS\log(e)/(kT/q)-1]C_i/q$,[19] where C_i is the gate capacitance per unit area, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary electron charge], which assumes that there is no semiconductor bulk trap (N_{ss}) in the ZITO thin film. The $N_{it,max}$ value ($2.1\times 10^{11}/cm^2$) for device C was much smaller than those ($7.8\times 10^{11}/cm^2$, $6.7\times 10^{11}/cm^2$) for devices A and B. This lower N_{it} might constitute the reason why no V_{th} shift caused by charge trapping was observed for device C. Now it is obvious that the ratio of Sn/Zn is critical to the effect of charge trapping and/or trap creation including N_{ss} and D_{it} after the PGVS. The absence of any shift in V_{th} under PGVS for devices C would suggest the ruling out of charge injection into the Al_2O_3 gate dielectric layer as the origin of the positive V_{th} shift of device B. It should be noted that the V_{th} shift for the unpassivated device with the same channel composition of device C was more than 1.0V under the identical PGVS condition (data not shown), indicating that the passivation is indeed crucial to prevent the effect of ambient effect. Furthermore, the fact that increasing the Sn content from 35% to 45% significantly improved the dc stability of the resulting ZITO transistors with the bottom gate structure suggests that the role of the Sn ion may be that of a stabilizer of the amorphous ZITO network and an annihilator of the overall trap sites including N_{it} and N_{ss}.

Figures 3(a) and 3(b) show the evolution of the transfer curves as a function of the measurement temperature for devices A and C, respectively. It can be seen that V_{th} is negatively shifted with increasing temperature for both devices. Though the V_{th} value for device A was shifted by approximately 0.4 V from 0.2 to -0.2 V, the negative V_{th} shift in device C after increasing the measurement temperature from 298 to 398 K was relatively small ($\sim$0.2 V). This negative V_{th} shift with increasing temperature can be explained by the

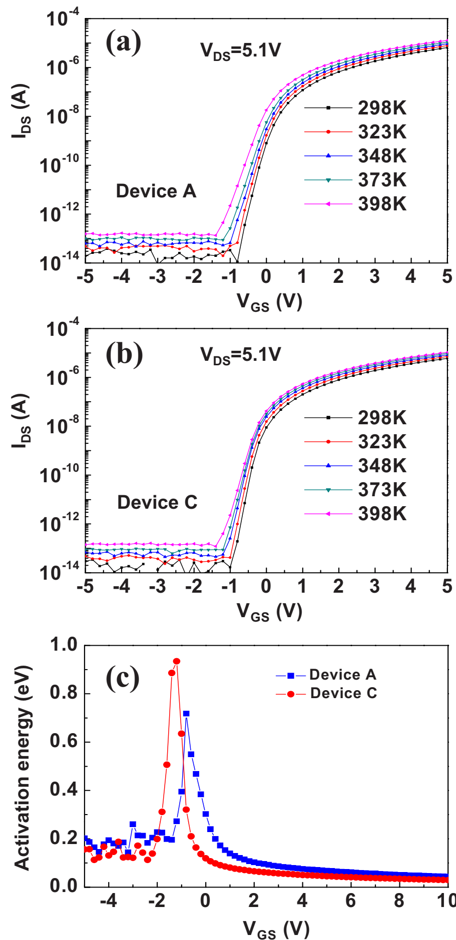

FIG. 3. (Color online) The evolution of the transfer curves as a function of the measurement temperature for devices (a) A and (b) C. (c) Variations of the activation energy (E_A) of the I_{DS} vs V_{GS} for devices A and C.

thermal activation process of the subthreshold drain current. The conductance activation energy (E_A) can be calculated as a function of V_{GS} in the forbidden bandgap from the fitting of the temperature-dependent log(I_{DS}) versus 1/T curve, where $E_A=E_C-E_F$ assuming Boltzmann statistics.[21,22] Figure 3(c) shows $E_A(=E_C-E_F)$ as a function of V_{GS} for devices A and C. The maximum E_A value (0.72 eV) for devices A was observed at a V_{GS} of −0.8 V and gradually decreased to 0.2 eV at a V_{GS} of 0.4 V. In contrast, the highest energy barrier for device C was approximately 0.93 eV at a V_{GS} of −1.2 V and E_A rapidly decreased to 0.2 eV at a V_{GS} of −0.6 V. The falling rate of E_A with respect to V_{GS} in the subthreshold current region should have the same magnitude as the rising rate of E_F. In the case of a TFT having a significantly large trap density (N_{total}) including N_{SS} and N_{it}, the rate of change of E_F with respect to V_{GS} ($\partial E_F/\partial V_{GS}$) is roughly inversely proportional to the magnitude of N_{total}, because all of trap sites below E_F must be fulfilled with electron before a move to the E_F level in the forbidden bandgap region become possible. Thus, the much faster falling rate ($|\Delta E_F/\Delta V_{GS}|\sim 1.2$ eV/V) of E_A in device C compared to that ($|\Delta E_F/\Delta V_{GS}|\sim 0.43$ eV/V) of device A, means that the N_{total} value is reduced by approximately 3 times compared to that of device A. This speculation is quite consistent with the aforementioned $N_{it,max}$ values, which were calculated from the SS values. Therefore, the better temperature stability as well as dc stability for device C can be attributed to the much reduced N_{total} at the channel/gate dielectric interface and ZITO bulk film.

In summary, the effect of the Sn/Zn ratio in amorphous ZITO semiconductors on the device stability of the resulting TFTs was investigated. With increasing Sn/Zn ratio from 0.35/0.45 to 0.45/0.35, the μ_{FE} and SS values of the ZITO TFT were slightly decreased and dramatically improved, respectively. The dc stability was highly dependent on the cation composition: the optimized Sn/Zn ratio of 0.45/0.35 resulted in the excellent temperature stability as well as dc stability of the ZITO TFTs. Therefore, it was concluded that the ZITO semiconductor system can be a promising candidate for TFTs with excellent stability as well as high performance, thereby replacing the commercially available amorphous Si and polycrystalline Si TFTs.

This work was supported by the IT R&D program of the Ministry of Knowledge Economy (Grant No. 2006-S079-04, smart window with transparent electronic devices). J.K.J. acknowledges the support from Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (Grant No. 2009-0087297).

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