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Effect of the Electrode Materials on the Drain-Bias Stress Instabilities of In−Ga−Zn−O Thin-Film Transistors

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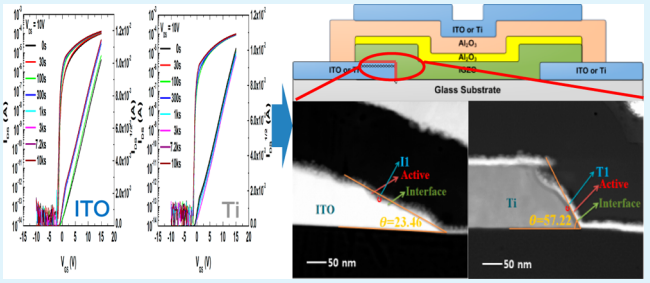
ABSTRACT: The effects of electrode materials on the device stabilities of In−Ga−Zn−O (IGZO) thin-film transistors (TFTs) were investigated under gate- and/or drain-bias stress conditions. The fabricated IGZO TFTs with a top-gate bottom-contact structure exhibited very similar transfer characteristics between the devices using indium−tin oxide (ITO) and titanium electrodes. Typical values of the mobility and threshold voltage of each device were obtained as 13.4 cm^2 V^{-1} s^{-1} and 0.72 V (ITO device) and 13.8 cm^2 V^{-1} s^{-1} and 0.66 V (titanium device). Even though the stabilities examined under negative and positive gate-bias stresses showed no degradation for both devices, the instabilities caused by the drain-bias stress were significantly dependent on the types of electrode materials. The negative shifts of the threshold voltage for the ITO and titanium devices after the 10^4-s-long drain-bias stress were estimated as 2.06 and 0.96 V, respectively. Superior characteristics of the device using titanium electrodes after a higher temperature annealing process were suggested to originate from the formation of a self-limiting barrier layer at interfaces by nanoscale observations using transmission electron microscopy.



KEYWORDS: *oxide semiconductor, thin-film transistor, device reliability, bias stress, electrode, In−Ga−Zn−O*

1. INTRODUCTION

Oxide semiconductors such as In−Ga−Zn−O (IGZO) have actively been researched and developed because of their promising characteristics such as a high mobility, a low-temperature process compatibility, and a uniform device performance for use in the backplanes of flat-panel displays.[1−4] For these oxide thin-film transistors (TFTs), it is increasingly important to guarantee the device reliabilities, and numerous related studies have been performed under various test conditions such as adsorption and desorption of water/oxygen molecules,[5,6] the annealing temperature effect,[7] gate-bias stress tests,[8] and the light illumination effect.[9−12] Because these characteristics of the oxide TFTs are very complicated and are affected by multiple origins, physical descriptions are still controversial and sometimes very tricky. On the other hand, drain-bias-induced stress tests have not been so widely investigated,[13,14] in spite of their critical effects on the long-time stability of TFT characteristics. According to some reports on poly-Si TFTs,[15−18] the devices have experienced alteration of the off-current and collapse of the on-current under drain-bias conditions because of the creation of defects. The contact between source−drain (S/D) regions and the oxide channel layer can be regarded as a kind of metal−semiconductor junction. Therefore, Schottky or ohmic behaviors at the contact interface[19] may have a great impact not only on the static device characteristics but also on the long-time stabilities. While the gate electrode and active channel layer are physically separated by the gate insulator, the drain electrode directly encounters the active layer. This direct contact always is exposed to the possibility of physical or chemical degradation at the interface by some external stresses like an applied electric field and/or light illumination. In other words, the device stability characteristics of the oxide TFTs under drain-bias stress conditions would be supposed to be critically affected by the type of drain electrode employed. However, any intensive study on the relationship between the electrode materials and the drain-bias stress under a strong electric field has rarely been reported so far. It would be very interesting to investigate the effects of material variations for the drain electrode.

In this study, we have fabricated IGZO TFTs using indium−tin oxide (ITO) and titanium as S/D electrodes. ITO electrodes have been intensively employed as some of the most well-known transparent electrodes.[20,21] Titanium electrodes have also been used as some of the typical metal electrodes

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suitable for fabrication of the oxide TFTs.[22,23] In order to elucidate the degradation mechanism under the drain-bias stress conditions, the transfer characteristics of two fabricated devices were compared and nanoscale observations of the interface regions in the vicinity of drain electrodes were conducted by means of transmission electron microscopy (TEM). Visual evidence provided interesting and important insights for understanding the influences of electrode materials on the device reliabilities.

2. EXPERIMENTAL SECTION

Two types of IGZO TFTs with a top-gate bottom-contact structure were fabricated using ITO (termed the ITO device) and titanium (termed the Ti device) as S/D and gate-electrode materials, as shown in Figure 1. In order to focus the bias stability on the S/D electrode

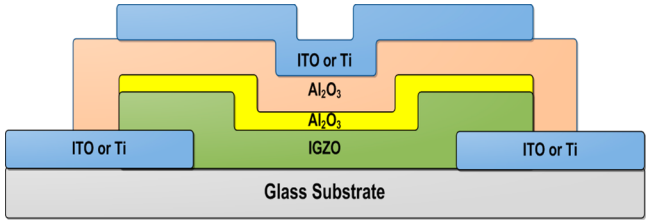

Figure 1. Schematic diagram of the top-gate bottom-contact structured IGZO TFT using an ITO or Ti electrode. The thickness of the IGZO active channel was deposited as 20 nm. Gate insulators were composed of a first protection layer of 9-nm-thick Al_2O_3 and a second main layer of 176-nm-thick Al_2O_3, which were prepared in a two-step process performed before and after patterning of the IGZO channel layer. The ITO and Ti layers for S/D and gate electrodes were prepared as 150 and 200 nm in thickness, respectively.

materials without an additional passivation process and interface damages between the gate insulator and channel layer during the plasma-induced deposition process, we employed the top-gate devices. The 200-nm-thick Ti or 150-nm-thick ITO thin film was prepared using a direct-current (dc) sputtering method as S/D electrodes at room temperature. The sheet resistivities measured by a four-point prove method were 6 and 10 Ω/□, respectively. Then, as an active layer, a 20-nm-thick IGZO (In:Ga:Zn = 1:1:1 atomic ratio) film was deposited by a radio-frequency sputtering method in an atmosphere of an Ar and O_2 gas mixture at room temperature. To prevent any chemical damage during the patterning process, 9-nm-thick Al_2O_3 was formed at 200 °C by the atomic layer deposition (ALD) method. This process is one of the important features of our devices that have been reported so far.[24] 150-nm-thick Al_2O_3 was formed at 150 °C by ALD as a gate insulator. The Ti or ITO electrode was deposited by the dc sputtering method and patterned as a gate electrode by the wet-chemical-etching process. Especially, during the patterning process of Ti electrodes, an etchant composition and etch time/temperature conditions should be carefully controlled, which were found to be very important to obtain the reproducibility in TFT characteristics among the devices. The final annealing process for the fabricated IGZO TFTs was conducted at 200 °C in vacuum for 2 h. All electrical characteristics were measured using a semiconductor parameter analyzer (Agilent B1500A) in a dark box at room temperature. The channel width and length of evaluated devices were defined as 40 and 20 μm, respectively. Cross-sectional nanoscale microstructures of the channel region in the vicinity of drain electrodes were observed using TEM (FEI TecnaiG^2 F30 S-Twin) at an accelerating voltage of 300 kV. The compositions of each layer were investigated using a scanning TEM (STEM)-high angular annular dark-field (HAADF) mode and energy-dispersive X-ray spectroscopy (EDS). The TEM samples were prepared using a dual-beam focused ion beam (DB-FIB; FEI, Nova200) in TEM sample preparation mode.

3. RESULTS AND DISCUSSION

For the first step, the basic characteristics of the fabricated ITO and Ti devices were examined. Parts a and b of Figure 2 show

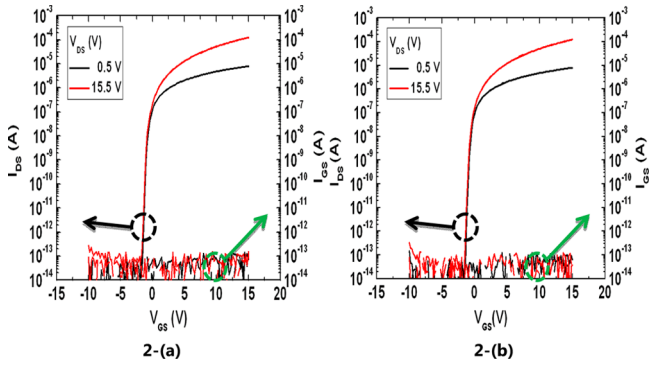

Figure 2. I_{DG}–V_{GS} transfer characteristics of the fabricated IGZO TFTs using (a) ITO (ITO device) and (b) Ti (Ti device) electrodes. The measurements were performed in the forward and reverse directions of V_{GS} at V_{DS}'s of 0.5 and 15.5 V. The channel width and length of measured devices were 40 and 20 μm, respectively. The final annealing temperature was 200 °C. The values of μ_{sat}, V_{TH}, and SS for the ITO and Ti devices were obtained as 13.4 cm^2 V^{-1} s^{-1}, 0.72 V, and 134 mV decade^{-1} and 13.8 cm^2 V^{-1} s^{-1}, 0.66 V, and 141 mV decade^{-1}, respectively.

the drain current (I_{DS})–gate voltage (V_{GS}) transfer curves of the ITO and Ti devices, respectively. The electrical device parameters of the field-effect mobility at the saturation region (μ_{sat}), threshold voltage (V_{TH}), and subthreshold swing (SS) were calculated as 13.4 cm^2 V^{-1} s^{-1}, 0.72 V, and 134 mV decade^{-1} (ITO device) and 13.8 cm^2 V^{-1} s^{-1}, 0.66 V, and 141 mV decade^{-1} (Ti device), respectively. It was confirmed that there were no noticeable differences in the basic transfer characteristics between two devices.

Next, we evaluated the transfer characteristics of two devices under the gate-bias stress conditions, in which V_{GS} of −20 or +20 V was continuously applied to the gate terminal for 10^4 s. Under positive stress conditions, the estimated values of μ_{sat}, V_{TH}, and SS of the ITO device showed changes from 10.9 to 10.6 cm^2 V^{-1} s^{-1}, from −0.14 to −0.45 V, and from 151 to 153 mV decade^{-1}, respectively, between before and after the stress time, as shown in Figure 3a. On the other hand, for the Ti device, these parameters showed changes from 10.9 to 10.5 cm^2 V^{-1} s^{-1}, from −0.16 to −0.46 V, and from 165 to 158 mV decade^{-1}, respectively, as shown in Figure 3c. Although V_{TH}'s were observed to experience a negative shift of approximately 0.3 V for both devices, the device characteristics did not exhibit some severe degradation. Furthermore, the noticeable differences in changing the transfer properties were not recognized between the two devices. Parts b and d of Figure 3 show variations in the transfer characteristics for ITO and Ti devices under negative stress conditions, respectively. Compared with the data obtained in Figure 2a,b, the μ_{sat} and SS values did not show any significant changes for both devices. The estimated values of μ_{sat} and SS for the ITO and Ti devices were observed to vary from 10.8 to 10.7 cm^2 V^{-1} s^{-1} and from 165 to 158 mV decade^{-1} and from 10.7 to 10.7 cm^2 V^{-1} s^{-1} and from 160 to 152 mV decade^{-1}, respectively. Similar to the positive gate-bias stress situations, small variations in V_{TH} in the negative direction were detected. However, the degree of variations was smaller than that under the positive stress conditions, which

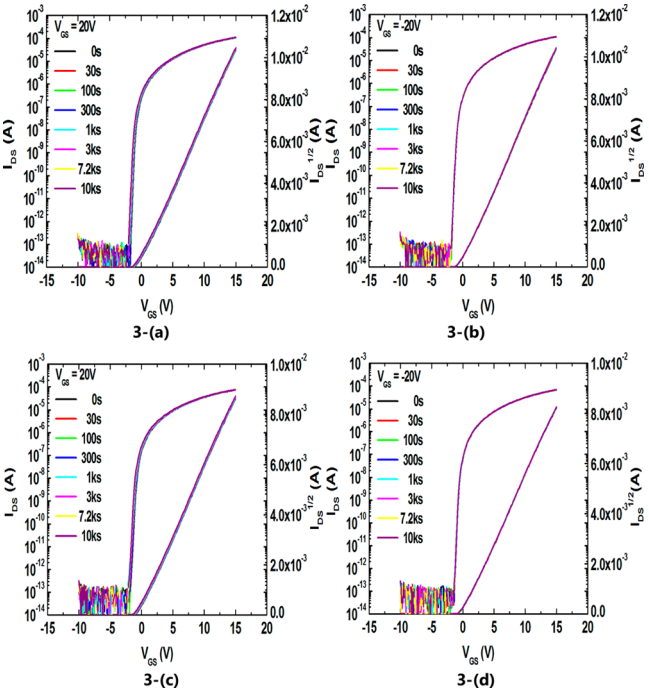

Figure 3. Variation in the $I_{DG}-V_{GS}$ transfer characteristics for the ITO and Ti devices as a function of the stressed time for 10^4 s under gate-bias stress conditions. Sets of transfer curves for the ITO device at the applied V_{GS} of (a) +20 and (b) −20 V and for the Ti device at the applied V_{GS} of (c) +20 and (d) −20 V. V_{DS} of 10 V was applied for the measurements. Negative shifts in V_{TH} for both devices were estimated as 0.30 and 0.14 V after the positive or negative gate-bias stress, respectively.

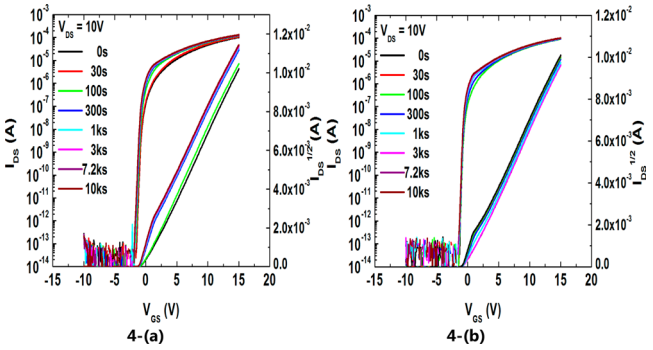

Figure 4. Variation in the $I_{DG}-V_{GS}$ transfer characteristics for the (a) ITO and (b) Ti devices as a function of the stressed time for 10^4 s under a drain-bias stress of 20 V. V_{DS} of 10 V was applied for the measurements. Negative shifts in V_{TH} for the ITO and Ti devices were estimated as 2.06 and 0.96 V after the positive drain-bias stress, respectively.

was estimated to be approximately 0.14 V. There were no marked differences between both devices. This tendency of the amounts of V_{TH} shifting under negative gate-bias stress was smaller than that under positive gate-bias stress has been frequently introduced for the well-fabricated IGZO TFTs.[25] As can be seen in the figure, it can be suggested that the device reliabilities obtained under gate-bias stress conditions were very excellent even when the gate and S/D electrodes were modulated to ITO and Ti devices. We believe that a dense Al_2O_3 gate insulator and an initial protection layer of thinner Al_2O_3 prepared in this work could be effective prescriptions to enhance the gate-bias stability for the top-gate IGZO TFTs. Consequently, it can be concluded from these results that the device reliabilities under gate-bias stress tests are not so sensitive to the material types of the gate and S/D electrodes but mainly dependent on the process designed for the gate insulator. In other words, with only tests under gate-bias stress, we cannot recognize awesome effects of the electrode material on the stability characteristics of IGZO TFTs.

From these viewpoints, the device operations were characterized under drain-bias stress conditions. Parts a and b of Figure 4 show the transfer characteristics of ITO and Ti devices when a drain voltage (V_{DS}) of 20 V was continuously applied to the drain terminal for 10^4 s. Unlike the cases of gate-bias stress tests, remarkable changes in the characteristics were observed between the ITO and Ti devices. While the values of μ_{sat}, V_{TH}, and SS for the Ti device were obtained as varying from 9.5 to 9.2 $cm^2\ V^{-1}\ s^{-1}$, from −0.02 to −0.98 V, and from 115 to 121 mV $decade^{-1}$ between before and after the drain-bias stress, for the ITO device, the same parameters were changed from 10.2 to 10.5 $cm^2\ V^{-1}\ s^{-1}$, from −0.18 to −2.24 V, and from 148 to 154 mV $decade^{-1}$. The most marked difference between the two devices was the degree of negative shift in V_{TH} after drain-bias stress tests, even though the obtained overall characteristics were not so critically degraded. As a glance at Figure 4a, the on-state drain current of the ITO device showed an increasing trend with a lapse of stress time owing to the relatively large negative shift in V_{TH}, compared with the Ti device. In other words, the V_{TH} shift of the ITO device (ΔV_{TH} = −2.06 V) was much higher than that of the Ti device (ΔV_{TH} = −0.96 V). One more noticeable point is that the on-state drain current approached the saturation level with a steeper slope as a function of V_{GS} with increasing stress time. This result reveals that the field-effect mobility of the device becomes more strongly dependent on the applied gate voltage. These phenomena might be closely related to some composition changes in the active channel layer and/or in the interface regions between the drain electrode and active layer. A feasible scenario can be explained as follows: (1) During the active layer deposition, some plasma damage can be induced between the S/D electrodes and the active layer. (2) Considerably large drain bias applied for a long time might cause interdiffusion of the constituent elements by highly energetic electrons at the interface near the drain side damaged during step 1. (3) As a consequence of the drain-bias-induced interdiffusion, some compositional changes may occur at the interface near the drain side. It happens that the increase in the carrier concentration contributing to the channel conductance locally occurs at specified regions. These localized conductive regions influence the V_{TH} shift by the percolation effect. As a result, the Ti device was confirmed to be more robust than the ITO device under strong drain-bias stress conditions. All electrical parameters of measured devices are summarized in Table 1.

These interesting discussions can be visualized by means of TEM observations, in which the nanoscale cross sections of the interfaces between the drain electrodes and IGZO channel layers of ITO and Ti devices were observed. The electrical characteristics of the ITO and Ti devices were repeatedly evaluated before TEM observations to confirm the typical device characteristics under the drain-bias stress situations. Parts a and b of Figure 5 show the bright images of TEM and STEM-EDS mapping of the ITO device, respectively, which was a fresh device prepared prior to the drain-bias stress test. As

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Table 1. Comparisons of the Device Parameters for the ITO and Ti Devices Experienced Given Bias Conditions to Those of Their Initial Values before the Bias-Stress Tests[a]

device	kind of stress	anneal temp (°C)	stress status	μ_{sat} (cm^2 V^{-1} s^{-1})	V_{TH} (V)	SS (mV $decade^{-1}$)
Ti	no stress	200		13.8	0.66	141
	positive gate-bias stress (V_{GS} = 20 V)	200	before	10.9	−0.16	165
			after	10.5	−0.46	158
	negative gate-bias stress (V_{GS} = −20 V)	200	before	10.7	−0.14	160
			after	10.7	−0.28	152
	drain-bias stress (V_{DS} = 20 V)	200	before	9.5	−0.02	115
			after	9.2	−0.98	121
	drain-bias stress (V_{DS} = 20 V)	250	before	9.1	0.25	143
			after	9.2	0.29	142
ITO	no stress	200		13.4	0.72	134
	positive gate-bias stress (V_{GS} = 20 V)	200	before	10.9	−0.14	151
			after	10.6	−0.45	153
	negative gate-bias stress (V_{GS} = −20 V)	200	before	10.8	−0.11	165
			after	10.7	−0.25	158
	drain-bias stress (V_{DS} = 20 V)	200	before	10.2	−0.18	148
			after	10.5	−2.24	154

[a]For these evaluations, the positive/negative gate-bias or positive drain-bias conditions were applied for 10^4 s. The Ti device annealed at 250 °C was also evaluated as a controlled device to confirm the effect of the postannealing temperature.

can be seen in the figure, the device was confirmed to be well fabricated, in which each comprising layer was clearly defined as designed and processed (Figure 5a) and corresponding compositions were also well identified (Figure 5b). Although it is hard to evidently define the interface between the ITO and IGZO because of the common component of indium in the two layers, it was found that any mechanical collapse and/or terrible compositional interdiffusion were not detected. The main interest is to compare the differences at corresponding interfaces between the ITO and Ti devices experiencing the high-field drain-bias stresses. Parts c and d of Figure 5 show the STEM-HAADF images with the same magnifications of the interface regions for both devices, respectively. It is very interesting to note that the situations at the interfaces were completely different between the two devices. For the case of the stressed ITO device, the interface was severely degraded and mingled each other. The thickness of the deteriorated region amounts a few tens of nanometers. Thus, we cannot identify the layers of ITO and IGZO at the interface region. EDS was used to analyze the composition of the point (indexed as I1), which can be regarded as an intermediate region of the interface, as shown in Figure 5e. All elements of In, Ga, Zn, and Sn were simultaneously detected at the point I1. It is suggested that this nanoscale degradation at the interface was caused by the continuous electrical stress of drain bias and resulted in the undesirable stress-time-dependent variations of the device characteristics described in Figure 4a.

In contrast, for the case of the Ti device, clear interfaces were identified even after the drain-bias stress tests, as shown in the HAADF images of Figure 5d. The most important feature was formation of the transition layer at interfaces, which was imaged with darker contrast than the bulk region of the Ti electrode. It can be expected that the composition of this transition layer would be different from those of the Ti and IGZO regions. The EDS spectra measured at the transition layer (indexed as T1) showed that some interdiffusion occurred between the Ti and IGZO regions, as shown in Figure 5f, in which the elements of Ti, In, Ga, and Zn were simultaneously detected. Although it was found that the interfacial transition region was formed by ionic migration owing to the externally applied electrical stress of drain bias, it was highly inspiring that the formation of a compositionally modified transition layer could prevent limitless interdiffuion events across the interface and protect its sound behavior. In other words, we believe that this transition layer could be worked as a barrier layer against additional interdiffusion with a lapse of stress time. This difference from the case of the ITO device was reflected in the stable device characteristics shown in Figure 4b. The self-limiting action of the Ti electrode interfaced with the IGZO active channel is worth emphasizing, considering that the tapered angle of the patterned Ti electrode was larger than that of the patterned ITO electrode. As shown in Figure 5c,d, the angles of the tapered ITO and Ti electrode patterns were measured as 24.46 and 57.22°, respectively. The different angles of the tapered patterns for the ITO and Ti electrodes originated from the attributes of each electrode under wet-etching conditions. It can be said that the geometry of the interface for the Ti device is more vulnerable to the high field of drain bias because a higher electric field will be applied and concentrated at the local region having a larger tapered angle with a larger curvature. Actually, the contrast of the bottom-side transition layer was observed to be darker than that of the top-side layer, as shown in Figure 5d. On the other hand, the ITO device was revealed to be very prone to the high-field drain-bias stress, irrespective of a lower tapered angle at the interface. From these results and discussion, it suggests that the pattern shapes of the S/D electrodes can also play an important role in diminishing the concentrated electric field during drain-bias stress conditions. Consequently, we can expect that modification of the pattern shape and its tapered angle for the Ti device can enhance the device reliability under drain-bias stress conditions. From these TEM views and EDS spectra, it can be concluded that the device stabilities under drain-bias stress conditions are well explained by completely different situations of the interfaces between the two devices. The formation of a self-limiting transition layer at the interface for the Ti device is a new finding for understanding the device physics of IGZO TFTs.

In order to further investigate the action of the transition layer for the Ti device and its relationship with the electrical behavior of the device, a controlled device was prepared by

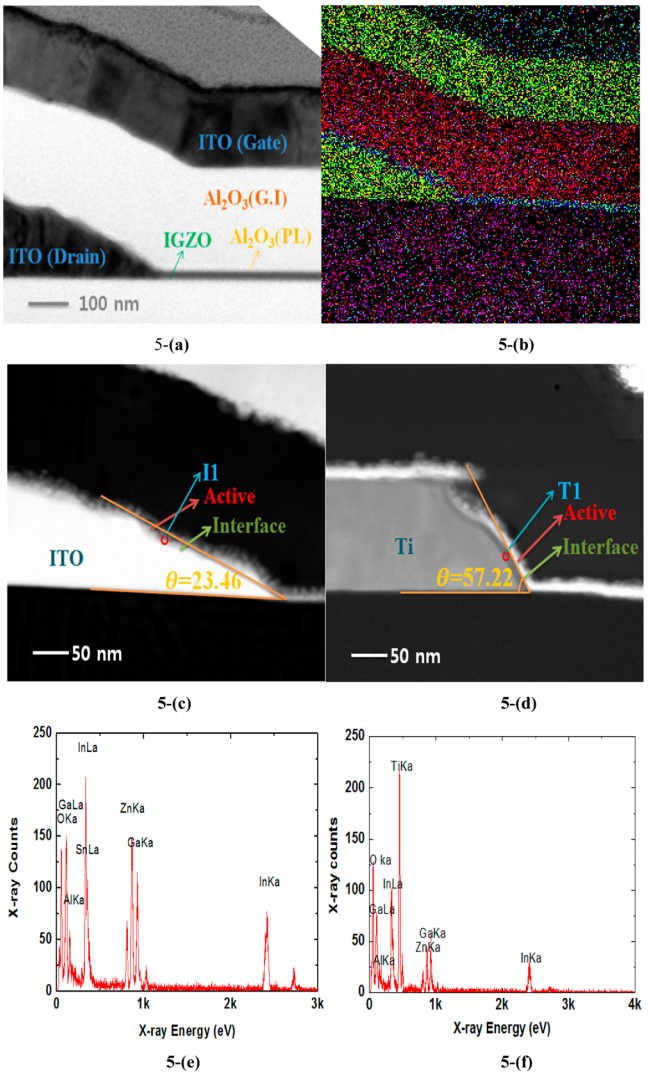

Figure 5. Cross-sectional TEM views of (a) bright and (b) EDS mapping images of the interface region between the drain electrode and IGZO channel layer for the ITO device before the drain-bias stress test. STEM-HAADF images for the (c) ITO and (d) Ti devices after the stress test for 10^4 s, in which a drain bias of 20 V was applied to the drain terminal. The interface regions of each device were marked as I1 and T1, respectively. EDS spectra of (e) point I1 for the ITO device and (f) point T1 for the Ti device. The samples were prepared using the electrically stressed devices, as tested in Figure 4a,b, in a FIB-TEM sample preparation mode.

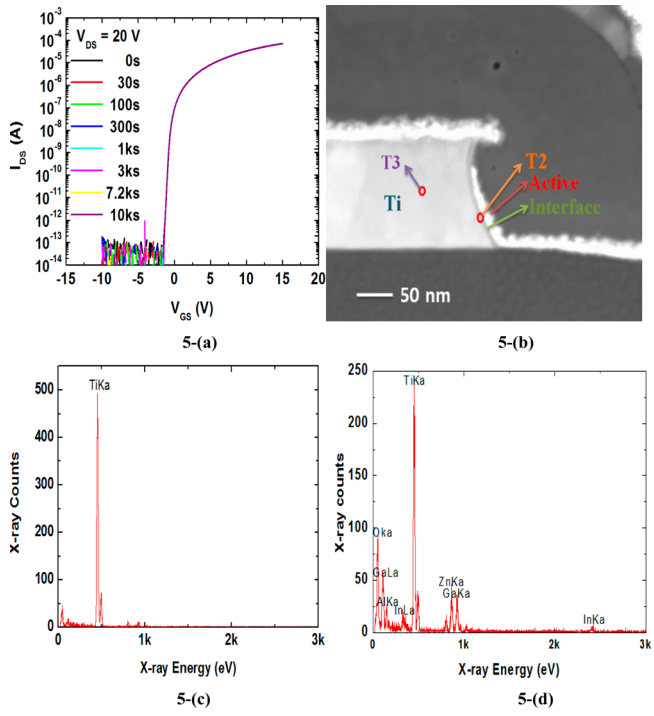

Figure 6. (a) Sets of I_{DG}–V_{GS} transfer characteristics of the Ti device annealed at 250 °C when a drain bias of 20 V was applied during the stress test for 10^4 s. V_{DS} of 10 V was applied for the measurements. V_{TH} shift in the negative direction after the drain-bias stress was observed to be as small as 0.1 V. (b) STEM-HAADF image of the Ti devices annealed at 250 °C. The interfacial transition layer and Ti bulk region were marked as T2 and T3, respectively. EDS spectra of (c) point T2 and (d) point T3.

performing the annealing treatment at a higher temperature of 250 °C. Figure 6a shows the I_{DS}–V_{GS} transfer characteristics when V_{DS} of 20 V was continuously applied to the controlled device for 10^4 s. V_{TH} did not exhibit any variation during the drain-bias stress tests, in which ΔV_{TH} was measured to be as small as 0.1 V. This value is much smaller than that (ΔV_{TH} = 0.96 V) obtained for the Ti device annealed at 200 °C. This result indicates that the postannealing process at a higher temperature of 250 °C can be an effective way of enhancing the device reliabilities. The situations at the interface and transition layer of the 250 °C-annealed Ti device were observed by TEM in the STEM-HAADF mode, as shown in Figure 6b. With maintenance of the good interface, the thickness of the transition layer was found to be reduced compared with the case of the 200 °C-annealed Ti device. The composition of this transition layer was confirmed by measuring the EDS spectra at point T2, as shown in Figure 6d. Although, as expected, the elements of In, Ga, and Zn were detected with Ti in this region, the detected amounts of diffused elements considerably decreased. For comparison, EDS was also analyzed at the bulk region of the Ti electrode (indexed as T3), as shown in Figure 6c, in which only Ti was detected without any interdiffusion during the thermal treatment and/or electrical drain-bias stress. These obtained results suggest two interesting insights: (1) The Ti device annealed at a higher temperature was more robust to undesirable interdiffusion of constituent elements between Ti and IGZO. A thinner transition layer formed at the interface resulted in enhanced device characteristics under drain-bias stress conditions. (2) The beneficial role of the transition layer as a barrier against physiochemical degradation of the interface was still valid even with a thinner thickness. Consequently, the interface between the Ti drain electrode and IGZO channel layer did not make any bad influence on the electrical characteristics, which was featured to be very different from the case of the ITO device. On the other hand, it was also confirmed that the situations for the ITO device were not so improved even when the annealing process was performed at 250 °C.

4. CONCLUSION

We have fabricated and characterized the IGZO TFT using ITO or Ti as an electrode material in order to investigate the material effects on the device reliabilities. The basic characteristics of ITO and Ti devices showed almost similar results, in which the μ_{sat}, V_{TH}, and SS were obtained as 13.4 $cm^2\ V^{-1}\ s^{-1}$,

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0.72 V, and 134 mV decade^{-1} (ITO device) and 13.8 cm^2 V^{-1} s^{-1}, 0.66 V, and 141 mV decade^{-1} (Ti device), respectively. It was also confirmed that there are excellent device stabilities under the positive and negative gate-bias stresses regardless of variations of the electrode materials. However, the drain-bias stability was sensitively dependent on the electrode materials. The negative shifts of V_{TH} for the ITO and Ti devices were 2.06 and 0.96 V, respectively. Nanoscale TEM images and EDS analysis showed big differences between the two devices. While the ITO device experienced terrible physiochemical degradation at the interface between the drain electrode and IGZO channel, the formation of a compositionally modified transition layer was observed for the Ti device. Thanks to this barrier layer, a limitless interdiffusion was suggested to be effectively suppressed. Moreover, the Ti device annealed at a higher temperature exhibited an enhanced stability under the drain-bias stress because of the synergy effects of the robust interface and role of the transition layer acting as a barrier. From these obtained results, we can conclude that the Ti device is more suitable than ITO as a drain electrode to prevent such device instabilities as a larger negative shift in V_{TH} and a stronger field dependence of the mobility under strong drain-bias stress. These informative results could be very useful for the design of the device structures and fabrication processes of the IGZO TFTs as promising backplane devices for large-area display panels with higher resolution.

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Notes

The authors declare no competing financial interest.

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