Oxide-Thin-Film-Transistor-Based Ferroelectric Memory Array

Byeong Hoon Kim, Chun Won Byun, Sung-Min Yoon, Shin Hyuk Yang, Soon-Won Jung, Min Ki Ryu, Sang-Hee Ko Park, Chi-Sun Hwang, Kyoung-Ik Cho, Oh-Sang Kwon, Eun-Suk Park, Him Chan Oh, Kyoung-Hwan Kim, and Kee Chan Park

***Abstract*—A new ferroelectric memory array on a glass substrate has been developed using In–Ga–Zn–O (IGZO) thin-film transistors (TFTs). Each memory cell is composed of two normal IGZO TFTs and a ferroelectric TFT (FeTFT). Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] is employed as the gate dielectric layer of the FeTFT. All the fabrication processes were performed below 200 °C. The fabricated memory successfully demonstrated disturb-free write/readout operation. The current ratio between the "1" and "0" states is about 10^4.**

***Index Terms*—Disturb-free, ferroelectric memory, In–Ga–Zn–O (IGZO), thin-film transistor (TFT).**

I. Introduction

DIGITAL memory integrated in a pixel of a mobile display panel is very promising for low-power driving. The power consumption for charging the large capacitance of the scan and data lines at a high frequency becomes negligible with the pixel memory. However, the conventional pixel memories are composed of normal thin-film transistors (TFTs) rather than ferroelectric transistors. Therefore, they occupy a large area to constitute a static memory like an SRAM [1]–[5]. We report a simple pixel memory structure composed of three In–Ga–Zn–O (IGZO) TFTs as shown in Fig. 1(a). One of the three IGZO TFTs has the ferroelectric poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)]/Al_2O_3 double layer as a gate dielectric. The structure of the TFT is shown in the previous publication [6]. This ferroelectric TFT (FeTFT) stores a datum,

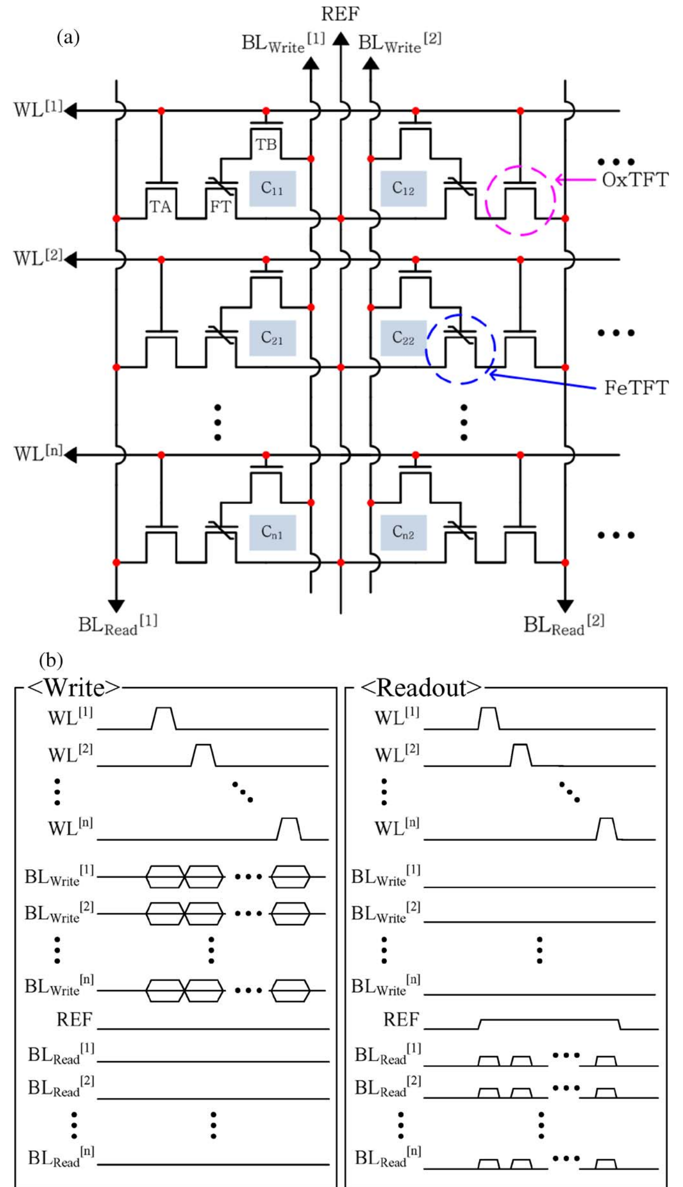

Fig. 1. (a) Circuit diagram of the proposed memory array. (b) Timing diagrams for write and readout operations.

and the other two TFTs (OxTFT) switch the bias on the FeTFT to write, hold, or readout the datum. The proposed memory array enables us to access each cell without disturbing the data stored in other cells (disturb-free operation), and the data are not destroyed during the readout process.

Manuscript received November 5, 2010; accepted November 16, 2010. Date of publication January 13, 2011; date of current version February 23, 2011. This work was supported by the Industrial Strategic Technology Development program [Project 10035225, Development of Core Technology for High Performance AMOLED on Plastic] funded by MKE/KEIT. The review of this letter was arranged by Editor J. K. O. Sin.

B. H. Kim is with the Department of Electronic Engineering, Konkuk University, Seoul 143-701, Korea, and also with the Oxide Electronics Research Team, Convergence Components and Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea.

C. W. Byun, S.-M. Yoon, S. H. Yang, S.-W. Jung, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, K.-I. Cho, O.-S. Kwon, E.-S. Park, H. C. Oh, and K.-H. Kim are with the Oxide Electronics Research Team, Convergence Components and Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea.

K. C. Park is with the Department of Electronic Engineering, Konkuk University, Seoul 143-701, Korea (e-mail: keechan@konkuk.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2096197

II. Memory Cell Design

The timing diagram for the memory array is shown in Fig. 1(b). To write a datum into the FeTFT, WL goes high, and the two switch TFTs TA and TB are turned on. $BL_{\rm Read}$ and REF are maintained at ground potential during the writing period. $BL_{\rm Write}$ conveys the datum to be stored in the FeTFT. "1" is stored if $BL_{\rm Write}$ has a positive voltage, and "0" is written if $BL_{\rm Write}$ has a negative voltage by changing the polarization of the P(VDF-TrFE) gate dielectric of the FeTFT.

When WL goes low, TA and TB are turned off, and the polarization of the FeTFT is preserved against further voltage fluctuation in $BL_{\rm Read}$ and $BL_{\rm Write}$. However, in the conventional 1T ferroelectric memory array, the data in the FeTFT are not free of this disturbance [7].

To readout the datum in the FeTFT, the potential of REF is set slightly above the ground level, and that of $BL_{\rm Read}$ is reset to ground. An optimized bias for $BL_{\rm Write}$ is applied depending on the hysteresis characteristics of the FeTFT in order to have a high current ratio between the "1" state and the "0" state and to minimize the polarization change of the P(VDF-TrFE) layer. Then, WL goes high. If "1" is stored, current may flow through the FeTFT, and a resultant potential rise in $BL_{\rm Read}$ is detected by an external sense amplifier. If "0" is stored, no potential rise may be observed.

During the readout process, the polarization change of the P(VDF-TrFE) is minimized because the electric field across the ferroelectric layer of the FeTFT is considerably reduced compared with that across the ferroelectric capacitor in the conventional 1T-1C FeRAM structure.

III. Fabrication

The TFTs were fabricated on glass substrates, and the process temperature did not exceed 200 °C. They have the staggered top-gate structure. Source/drain electrodes are made of ITO and in contact with the channel IGZO layer on them. A very thin (∼7 nm) Al_2O_3 layer was deposited to protect the channel layer during P(VDF-TrFE) patterning. A thick Al_2O_3 layer was deposited again to make the gate dielectric of the OxTFTs. As a result, the FeTFT has a P(VDF-TrFE)/Al_2O_3 double gate dielectric layer, and the OxTFT has an Al_2O_3/Al_2O_3 gate dielectric layer. On the top of the Al_2O_3 and P(VDF-TrFE), Al gate electrodes were formed. The detailed process conditions and the retention property of the FeTFT are described in the previous publications [6], [8].

Fig. 2(a) and (b) shows the transfer characteristics (I_D–V_G) of the fabricated OxTFT and FeTFT, respectively. They were measured by sweeping V_G from negative to positive and then from positive to negative in succession (double-sweep mode). The channel width and length of the TFTs are 40 and 20 μm, respectively. The field-effect mobility ($\mu_{\rm FE}$) of the OxTFT is 16.0 $cm^2/V \cdot s$, and the threshold voltage (V_T) is 2.5 V. The FeTFT exhibits hysteresis; V_T changes depending on the sweeping direction and range.

IV. Memory Cell Performance

We verified the basic operation of the memory cell as shown in Fig. 3(a). First, "0" was stored in the FeTFT by applying

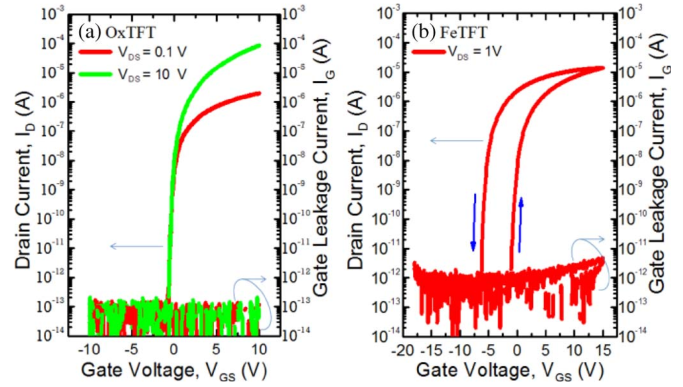

Fig. 2. I_D–V_G transfer characteristics and gate leakage currents (I_G) of the (a) fabricated normal IGZO TFT (OxTFT) and (b) IGZO TFT with ferroelectric P(VDF-TrFE)/Al_2O_3 gate dielectric (FeTFT). The measurements were performed in a double-sweep mode.

-10 V as the $V_{\rm GS}$ and $V_{\rm GD}$. In the "0" state, the current measured through TA and the FeTFT is as small as 1 pA. Then, "1" was stored in the FeTFT by applying $+10$ V as the $V_{\rm GS}$ and $V_{\rm GD}$. In the "1" state, the current is higher than 10 nA. Again, "0" was stored in the FeTFT by applying -10 V, and the current decreased to 1 pA. The switch TFTs TA and TB were turned on by $+15$ V and off by -15 V, respectively, during these operations. During the readout period, $BL_{\rm Write}$ was set to -5 V, and REF was 1 V.

Although the center of the hysteresis loop is -3 V in Fig. 2(b), it tends to shift in the negative direction due to the instability of the fabrication process. We have also found that the polarization of the P(VDF-TrFE) layer in the FeTFT does not change much as long as the gate bias is smaller than -5 V. Therefore, we applied -5 V to the gate of the FeTFT through the $BL_{\rm Write}$ during the readout period.

In order to evaluate the disturb-free write/readout operation of the memory cell, we carried out a crosstalk test as follows.

1) Write "0" or "1" in the nth row.
2) Write "1" or "0" in other rows.
3) Then, readout the data in the nth row.

Fig. 3(b) and (c) again shows that the current is as small as 1 pA when "0" is stored in the FeTFT. However, it is 10 nA when "1" is stored. This confirms that the data can be kept intact while other data are conveyed through the bit lines (disturb-free operation). In addition, the current measured at 1 s after the beginning of the readout process is, as shown in Fig. 3(c), larger than half of its initial value. This confirms the nondestructive readout characteristics of the fabricated memory, which may be attributed to the fact that the electric field across the ferroelectric layer is not so strong to change the polarization.

V. Conclusion

We have designed a new FeRAM structure based on the IGZO TFT technology. The channel conductivity of the FeTFT with the P(VDF-TrFE)/Al_2O_3 double gate dielectric and the IGZO active layer could be modulated by the polarization state of the P(VDF-TrFE) layer. Each memory cell composed of two normal IGZO TFTs and an FeTFT successfully exhibited disturb-free and nondestructive write/readout characteristics.

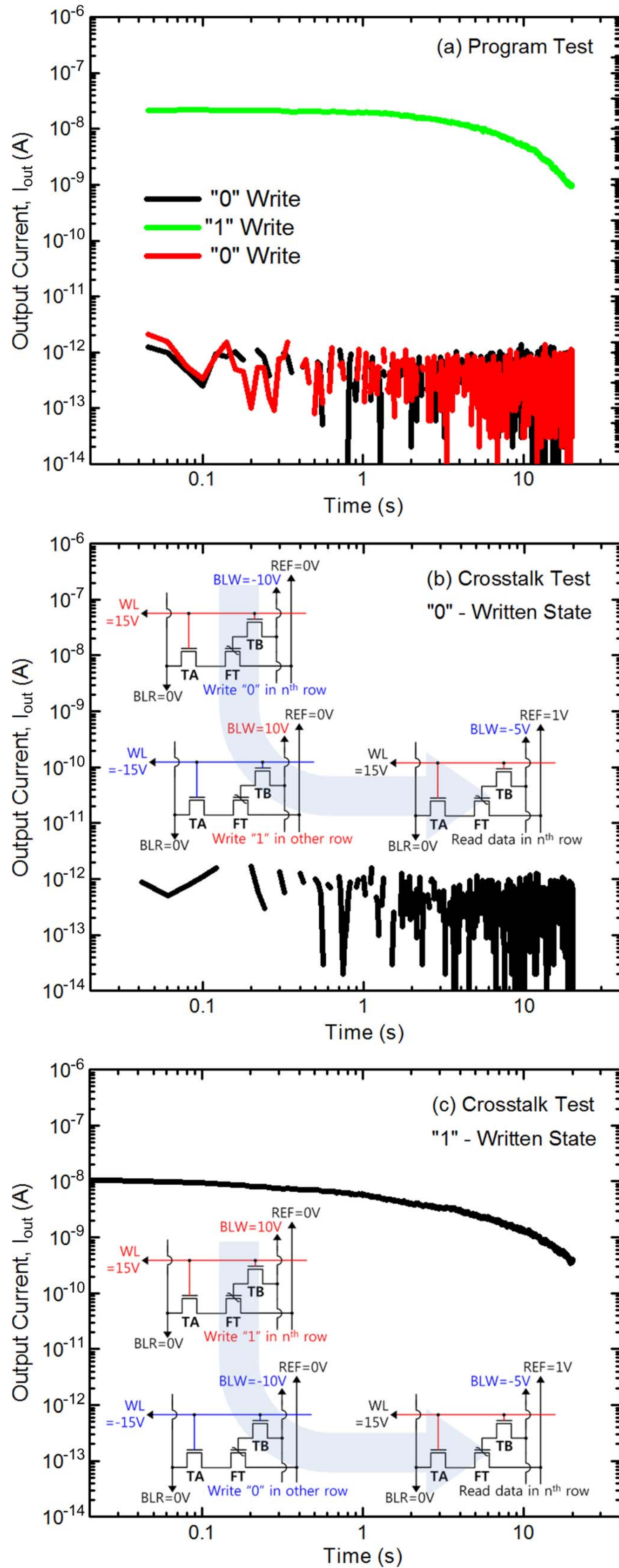

Fig. 3. (a) Readout currents for basic write/readout operations. Results of crosstalk test for (b) "0"-written state and for (c) "1"-written state.

The TFTs were fabricated on glass substrates, and the process temperature did not exceed 200 °C. The output current ratio between the "1" and "0" states was as high as 10^4. These results indicate that the new FeRAM structure can be used for various applications where a low-temperature process is required as well as display devices.

References

[1] N. Ueda, Y. Ogawa, K. Tanaka, K. Yamamoto, and Y. Yamauchi, "A novel multi-level memory in pixel technology for ultra low power LTPS TFT-LCD," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. Papers*, 2010, pp. 615–618.

[2] L.-W. Chu, P.-T. Liu, M.-D. Ker, G.-T. Zheng, Y.-H. Li, C.-H. Kuo, C.-H. Li, Y.-J. Hsieh, and C.-T. Liu, "Design of analog pixel memory circuit with low temperature polycrystalline silicon TFTs for low power application," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. Papers*, 2010, pp. 1363–1366.

[3] H. Kimura, T. Maeda, T. Tsunashima, T. Morita, H. Murata, S. Hirota, and H. Sato, "A 2.15 inch QCIF reflective color TFT-LCD with digital memory on glass (DMOG)," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. Papers*, 2001, pp. 268–271.

[4] Y. Nakajima, Y. Teranishi, Y. Kida, and Y. Maki, "Ultra-low-power LTPS TFT-LCD technology using a multi-bit pixel memory circuit," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. papers*, 2006, pp. 1185–1188.

[5] Y. Asaoka, E. Satoh, K. Deguchi, T. Satoh, K. Minoura, I. Ihara, S. Fujiwara, A. Miyata, Y. Itoh, S. Gyoten, N. Matsuda, and Y. Kubota, "Polarizer-free reflective LCD combined with ultra low-power driving technology," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. Papers*, 2009, pp. 395–398.

[6] S.-M. Yoon, C.-W. Byun, S. Yang, S.-H. K. Park, D.-H. Cho, S.-W. Jung, S.-Y. Kang, and C.-S. Hwang, "Nondestructive readout operation of oxide-thin-film-transistor- based 2T-type nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 138–140, Feb. 2010.

[7] H. Saiki and E. Tokumitsu, "Ferroelectric split-gate-field-effect-transistors for nonvolatile memory cell array," *IEICE Trans. Electron.*, vol. E87-C, no. 10, pp. 1700–1705, Oct. 2004.

[8] S.-M. Yoon, S.-H. Yang, S.-W. Jung, C.-W. Byun, S.-H. K. Park, C.-S. Hwang, G.-G. Lee, E. Tokumitsu, and H. Ishiwara, "Impact of interface controlling layer of Al_2O_3 for improving the retention behaviors of In–Ga–Zn oxide-based ferroelectric memory transistor," *Appl. Phys. Lett.*, vol. 96, no. 23, p. 232 903, Jun. 2010.