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Al-Zn-Sn-O Thin Film Transistors with Top and Bottom Gate Structure for AMOLED

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SUMMARY We have fabricated the transparent bottom gate and top gate TFTs using new oxide material of Al-Zn-Sn-O (AZTO) as an active layer. The AZTO active layer was deposited by RF magnetron sputtering at room temperature. Our novel TFT showed good TFT performance without post-annealing. The field effect mobility and the sub-threshold swing were improved by the post-annealing, and the mobility increased with SnO_2 content. The AZTO TFT (about 4 mol% AlOx, 66 mol% ZnO, and 30 mol% SnO_2) exhibited a mobility of 10.3 cm^2/Vs, a turn-on voltage of 0.4 V, a sub-threshold swing of 0.6 V/dec, and an on/off ratio of 10^9. Though the bottom gate AZTO TFT showed good electrical performance, the bias stability was relatively poor. The bias stability was significantly improved in the top gate AZTO TFT. We have successfully fabricated the transparent AMOLED panel using the back-plane composed with top gate AZTO TFT array.

key words: *thin film transistor, oxide, AMOLED, transparent*

1. Introduction

New flat panel displays based on organic light emitting diodes (OLED) have attracted interests because they are considered as blue ocean electronic products. Small-size active matrix OLED (AMOLED) displays are already used on mobile phones. The reliable TFT back-plane showing good electrical performance is indispensable for large-size AMOLED and it should be manufactured at low temperature for the flexible displays which are commercially available. In recent time, the flat panel display televisions demand high resolution, large size, fast response, and low power consumption. As the display size and resolution increases, the TFT back-plane with good uniformity and high stability is required [1]. Conventional a-Si TFT can be fabricated with high uniformity and low cost, however its mobility and bias stability are poor. LTPS (low temperature poly silicon) TFT has disadvantages for large size production due to relatively poor uniformity and high cost [2]. For these reasons, oxide TFT back-planes are considered as prominent candidate for the driving device of AMOLED. There are some candidates for oxide TFT material, and the oxide TFTs using ZnO [3], In-Zn-O [4], Zn-Sn-O [5], IGZO [6]–[8], and Al-Zn-Sn-O [9] as active channel material have been widely studied. Zn-Sn-O TFT is generally required high temperature (> 300°C) processing to represent a good electrical performance [5]. Several studies concerning about the oxide TFTs processed at low temperature (< 150°C) were reported, however the electrical performances were relatively poor [10]. We have successfully fabricated the oxide TFTs with a novel active layer which was composed with Al_2O_3-ZnO-SnO_2 (AZTO) and sputtered at room temperature [9], [11]. Al^{3+} is not a heavy-metal cation, therefore, the addition of Al_2O_3 is considered not to enhance the electron transport. However, addition of Al^{3+} may enhance the chemical and electrical stability like Ga^{3+} in In-Ga-Zn-O system [12]. The AZTO material is very stable chemically, and sputtering method has advantages on low cost and large area uniformity among various deposition methods. Therefore, the AZTO TFT is prominent device for driving the large size AMOLED panel. In this paper, we report the electrical characteristics and gate bias stabilities depending on TFT structures.

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2. Experimental Procedure

We have fabricated bottom gate and top gate TFTs with the new active material sputtered at room temperature. The novel active material was composed with amorphous oxide of Al_2O_3-ZnO-SnO_2. The schematic diagram of the AZTO TFT with the bottom gate and the top gate structure are shown in Fig. 1. The TFTs have a co-planar structure in the bottom gate structure and a staggered structure in the top gate structure. A 100×100 mm^2 alkaline-free glass was used as a substrate after the ultrasonic cleaning with acetone, iso-propyl alcohol and DI water in sequence. Gate and source/drain electrodes were constituted with 150 nm thick indium tin oxide (ITO). A gate insulator of Al_2O_3 was formed by atomic layer deposition (ALD) method at 150° and its thickness was 185 nm. An aluminum precursor was tri-methyl aluminum and an oxygen precursor was water vapor. An active layer of AZTO was formed by co-sputtering of an Al_2O_3-ZnO target and a SnO_2 target with an off-axis type RF magnetron sputter at room temperature. The sputtering was performed in the atmosphere of Ar and O_2 mixed gas with the chamber pressure of 0.2 Pa. All patterning processes were performed by conventional photo-lithographic method and wet etching process. The post-annealing was performed in vacuum using electric ovens. The electrical characteristics of the TFTs were measured with a semiconductor parameter analyzer (Agilent B1500A). The bias stabilities of the TFTs were measured with other semiconductor analyzer (HP 4145B). All the electrical measurements

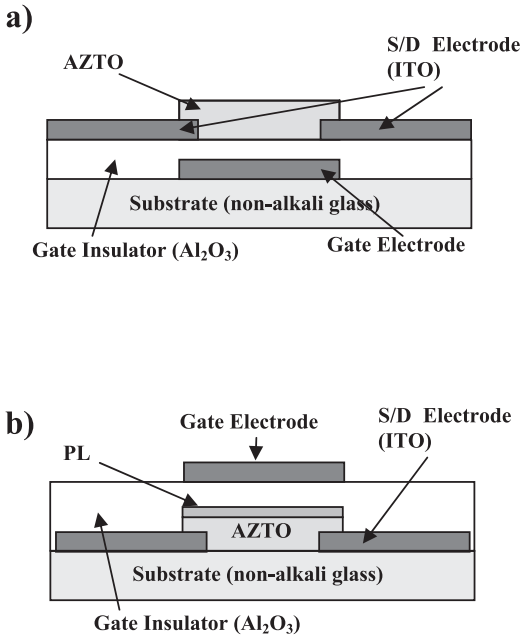

Fig. 1 The structure of the a) bottom gate and b) top gate AZTO TFT.

were carried out in air at room temperature. The bias stability measurements were performed under stress condition of $V_g = +20$ V and $V_{ds} = 0$ V. X-ray diffraction (XRD) spectra of the AZTO films were recorded with a Rigaku RU-200BH diffractometer using CuKα radiation. The chemical composition of the AZTO thin film was analyzed by Auger electron spectroscopy (AES) method. The electrical properties including the field effect mobility (μ_{FET}), the turn-on voltage (V_{on}), the on-off current ratio (I_{on}/I_{off}) and the sub-threshold swing (S/S) were calculated from the data of the transfer curve under 15.5 V source-drain voltage.

3. Results and Discussion

The thin films of AZTO deposited by RF magnetron sputtering were amorphous. Figure 2 shows the XRD spectra of AZTO thin films deposited on Si wafer by RF magnetron sputtering before and after annealing. There was no diffraction peak of crystalline phase in the XRD spectra even after the 300°C annealing. The AZTO active layer of the TFT was considered as very stable amorphous oxide material. Amorphous oxide active layer has advantages on large area uniformity and long-term reliability because it has no grain boundary [12]. Figure 3 shows the transfer characteristics of the bottom gate AZTO TFTs (W/L = 40 μm/20 μm) without heat treatment and after 150°C and 180°C annealing in vacuum. The composition of the active layer measured by AES was about 4 mol% AlOx, 66 mol% ZnO, and 30 mol% SnO_2. The AZTO TFT prepared at room temperature showed the μ_{FET} of 1.9 cm^2/Vs, the V_{on} of near −2.0 V, the I_{on}/I_{off} of more than 10^7. The off-current level was under 10^{-12} A and the S/S was relatively large. The 150°C annealed TFT exhibited the μ_{FET} of 6.2 cm^2/Vs, the V_{on} of 0.9 V, the I_{on}/I_{off} of about 10^9 and the S/S of 0.60 V/dec.

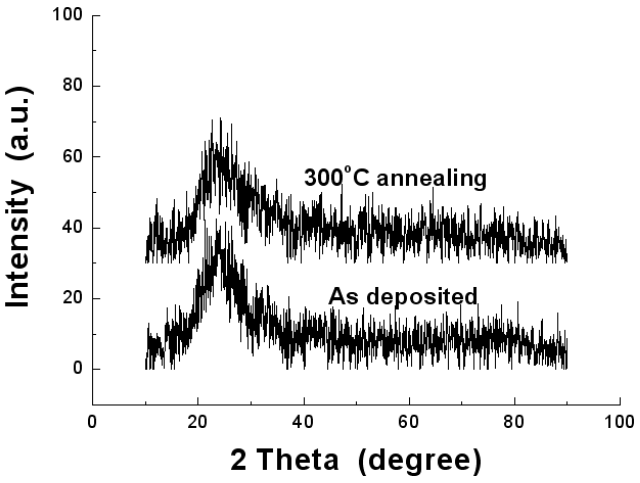

Fig. 2 XRD spectra of AZTO thin films before and after annealing.

The 180°C annealed TFT exhibited the μ_{FET} of 10.1 cm^2/Vs, the V_{on} of 0.9 V, the I_{on}/I_{off} of more than 10^9 and the S/S of 0.58 V/dec. It can be seen that the mobility increased with increasing the annealing temperature. The sub-threshold swing and the on-off current ratio were also improved with increasing annealing temperature. The turn-on voltage of the AZTO TFT was −1.1 V before the annealing. The turn-on voltage shifted to near 0 V by the low temperature annealing. Electrical performance was sufficiently good for the application to active matrix displays just by post-annealing at the temperature higher than 150°C. The electrical properties improved by post annealing up to about 250°C, and scarcely improved above 250°C. The electron transport properties of the as-deposited films fabricated at the inadequate condition are known to be improved by thermal annealing to a level which is almost the same as that in the films deposited at the optimized condition [13]. The AZTO active layer deposited by room temperature sputtering was supposed not to be optimized and improved by the post annealing. The field effect mobility changes with SnO_2 composition are shown in Fig. 4. The mobilities in Fig. 4 were measured for the bottom gate AZTO TFTs with the active layer composition of $xSn(1-x)(Al_{0.06}Zn_{0.94})O_y$. The mobility increased with SnO_2 content, and the mobility change was large until 16 mol% of SnO_2, from then, the mobility increment became slowdown. Below 10 mol% of SnO_2, the AZTO thin film did not show the field effect transistor characteristics, thus the mobility could not be measured. Amorphous oxides composed of heavy-metal cations with $(n-1)d^{10}\,ns^0$ ($n \geq 4$) electronic configurations show high electron mobilities because ns^0 ($n \geq 4$) orbitals overlap between adjacent orbitals. The large diameter and spherical symmetry of the ns^0 orbitals lead high degree of overlap and conduction band dispersion [5], [12]. In the AZTO thin films, Sn^{4+} and Zn^{2+} are such heavy-metal cations. As a result of the mobility dependence on SnO_2 content in Fig. 4, Sn^{4+} is supposed to control the field effect mobility rather than Zn^{2+} because $5s^0$ orbital of Sn^{4+} is larger than $4s^0$ orbital of Zn^{2+} [12].

Figures 5 and 6 show the transfer characteristics of the

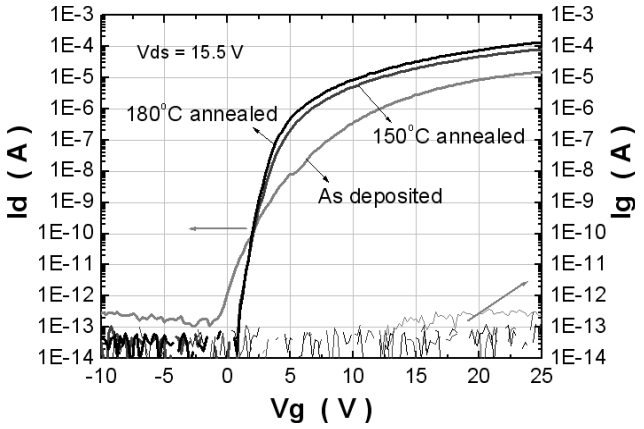

Fig. 3 Transfer characteristic change of AZTO TFTs with annealing temperature.

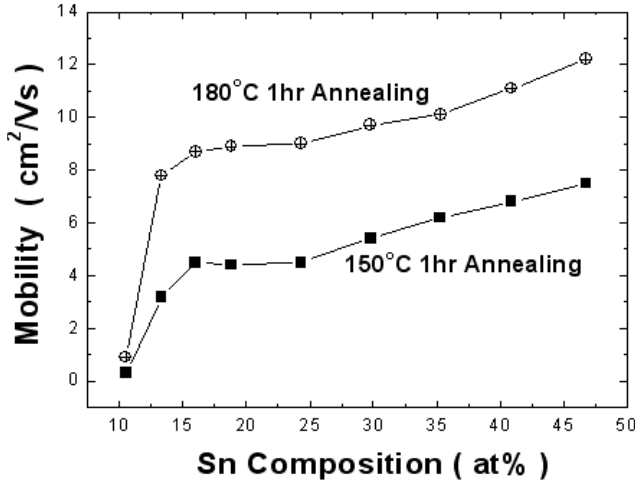

Fig. 4 The field effect mobility change with SnO_2 content in AZTO active layer.

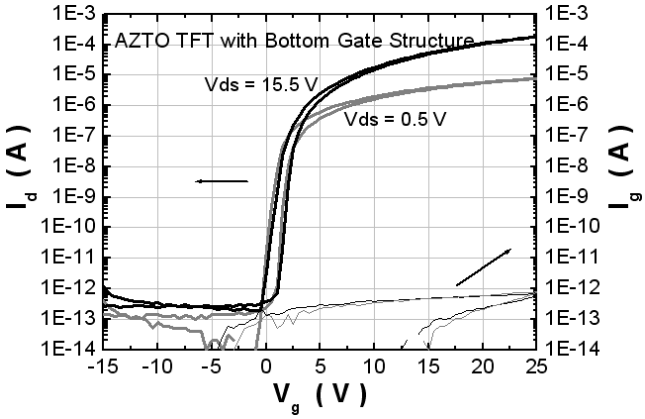

Fig. 5 Transfer characteristics of the bottom gate AZTO TFT after annealing at 250°C.

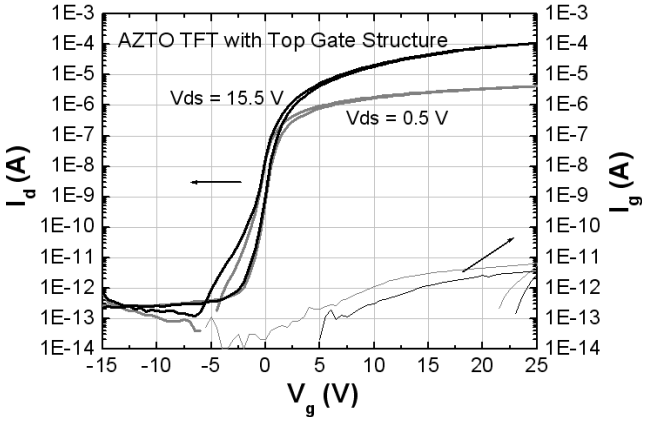

Fig. 6 Transfer characteristics of the top gate AZTO TFT after annealing at 250°C.

bottom gate and the top gate AZTO TFT after annealing at 250°C, respectively. The composition and sputtering condition of active layer, the gate insulator material and thickness were same in both cases. The turn-on voltage of the top gate AZTO TFT was about −5 V, while that of the bottom gate TFT was near 0 V. The μ_{FET}'s of the bottom gate TFT and the top gate TFT were 10.3 cm^2/Vs and 6.0 cm^2/Vs, respectively. The top gate TFT showed shoulders in the sub-threshold region as shown in Fig. 6. In the bottom gate structure the interface between active layer and gate insulator is damaged by ITO and active layer sputtering process. Since those sputtering damages were partially recovered by post-annealing, the electrical properties were improved by the post-annealing. On the other hand, the active layer and the interface of the top gate structure may be contaminated or damaged during the active layer patterning and gate insulator deposition process. We have patterned the active layer by conventional photo-lithography method. Thus, the active layer surface might be contaminated by photoresist and PR stripper. The surface contamination is connected to the active-insulator interface defects. The Al_2O_3 gate insulator was deposited by atomic layer deposition (ALD) method using tri-methyl aluminum and water vapor at high temperature so that the active-insulator interface in the top gate TFT might be contaminated with hydrogen and carbon related defects. It is thought that such defects are hard to be eliminated sufficiently and may cause the sub-threshold region shoulders and the decrease of mobility. Those defects can be reduced by an appropriate gate insulator deposition process and post-annealing. Figures 7 and 8 show the gate bias stabilities of the bottom gate and the top gate AZTO TFT, respectively. The shift of V_{on} of the bottom gate AZTO TFT and the top gate AZTO TFT under +20 V of gate bias after 14 hrs was 7.6 V and 0.8 V, respectively. The gate bias stability of the top gate AZTO TFT was improved significantly compared to that of the bottom gate TFT. The gate bias instability is thought to originate primarily from charge trapping considering the direction of the V_{on} shift. The interface between active layer and gate insulator of the bottom gate TFT may have a lot of electron traps compared to the top gate TFT. A large part of the insulator interface damage that causes the degradation of μ_{FET} and S/S is supposed to be eliminated by post-annealing at a high temperature for

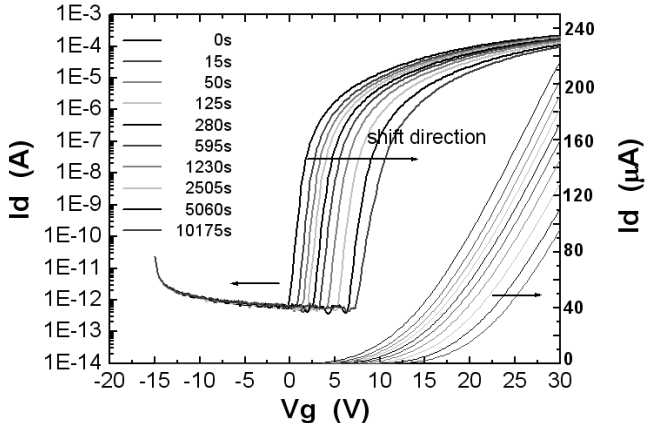

Fig. 7 Transfer curve shift of the bottom gate AZTO TFT annealed at 250°C under the +20 V gate bias voltage.

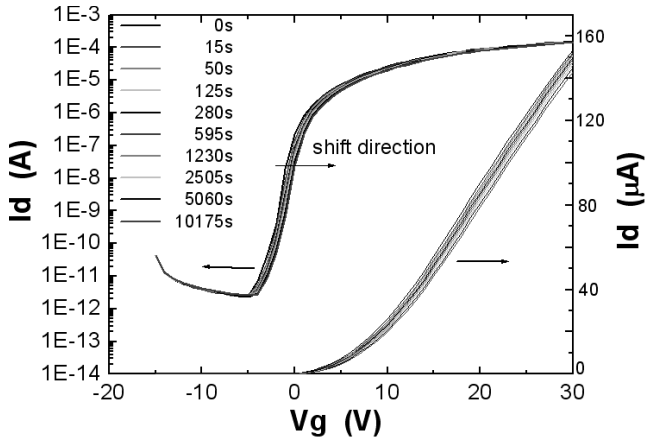

Fig. 8 Transfer curve shift of the top gate AZTO TFT annealed at 250°C under the +20 V gate bias voltage.

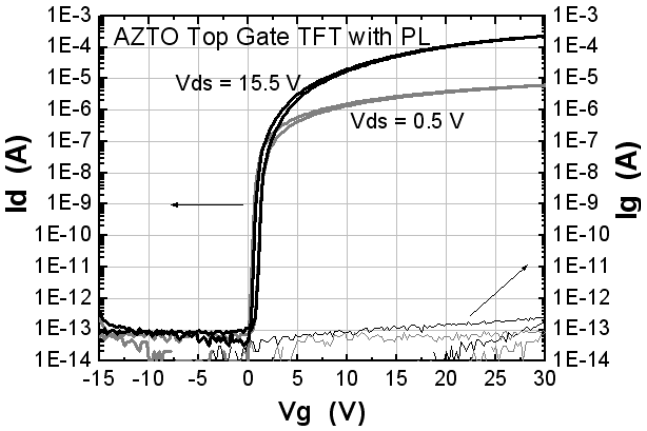

Fig. 9 Transfer characteristics of the top gate AZTO TFT with PL after annealing at 300°C.

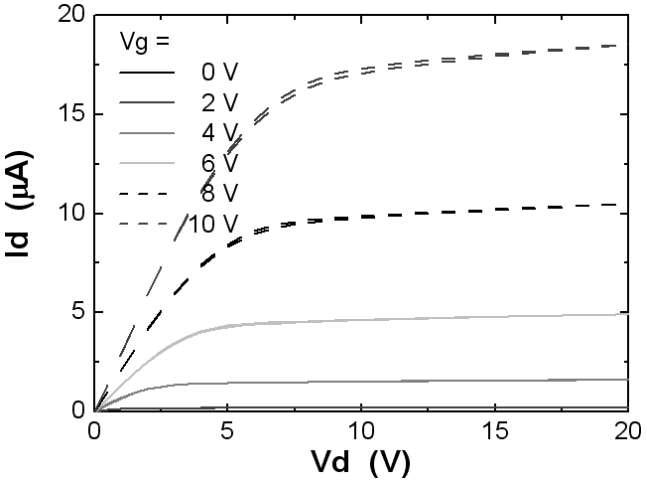

Fig. 10 Output characteristics of the top gate AZTO TFT with PL after annealing at 300°C.

the bottom gate structure. However the charge traps degrading the bias stability can't be eliminated sufficiently in the bottom gate TFTs just by the post-annealing. In the case of the top gate structure, the electrical characteristics did not improved to a level of the bottom gate TFT by the post-annealing, while the gate bias stability was significantly improved compared to that of the bottom gate TFT. The origins suffering the electrical characteristics are supposed to be different from those suffering the bias stability.

The top gate structure has advantages on the bias stability and is appropriate for the driving devices of AMOLED. We investigated the optimum process for the AZTO TFT with top gate structure. The control of the active-insulator interface was thought to be the most important process for controlling final electrical characteristics of the top gate TFT. Before the active layer patterning and the gate insulator deposition, we deposited the thin (30 nm) Al_2O_3 protective layer (PL) on the active layer with plasma enhanced ALD in order to reduce the active-insulator interface contamination of hydrogen and carbon related defects. The oxygen precursor for ALD was not water vapor but oxygen plasma in the PL process. The PL was deposited after the active layer deposition and active patterning was carried out after the PL deposition. Therefore, the contamination of the interface between active and insulator by photoresist and PR stripper was not occurred. Figures 9 and 10 show the transfer and output characteristics of the AZTO TFT including the PL after annealing at 300°C, respectively. The shoulders in sub-threshold region were almost disappeared and the S/S was significantly improved to 0.15 V/dec. The μ_{FET} of the PL-included AZTO TFT with top gate structure increased up to 9.5 cm^2/Vs. It was similar value to μ_{FET} of the bottom gate TFT. Figure 11 shows the gate bias stability of the top gate AZTO TFT including the PL. The shift of V_{on} was smaller than 0.2 V after 14 hour gate bias stress.

In the case of the top gate TFT including the PL, the S/S and hysteresis were poor after annealing below 250°C. However, the 300°C annealing improved them remarkably. The PL and post-annealing at relatively high temperature was effective to improve not only the electrical characteristics but also the bias stability. For comparison, the transfer curve and gate bias stability characteristics of the 300°C an-

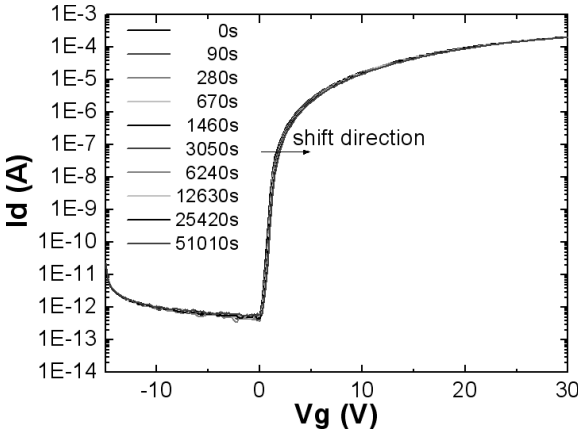

Fig. 11 Transfer curve shift of the top gate AZTO TFT with PL under the +20 V gate bias voltage.

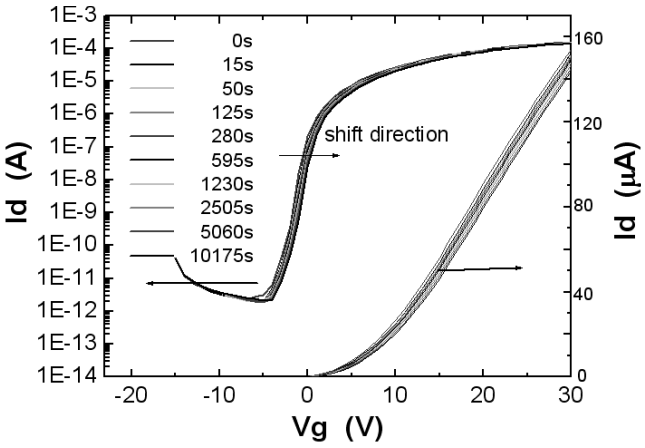

Fig. 13 Transfer curve shift of the top gate AZTO TFT annealed at 300°C without PL under the +20 V gate bias voltage.

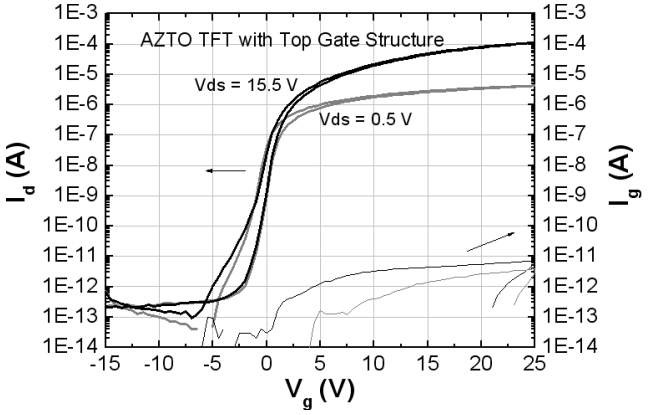

Fig. 12 Transfer characteristics of the top gate AZTO TFT without PL after annealing at 300°C.

Fig. 14 AMOLED panel using the top gate AZTO TFT back-plane.

nealed AZTO TFT without PL are shown in Figs. 12 and 13, respectively. The μ_{FET} of the 300°C annealed top gate AZTO TFT without PL was 6.2 cm^2/Vs. And the shoulders in sub-threshold region and S/S were scarcely improved compared to the 250°C annealed TFT. The shift of V_{on} under +20 V of gate bias after 14 hrs was 0.7 V as shown in Fig. 13. The bias stability was scarcely improved too. The improvement of electrical properties and stability are considered to be restrictive just by post-annealing. The interface control by the PL was more important to improve the electrical properties and stability than the post annealing. Although the PL thickness was 30 nm, it was enough to protect the active-insulator interface from the contamination. Therefore, the defects degrading electrical characteristics at the active-insulator interface region were supposed to be reduced by the PL deposited with plasma enhanced ALD. Generally, oxygen plasma treatment on oxide thin film may damage the surface and the surface damage can be recovered by post-annealing considerably. In oxide TFTs, the interface defects related oxygen vacancy, hydrogen and carbon may deteriorate the electrical properties significantly. And the active surface should be defective before the PL deposition because the active layer deposited by room temperature sputtering. It is supposed that the oxygen plasma used in the PL process reduced such defects and the post-annealing at 300°C recovered the oxygen plasma-induced damages sufficiently. The oxygen plasma effect and the post-annealing in combination with the elimination of active patterning process were considered to enhance the electrical performance and stability of the top gate AZTO TFTs.

The transparent AMOLED panel using the top gate AZTO TFT back-plane is shown in Fig. 14. The AMOLED pixel had 2 transistors and 1 capacitor structure, and the AMOLED display specification was 2.5 inch QCIF+ monochrome. The TFT array had staggered type top gate structure, the Al_2O_3 PL, and the Al_2O_3 gate insulator by atomic layer deposition method. The transparency of the AMOLED panel in visible region was more than 55%. Although left side of the AMOLED panel showed many white spots, the image of the input data was clear and bright. The back-plane of the AMOLED panel using the top gate AZTO TFT array showed good electrical performance and stability.

4. Conclusion

We have manufactured novel oxide TFTs with Al_2O_3-ZnO-SnO_2 (AZTO) active layer which was deposited at room temperature and processed at relatively low temperature. The AZTO layer was deposited by the RF magnetron sputtering which is convenient for large size commercial production. The film deposition at room temperature and the low temperature processing are significant advantages for the fabrication of flexible electronics. The AZTO TFTs with bottom gate structure exhibited good electrical performance in spite of low temperature processing. The 180°C annealed TFT with bottom gate structure exhibited the μ_{FET} of 10.1 cm^2/Vs, the V_{on} of 0.9 V, the I_{on}/I_{off} of more than 10^9 and the S/S of 0.58 V/dec. However, their bias stability was not enough to apply AMOLED back plane. The AZTO TFT with top gate structure including protective layer showed excellent bias stability as well as good field effect mobility (9.5 cm^2/Vs) and sub-threshold swing (0.15 V/dec). We also fabricated the 2.5 inch AMOLED panel (QCIF+; 176 X 220, MONO) driven by the top gate AZTO TFT. We are developing the optimum process of AZTO TFT fabrication at low temperature below 200°C for better performance. The AZTO TFT is considered to be an excellent candidate for active matrix back-plane of large size flexible displays and electronics with plastic substrates.

Acknowledgments

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