A Low-Power Single-Input Level Shifter for Oxide Thin-Film Transistors

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***Abstract*—A new level shifter circuit suitable for implementation using n-channel oxide thin-film transistors (TFTs) is reported. This level shifter is designed to convert a single 10 V input signal into a 20 V output signal. In order to raise the output voltage up to V_{DD} in spite of the large zero-V_{GS} current of the oxide TFT, negative V_{GS} is applied to the pull-down TFTs. Simulation and fabrication results show that the level shifter operates correctly with oxide TFTs and that the power consumption is as low as 0.2 mW at an input signal frequency of 10 kHz.**

***Index Terms*—Level shifter, low-power, negative threshold voltage, oxide thin-film transistor (TFT).**

I. Introduction

RECENTLY oxide thin-film transistors (TFTs) employing In–Ga–Zn–O (IGZO) active layer has attracted considerable attention because of their relatively high on-current and low fabrication cost [1]–[3]. The high on-current of the oxide TFTs improves the pixel charging rate, reduces the operating voltage and/or increases the aperture ratio in active-matrix liquid-crystal displays (AMLCDs) [3]. Oxide TFTs also exhibit high short-range uniformity that resolves the mura issue in active-matrix organic light-emitting diode (AMOLED) displays [4], [5]. In addition, the high current-driving capability of the oxide TFTs enables us to integrate driving circuits on a glass substrate such as a level shifter and a DC–DC converter as well as a scan driver [6]–[8].

Unfortunately, oxide TFTs often have negative threshold voltages ($V_T s$) due to process fluctuation or external influences such as illumination and bias stress [9]–[12]. Accordingly a considerable amount of current can flow at zero gate-to-source bias (V_{GS}). Because of the possibility of having negative V_T, it is not desirable to utilize conventional circuit scheme when we make driving circuitry on a display panel using the oxide TFTs. B. Kim *et al.* have reported a level shifter circuit that operates properly with the oxide TFT by applying negative V_{GS} to turn off the pull-down TFT [6]. However a substantial current flows between V_{DD} and V_{SS} through the diode-connected TFT in their circuit when the output is low, which leads to high power consumption. If the channel width-to-length ratio of the diode-connected TFT is decreased so as to reduce power consumption, V_{GS} of the pull-up TFT would decrease during bootstrapping, which may result in longer rise time of the output signal.

In this letter, we propose a low-power single-input level shifter as shown in Fig. 1. To reduce power consumption, there is no diode-connected TFT in the circuit and the pull-up TFTs and the pull-down TFTs are never turned on simultaneously. In addition, only a single input signal is required by this circuit, which simplifies the interface design considerably.

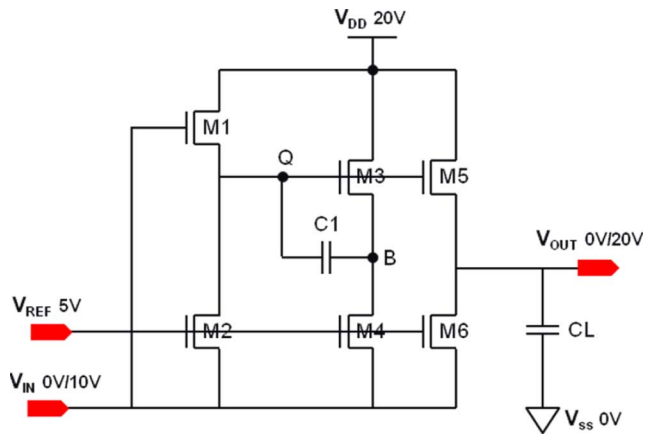

Fig. 1. Circuit diagram of the single-input level shifter for oxide TFTs.

II. Operation of Level Shifter

Fig. 1 is the circuit diagram of the low-power single-input level shifter. It is composed of six TFTs and one capacitor. The capacitor facilitates the bootstrapping ability of M3. In this example, a single input signal of 10 V swing drives the circuit and a 20 V swing output signal is produced because the supply voltage V_{DD} is 20 V. The channel widths/lengths of TFTs M1–M6 are 100/10, 100/10, 100/10, 750/180, 100/10, and 500/10, respectively, in microns. The capacitance of C1 is 6.5 pF.

When the input signal V_{IN} is 0 V, the pull-down TFTs M2, M4, and M6 are turned on with $V_{GS} = +5$ V because V_{REF} is 5 V. On the contrary, the pull-up TFTs M1, M3, and M5 are turned off because V_{IN} is 0 V and node Q is also pulled down to 0 V through M2. Accordingly the voltages of nodes B and OUT also become 0 V.

Fig. 2 shows the SPICE simulation results of the level shifter for two cases: (a) $V_T = 0$ V and (b) $V_T = -2$ V. As V_{IN} rises from 0 V to 10 V at the beginning of T_1 period, M1 is turned on with $V_{GS} = +10$ V and therefore node Q begins to be pulled up from 0 V. At this moment, M4 is still on with $V_{GS} = +5$ V. It should be noted that node B is the source of M4 during T_1 period because V_{IN} (10 V) is higher than the potential at node B. Accordingly, the B node voltage also rises. During T_1 period the rate of increase in the voltage at node Q should be faster than that at node B so as to make the V_{GS} of M3 large. This is accomplished partly by the larger V_{GS} of M1 (10 V) than that of

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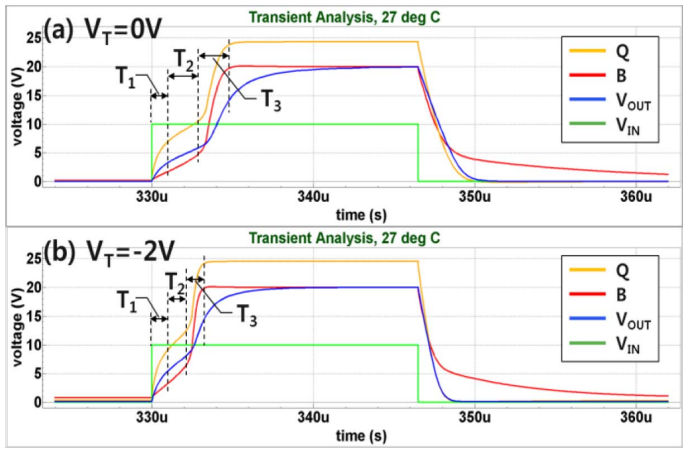

Fig. 2. SPICE simulation results of the level shifter for (a) TFT $V_T = 0$ V and (b) -2 V. A 20 pF load capacitance is attached to the output.

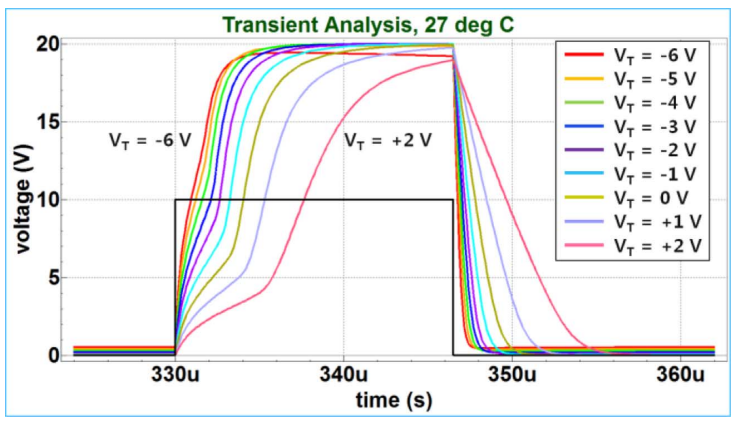

Fig. 3. SPICE simulation results of the level shifter for various TFT V_T values. A 20 pF load capacitance is attached to the output.

M4 (5 V). Additionally we increased the parasitic capacitance attached to node B by increasing the size of M4 so as to delay the voltage rise at node B. The channel area of M4 is more than one hundred times larger than those of M1–M3. In Fig. 2, the rate of increase of the Q node voltage is much faster than that of the B node voltage during T_1 period for the above-mentioned reasons. As the Q node voltage quickly rises, $V_{\rm GS}$ of M1 decreases much faster than that of M4. Soon $V_{\rm GS}$ of M1 and M4 become similar. At the end of T_1 period, $V_{\rm GS}$ of M3 becomes about 5 V, as desired.

Next, the rate of increase in the voltages at nodes Q and B is similar during T2 period. Finally at the end of T2 period, M1 and M4 are turned off as the Q node voltage approaches (10 V-V_{T1}) and the B node voltage approaches (5 V-V_{T4}). As M1 is turned off, node Q becomes floating. At this moment, $V_{\rm GS}$ of M3 is 5 V if V_{T1} is the same as V_{T4}. Therefore the bootstrapping effect of M3 occurs.

The bootstrapping effect is enhanced during T_3 period because the parasitic capacitance attached to node B is greatly decreased as M4 is turned off. Owing to the enhanced bootstrapping effect, the voltages at nodes Q and B rise very quickly as shown in Fig. 2(a) and (b). As the Q node voltage becomes higher than $V_{\rm DD}$, the output voltage finally reaches $V_{\rm DD}$. It should also be noted that the boosted Q node voltage is preserved, even if the TFTs have negative V_T, because M1 and M2 (the only TFTs connected to the Q node) are turned off with negative $V_{\rm GS}$, i.e., -10 V for M1 and -5 V for M2 when the output is high.

III. Results

We used SmartSpice to simulate the operation of the new level shifter circuit. The RPI amorphous silicon TFT model (level 35) was used to fit the measured IGZO TFT characteristics. We prepared several IGZO TFT models with various values of V_T to investigate the performance of the circuit. A 20 pF load capacitor was attached to the output node.

Fig. 3 shows the simulated output voltage waveforms for various TFT V_T values. The level shifter operates correctly for a range of V_T from -5 V to $+1$ V when the input signal frequency is 30 kHz. For $V_T = -6$ V, the output voltage decreases while the input is kept high because the Q node voltage drops due to the leakage current through the M2 TFT which is turned off with $V_{\rm GS} = -5$ V. For $V_T = +2$ V, the output does not reach $V_{\rm DD}$ (20 V) because $V_{\rm GS} = +5$ V for M3 is not sufficient to charge node B during such a short period (16.7 μs) and because the on-current of M5 is reduced.

Fig. 4 shows the measured output waveform of the fabricated level shifter employing IGZO TFTs. The inset of this figure shows the fabricated circuit. The value of V_T of the TFTs around the circuit on the same substrate ranges from -2 V to -1 V. Even though the TFTs have negative V_T values, the circuit op-

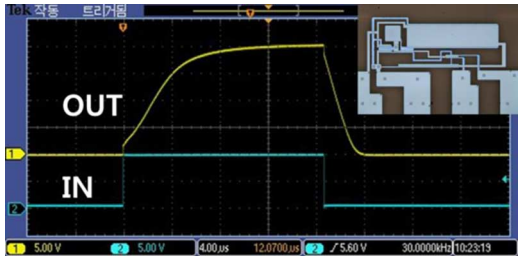

Fig. 4. Measured input and output waveforms of the level shifter fabricated using the IGZO TFT process. The inset shows the fabricated circuit. The input signal frequency is 30 kHz.

erates correctly and the measured output waveform is similar to the simulation results.

The power consumption of the fabricated circuit depends on the operating frequency. It is 0.43 mW for a 30 kHz input signal and 0.20 mW at 10 kHz. This is 30% lower than that for the previous report [6]. Unlike in the previously developed circuit, there is no static current path between V_{DD} and V_{SS} in the new circuit regardless of whether the output is high or low. This is the reason for the low power consumption.

IV. Conclusion

A low-power single-input level shifter circuit suitable for implementation using n-channel oxide TFTs with negative values of V_T has been developed. Only a single input signal is sufficient to drive the circuit at as a high frequency as 30 kHz for a TFT V_T range from -5 V to $+1$ V. The output signal remains high and stable when desired, because the switch TFTs connected to the floating node are turned off with negative values of V_{GS}. The power consumption is as low as 0.2 mW for an input signal frequency of 10 kHz because there is no static current between V_{DD} and V_{SS} in the circuit regardless of whether the output is high or low.

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