Oxide Vertical TFTs for the Application to the Ultra High Resolution Display

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Abstract

The ultra-high resolution display is in demand as virtual reality (VA) and augmented reality (AR) displays, and hologram display become much more important. We present vertical TFTs for the application to the driving TFT of ultra-high resolution display. The IGZO deposited by sputtering and InO_x deposited by means of plasma-enhanced atomic layer deposition (PEALD) have been adopted as the channel layers. While the IGZO vertical TFT shows on-current of 0.23 mA at V_g = 5 V and V_{ds} = 2.1 V, that of InO_x TFT shows 1.26 mA at the same driving condition.

Author Keywords

Vertical oxide TFT; Ultra high resolution display; PEALD InO_x

1. Objective and Background

The recent trend in display may be listed as large SHV TV, AMOLED TV, high resolution mobile display, and new display with novel design or function such as flexible transparent display. Very recently high resolution displays become one of the big concerns[1] as virtual reality or augmented reality displays began to penetrate into the real market and hologram display is being developed. The display with resolution higher than 2000 ppi is considered to be achieved as ultra-high resolution displays. The most important factor in the ultra-high resolution display is the pixel area and the smallest TFT size would be the first criteria in the TFT point of view.

The back channel etch (BCE) TFT[2] and self-aligned (SA) TFT[3] have been used for driving high resolution LCD and OLED, respectively. The comparison of foot print of TFT in Figure 1, however, shows that vertical TFT has the smallest pixel pitch value. In addition, vertical TFT can have precisely controlled short channel length defined by not the lithography instrument but the thin film thickness of spacer, resulting in high and uniform on-current. The paradoxical advantage of vertical TFT would be increasing channel length longer than the sub-pixel length. This would be the most important advantage of vertical TFT for the application to the high resolution display since properly designed vertical TFT allows high current gain at proper driving voltage which be decided from the threshold voltage of LCD or OLED device.

Among the TFTs, oxide TFTs have been intensively researched due to the stellar performances of mobility and stability, large area

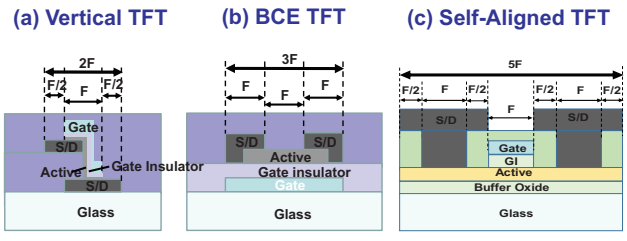

Figure 1. Comparison of minimum feature size and cross section of (a) vertical TFT, (b) BCE TFT, and (c) self-aligned TFT

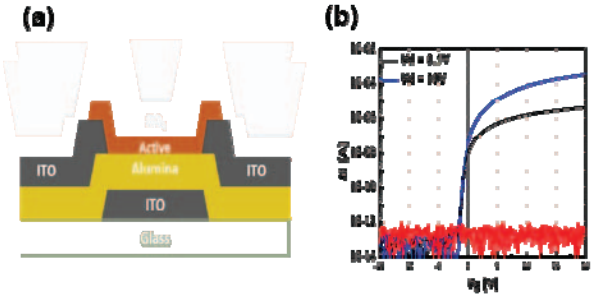

Figure 2. Characteristics of bottom-gate bottom-contact oxide TFT with polycrystalline InO_x

uniformity, and use of existing facility[4-5]. Furthermore, architecture, materials, and process for the oxide TFT can be carefully selected depending on the device application. One of the most beautiful advantages of oxide TFT would be that it does not show short channel effect even with the channel length shorter than sub-micrometer[6-7]. This makes oxide semiconductors very suitable for the channel material of vertical TFT. Furthermore, considering the main issue in the vertical TFT, step coverage of active layer, oxide TFT would be the best selection since oxide semiconductor and gate insulator of alumina[8] or SiO_2[9] used for the oxide TFT can be deposited by means of plasma-enhanced atomic layer deposition (PEALD). PEALD provides excellent step coverage of films with excellent dielectric properties.

There are many issues in the fabrication of vertical oxide TFT such as device structure, contact resistance between the source/drain (S/D) and active layer, leakage current of gate insulator and active layer, thickness control of active film, back channel effect, and unavoidable overlap capacitance between gate and S/D with thin gate insulator.

As a starting step of the research, we report the performance of vertical oxide TFTs with IGZO and InO_x active layers deposited by off-axis RF sputtering and PEALD, respectively. The main purpose of this research is to verify the feasibility of active layer processes for the vertical TFT. While vertical IGZO TFT shows on-current of 0.23 mA at V_g = 5 V and V_{ds} = 2.1 V with S.S of 0.12 V/dec., that of InO_x TFT shows 1.26 mA at same condition with S.S of 0.14 V/dec. This shows the promise of oxide vertical TFT applicable to the ultra-high resolution display.

2. Experiments

Before fabrication of vertical TFT, we optimized the PEALD process for InO_x oxide semiconductor. Indium oxide films are deposited using $Et_2InN(SiMe_3)_2$ provided by UP chemical Co., Ltd and oxygen plasma as the precursors of In and oxygen, respectively. The Sequence of depositing indium oxide consists of sourcing indium precursor to the reactor chamber, Ar purge, oxygen plasma, and Ar purge at working pressure of 3 torr and plasma power of 100 W.

The thickness of films on Si(100) substrates were determined using J.A. Woolam Co. Alpha-SE ellipsometer. The crystallinity

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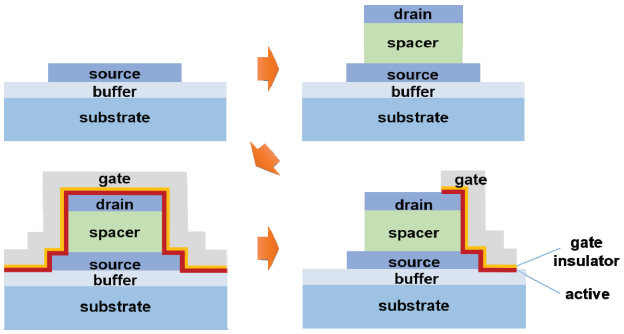

Figure 3. Process flow for fabrication of vertical TFT

of the films were clarified by X-ray diffraction (XRD) patterns with theta/2theta scan mode using Cu Kα X-ray source. Prior to fabricating vertical TFT, we applied PEALD grown InO_x film to the active layer of the bottom-gate bottom contact (BGBC) TFT as shown in Figure 2(a). At first, the prepared 150 nm-thick ITO glass was patterned as a gate and Al_2O_3 film was deposited as a gate insulator. After depositing and patterning source/drain ITO by wet etching, PEALD-InO_x was grown to 5 nm-thick. Deposited InO_x films were patterned, followed by annealing at the temperature of 350°C under O_2 condition. As a final step, the devices were completed with the deposition of silicon oxide layer on the indium oxide channel as a passivation layer to ensure stable operation before post-annealed at 300°C under vacuum. The electrical characteristics of InO_x TFTs were analyzed with transfer curves by HP 4156A. The electrical parameters such as field effective mobility, turn-on voltage, and sub-threshold swing could be obtained from those curves.

The process sequence of vertical oxide TFT is shown in Figure 3. After deposition of buffer layer of SiO_2, 150 nm-thick ITO source electrode was deposited onto buffer layer by RF sputtering and patterned by wet etching process using mixed acid. The 500 nm-thick spacer of SiO_2 which was deposited by PECVD using SiH_4 and N_2O plasma, followed by 150 nm-thick ITO drain electrode by RF magnetron sputtering. With photo-mask of drain, ITO and SiO_2 spacer were etched sequentially by means of wet and dry etching. After deposition of active layer (IGZO-sputter, InO_x-PEALD), a 20 nm-thick Al_2O_3 was deposited by PEALD, followed by Mo gate electrode deposition by DC sputtering. These active/GI/gate layers were patterned at once by wet etching. After depositing passivation film of SiO_2, gate and S/D via was formed at once with wet etching. The annealing was performed at 300°C under vacuum.

3. Results and Discussion

The BGBC structure shown in Figure 2(a) is very efficient in optimizing the active layer process. We can confirm TFT performance very easily by splitting deposition of active layer

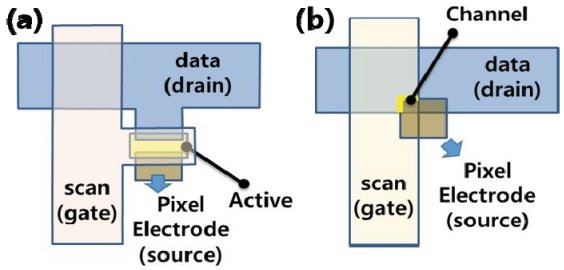

Figure 4. Pixel layout using (a) BCE TFT and (b) vertical TFT

Figure 5. Cross-sectional SEM image and optical image of top view of VTFT fabricated using InO_x.

process on top of the ITO S/D, followed by passivation layer formation. The InO_x film deposited by PEALD has higher carrier concentration with nano-crystalline structure compared with other IGZO based semiconductor, indicating possibility of high mobility. However, it is still very important to control the whole carrier amounts in the semiconductor film, so that we needed to optimize carrier amounts by modification of active film thickness. Figure 2(b) displays the transfer characteristics of optimized InO_x TFT at drain voltage of 0.1 V and 10 V. The mobility of InO_x TFT is 37 cm^2/Vs. Although sputtered amorphous oxide semiconductor TFTs are well known to have high mobility, it is also certain that PEALD-InO_x TFTs exhibited excellent electrical performance even with poly-crystalline phase. We applied PEALD-InO_x film to the vertical TFT. Since there is no contact issue between the ITO S/D and InO_x active layer in BGBC structure, we applied this ITO electrode as the S/D layers in the vertical TFT.

As shown in Figure 3, one of the merits of vertical TFT is the simple fabrication process (only 3-masks are used). Another advantage of vertical TFTs is that the foot print of channel region in the array can be extremely small compared with plane channel TFTs (for example, BCE TFT) as shown in Figure 4(a) and (b). The layout shown in figure 4(b), which will be adopted for the array process, is used for the evaluation of vertical TFT. Figure 5 shows cross-sectional SEM image of vertical TFT and optical image of top view of TFT fabricated using InO_x. Due to the superior step coverage of PEALD grown films, it shows uniform film formation even at the area of vertical channel region.

Although InO_x TFT shows high mobility in BGBC structure with low off-current, we need to secure low off-current level even in the vertical TFT with extremely short channel length. Therefore, we also applied low mobility IGZO semiconductor as the channel layer

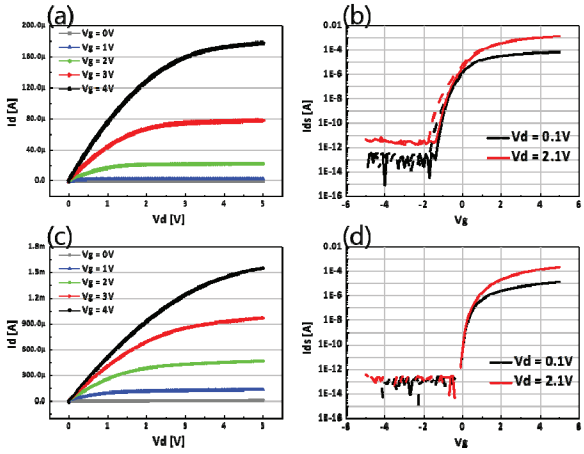

Figure 6. (a) Output and (b) transfer characteristics of IGZO vertical TFT, and (c) output and (d) transfer characteristics of InO_x vertical TFT

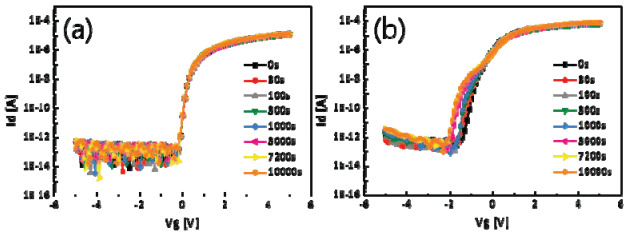

Figure 7. (a) V_{th} shift of IGZO and (b) InO_x vertical TFT under +0.75 MV/cm bias stress

of the vertical TFT. Ternary semiconductor IGZO film was deposited by sputtering. To make sure conformal film deposition of IGZO in vertical structure, we used off-axis sputtering system, which was verified to show good step coverage of the film.

Figure 6 shows transfer and output characteristics of IGZO TFT and InO_x TFT. Although sputtering system used for the mass production would not have good step coverage, our sputter yielded good coverage due to the off-axis design with circulation. As expected, vertical TFT fabricated by sputter also shows good transfer behavior with the mobility of 3.43 cm^2/Vs, S.S of 0.12 V/dec., and on/off ratio of 10^8. Even though the gate insulator thickness is very thin to enhance the effect of gate field, the gate leakage current is very low. Furthermore, the off-current level is also very low even at high V_{ds} in the case of low mobility IGZO TFT. The mobility, however, is too deteriorated from 19.6 cm^2/Vs in BGBC TFT to 3.43 cm^2/Vs in vertical TFT. Similar to the IGZO TFT, the InO_x vertical TFT also shows degradation of mobility from 37 cm^2/Vs in BGBC TFT to 13.2 cm^2/Vs in vertical TFT. Considering the large capacitance of gate insulator, the swing value of vertical TFT is relatively large value of 0.14 V/dec.

The thickness of InOx film is just 5 nm to control the carrier amount. We doubt severe back channel effect in InO_x as well as the F incorporation effect. We doubt firstly, back channel effect in vertical TFT. The back channel of SiO_2 film is formed after dry etching of spacer, SiO_2. During the dry etching process using florin based etching gas, defects can be generated on the surface of SiO_2. Furthermore, the surface of SiO_2 back channel after dry etching is not that flat, showing large surface roughness. This would result in larger effective channel length than the mask dimension. Additionally, over etching of both source and drain electrode via wet process also contribute to the longer channel length. Secondly F doping into the active layer could be one of the origin of the deterioration of the TFT performance. According to the SIMS analysis, F residue on the surface of the back channel are incorporated into the active layer after thermal annealing. Then, it did affect the electrical performance of semiconductor film. We are under investigation of origin of the reduced mobility of vertical TFTs compared with those in BGBC TFTs.

The InO_x vertical TFT with relatively higher mobility than IGZO TFT shows more negative shifted Von value with higher off-current level than those of IGZO TFT. Depending on the application of vertical TFT, it seems to be necessary to control the mobility of active layer to obtain high on-off ratio with reasonable Von value.

In the case of IGZO TFT, except the mobility decrease, bias stress stability is very good and negligible V_{th} shift is occurred after 3 hours stress under positive gate field of +0.75 MV/cm (Figure 7). Meanwhile, InO_x vertical TFT shows negative V_{th} shift under positive bias stress. Under negative bias stress, it shifts negative way. This behavior cannot be ascribed to the InO_x semiconductor in vertical TFT structure since similar results were also observed in BGBC structure. It is reported that negative V_{th} shift under positive gate bias is because of H migration from the gate insulator. We are also investigating the origin of the instability under positive bias stress.

4. Impact

We report vertical TFTs with IGZO active layer deposited by sputtering and InO_x semiconductor deposited by PEALD for the application to the ultra-high resolution display. Scale down effect of oxide TFT such as negative Vth shift and gate leakage induced by thinning of gate insulator are not observed. High on-current and excellent bias stress stability demonstrate that vertical oxide TFT fabricated using the processes applicable to the array are very suitable for the ultra-high resolution display driving.

5. Acknowledgements

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