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Upside–Down Annealing of Oxide Thin-Film Transistors and its Analysis Using Hydrogen-Diffusion Model

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Hydrogen plays a crucial role in controlling the electrical characteristics of oxide thin-film transistors (TFTs). The conductivity of the semiconductor can be modulated by controlling the amount of hydrogen in the active layer. In this study, a thermal annealing of the sample in an inverted orientation (referred to as "upside-down annealing") is introduced. The impact of this approach on the hydrogen content within the In_2O_3 active layer is examined through the lens of a hydrogen diffusion model. By time-of-flight secondary ion mass spectrometry analysis, a hydrogen diffusion model for the TFT is established, and it is demonstrated that upside–down annealing is an effective method for preventing hydrogen depletion caused by out-diffusion. A bottom-gate bottom-contact TFT is fabricated to analyze electrical characteristics. By employing different post-thermal annealing methods on the device, it is discovered that the upside–down annealing enhances the device's performance significantly up to mobility of 22.3 $cm^2 V^{-1} s^{-1}$, which surpasses more than twice the mobility achieved with the traditionally oriented, "straight" annealed TFT.

1. Introduction

Oxide thin-film transistors (TFTs) are a focal point of extensive research due to their remarkable ability to exhibit high mobility, large-area uniformity, and a superior on/off ratio.[1] With mobility values surpassing 10 times those of amorphous silicon (a-Si) TFTs, oxide TFTs present a compelling option for advanced electronic applications. These TFTs play a pivotal role in backplane devices and next-generation displays, leveraging their exceptional characteristics to advance display technologies and enhance the performance of electronic devices.[2]

In the context of oxide TFTs, hydrogen plays a significant role in various bonding states within the device.[3] Hydrogen is particularly relevant to its role as a shallow donor when present at more than a defined threshold of 10^{20} cm^{-3} for indium-based semiconductors.[4] Previous investigations have demonstrated that when the hydrogen content surpasses this critical level, it actively provides an electron to the device. Thus, effectively managing the number of hydrogen atoms within the active layer is pivotal in attaining high-mobility TFTs with acceptable V_{on}[5] and emphasizing the importance of observing hydrogen behavior as a shallow donor. This observation underscores the need for a meticulous examination of hydrogen's impact on the performance of oxide TFTs to enhance our understanding of these systems.

Thermal annealing of the device in a vacuum environment has several impacts on TFT performance, such as an increase in film density, oxygen vacancy carrier control, passivation of defects, etc.[6] These improvements play a crucial role in enhancing overall TFT performance.

Despite its diverse advantages, post-thermal vacuum annealing has a noteworthy drawback. This drawback stems from the out-diffusion of hydrogen from the active layer into the vacuum atmosphere. The extent of hydrogen out-diffusion surpasses the in-diffusion from the bottom gate insulator (GI), as evidenced by the hydrogen depth profile in **Figure 1**.[7] This out-diffusion degrades mobility since hydrogen functions as a shallow donor and defect passivator within oxide semiconductors.

Researchers commonly implement a strategy to mitigate out-diffusion by applying a protective/passivation layer atop the device, where the active layer is exposed.[8] The layer works as a barrier against hydrogen diffusion during subsequent annealing, thereby retaining shallow donor concentration within the active layer. This precautionary measure is a requirement for maintaining the integrity and performance of the device after vacuum annealing.

Our research extends beyond conventional strategies as we seek to utilize hydrogen diffusion to enhance device performance. We introduced an innovative approach to suppress hydrogen out-diffusion: the vacuum annealing of the TFT device in an inverted orientation. We have coined this technique "upside-down annealing" in contrast to the traditional annealing method, referred to as "straight annealing" in this letter. Note that a silicon wafer was placed under the device during upside–down annealing to prevent contamination from the furnace surface, as shown in **Figure 2**. Through this novel approach, we successfully reduced the out-diffusion of hydrogen. An In_2O_3 TFT with upside–down annealing showed a high-mobility performance and reduced hysteresis compared to the conventional, straight-annealed TFT. This novel annealing technique holds a potential for valuable insights into optimizing the performance of oxide TFTs.

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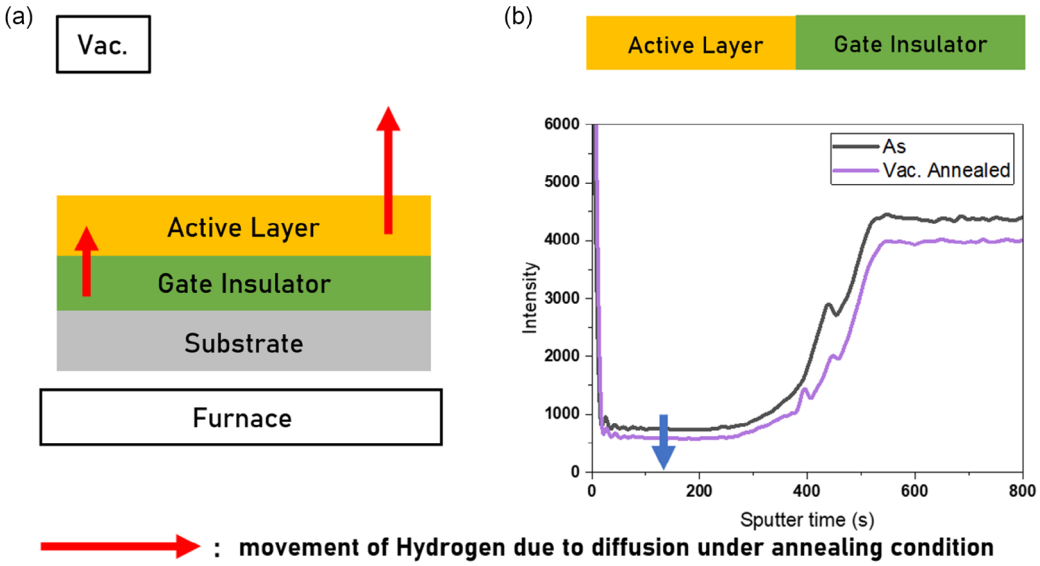


Figure 1. a) Simplified schematic of a BGBC type oxide TFT without passivation layer annealed in vacuum, red arrows represent the diffusion of hydrogen; b) hydrogen depth profile showing the decrease of hydrogen due to out-diffusion.

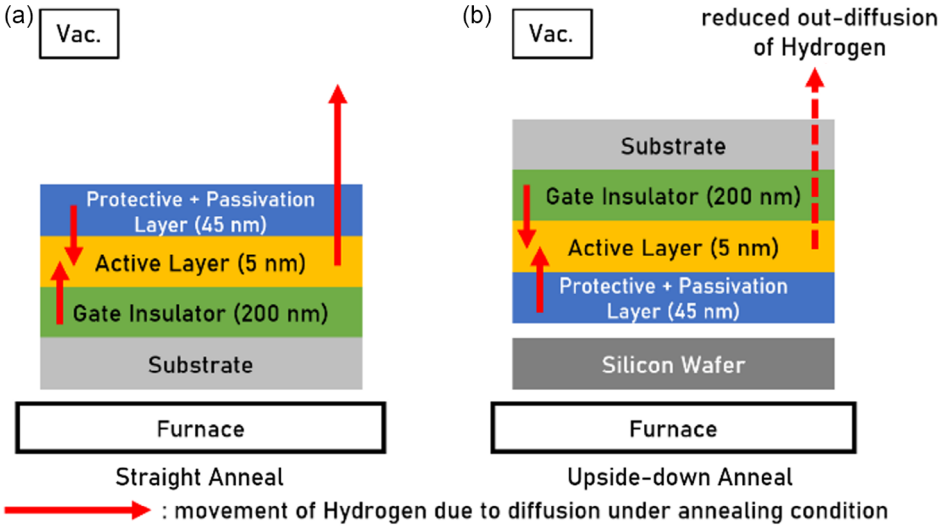


Figure 2. Cross-sectional diagram of BGBC-structured TFT device annealed in vacuum by two methods: a) straight anneal and b) upside–down anneal.

2. Experimental Section

We fabricated TFT devices with bottom-gate-bottom-contact (BGBC) structure. The width and length of the channel were 40 and 20 μm, respectively. **Figure 3** shows a schematic of the fabricated oxide TFT. InSnO (ITO) on glass substrate was used as the gate electrode. Next, 200 nm thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. For the source/drain electrodes, 150 nm thick ITO was deposited by sputtering, followed by vacuum annealing at 250 °C for 2 h. To maximize the effect of hydrogen shallow donors, we chose In_2O_3, a high-mobility oxide semiconductor as the active layer. The 5 nm thick In_2O_3 was deposited by plasma-enhanced atomic

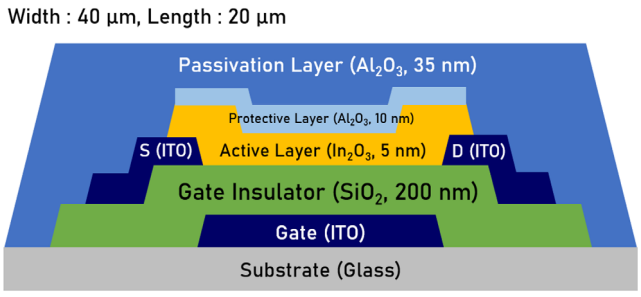


Figure 3. Schematic of BGBC TFT used in research.

layer deposition (PEALD) at 200 °C. Without breaking vacuum, a 10 nm thick Al_2O_3 protective layer (PL) against channel contamination from chemical exposure was deposited by PEALD at 200 °C.[9,10] The PL was patterned in conjunction with the active layer. For the passivation layer, 35 nm thick Al_2O_3 was deposited by the same methods with the PL. Al_2O_3 is widely used for passivation in oxide TFTs. It has a superior hydrogen barrier capacity due to its chemical inertness and low hydrogen permeability.[11] All layers were patterned through photolithography and wet etching. After device fabrication, we split the annealing methods into three groups: as fabricated, straight annealed, and upside–down annealed. The devices were first annealed in vacuum at 200 °C for 2 h, and were subsequently annealed at higher temperatures of 220 and 250 °C. Electric performances of TFT were measured using a probe station. Hydrogen depth profiles were obtained by time-of-flight secondary ion mass spectrometry (ToF–SIMS) analysis.

The samples for SIMS measurements were fabricated to mimic the stacking structures of the TFT devices. The substrate was changed from glass to silicon wafer, the thickness of Al_2O_3 protective/passivation layer decreased to 10 nm, and the thickness of In_2O_3 was increased to 20 nm for clearer depth profile results. The annealing conditions of SIMS samples were also split into three groups, as in TFTs.

3. Results

Figure 4 displays the transfer curves of the devices under each annealing condition. In the as-fabricated state, the device did not show a transfer characteristic. However, after annealing at 200 °C by both straight and upside–down methods, the devices showed clear transfer characteristics. The linear mobility of upside–down annealed device was twice as higher than straight annealing. The hysteresis and subthreshold swing were smaller, indicating an improvement in device performance.

This trend of electrical performances remained after cumulative vacuum annealing at 220 and 250 °C for 2 h. The results are shown in **Figure 5**, indicating that the upside–down annealed device performs better across all temperature ranges. From these results, we can see that upside–down annealing has positive impacts on TFT devices, with higher mobility and lower hysteresis.

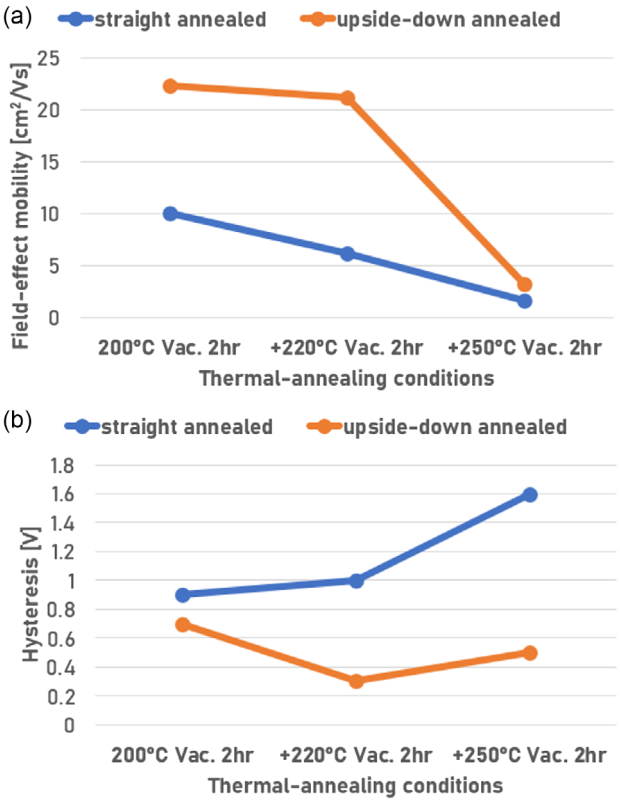
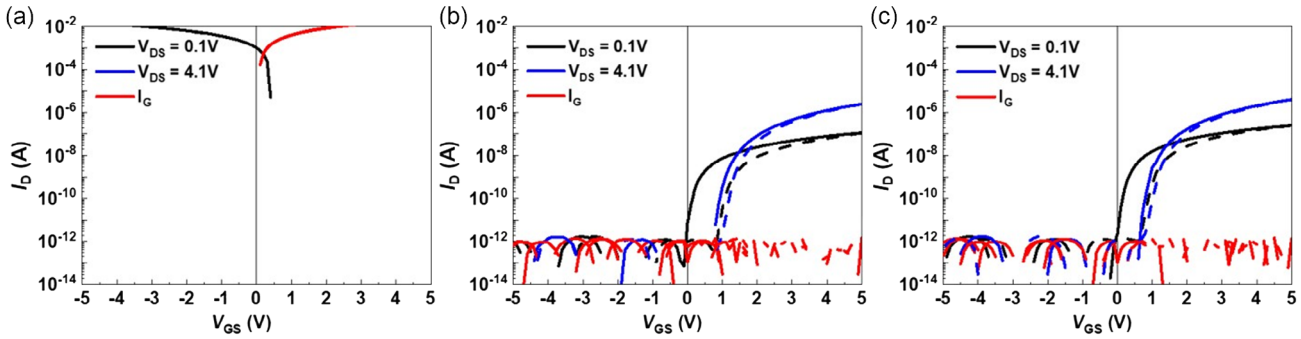


Figure 5. Electrical performance result: a) mobility and b) hysteresis, after cumulative annealing the device.

4. Discussion

To determine the origin behind this phenomenon, we analyzed the resulting hydrogen depth profile of each annealed sample by ToF–SIMS. The hydrogen depth profile of the upside–down



S.S	Von	Hys	μ_lin	μ_sat
No transfer curve drawn				

As Fabricated

S.S	Von	Hys	μ_lin	μ_sat
0.118	0	0.9	10.033	10.271

200°C Straight Annealed

S.S	Von	Hys	μ_lin	μ_sat
0.079	0	0.7	22.338	15.933

200°C Upside-down Annealed

Figure 4. Transfer curve of fabricated TFT device with differed annealing condition: a) as fabricated, b) straight-annealed, and c) upside–down annealed.

annealed sample is shown in **Figure 6**a as the blue line. We observed two significant features from the profile. The first is a notable reduction in hydrogen content, particularly in the gate insulator region.

Figure 6b indicates this more clearly, illustrating the overall decrease in hydrogen content within the active layer. From this, we can infer that the desorption of hydrogen, caused by the out-diffusion of hydrogen to the vacuum, plays a significant role in hydrogen movement during annealing. Another noteworthy observation is that the straight-annealed sample exhibits a higher average hydrogen content within the active layer than the upside–down annealed sample. We attributed this to prior research findings regarding aluminum oxide's superior hydrogen barrier properties compared to other oxide materials.[12] As a result, more hydrogen escaped through the silicon oxide and into the silicon wafer during upside–down annealing. The second is a leftward shift of the hydrogen depth profile. We suspected this as the primary reason of increased mobility.

We used highly conformal atomic layer deposition for the upper layers. However, for more accuracy in interpreting depth profiles, we determined the boundaries of each oxide thin film. Following the method outlined in a ToF–SIMS study,[13] we set the cross-points of normalized content of O, Si, Al, and In as the interfaces between layers. **Figure 7**a depicts these resulting interfaces as black-dashed lines in the case of upside–down annealed sample. We also marked this boundary inside the hydrogen depth profile in the same position. Figure 7b is a result of this process which is an example of upside–down annealed sample. This process was performed for all three oxide samples.

One notable point is that within the active layer, silicon atoms are present to some extent at the interface. As shown in red line of Figure 7a, we confirmed the presence of silicon around sputtering time of 600 s in the SIMS depth profile. In this article, we refer to the region in the active layer where silicon is present as the silicon existing zone. Indium in the active layer plays a crucial role in achieving high mobility in oxide semiconductors due to

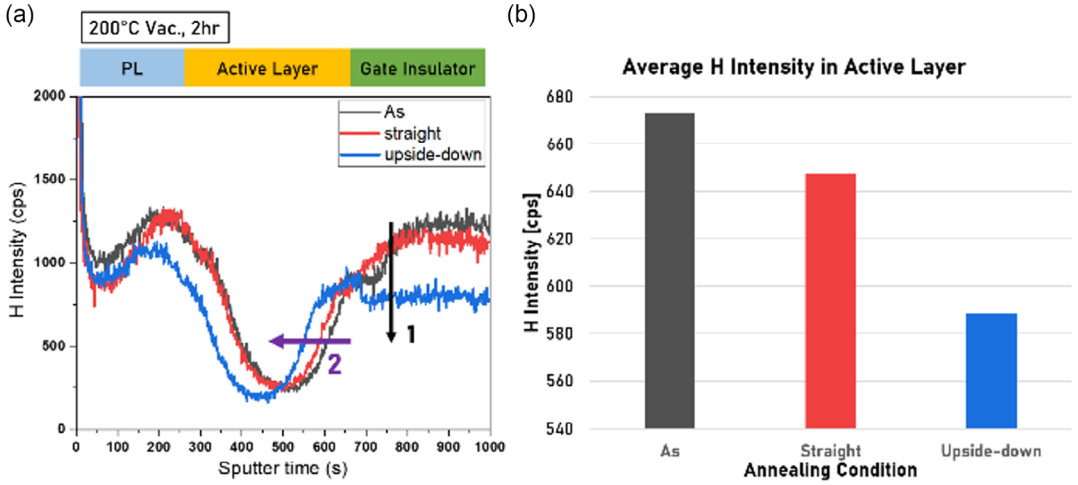


Figure 6. a) Hydrogen depth profile data by SIMS analysis and b) average hydrogen intensity in active layer.

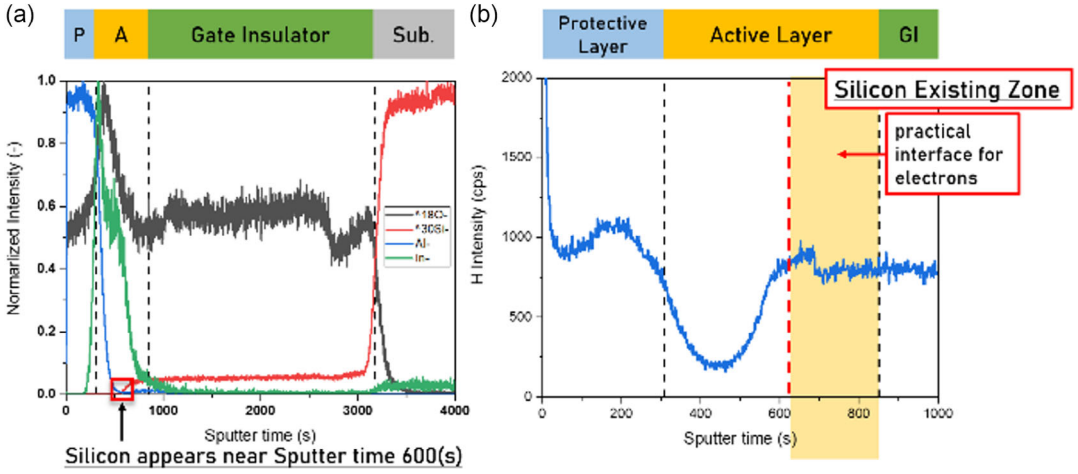


Figure 7. a) SIMS depth profile of silicon (red) indicating the starting point of silicon existing zone. b) Highlight of silicon existing zone inside an active layer which shows an insulator-like behavior.

orbital overlapping.[14] However, in this region, the contribution of indium to high mobility is limited by silicon atoms. Consequently, the boundary of the silicon existing zone serves as a practical interface for electrons.

Figure 8a shows the modified depth profile with interfaces obtained earlier. The leftward shift of the hydrogen depth profile remained in the standardized graph. Due to the leftward shift of the hydrogen distribution, the most significant difference in hydrogen content was found near 20 nm in depth. This is the region next to the interface of silicon existing zone. As shown in Figure 8b, the upside–down annealed sample exhibits the highest hydrogen content in this highlighted region, despite having the lowest average hydrogen content among the samples.

Figure 9 illustrates this in detail from the perspective of electrons. When a positive voltage is applied to the gate, an electric field is induced in the gate insulator, creating dielectric dipoles. Electrons within the oxide semiconductor are influenced by this electric field, building a channel region where current can flow. However, as mentioned earlier, within the silicon existing zone, the behavior of electrons is more akin to that of inside of insulator. Therefore, carriers tend to exist outside this zone, making an effective channel right next to it. We suspected that this is the channel region, the part that has the most impact on device performance. Also, from Figure 8a, we could find that this region is where the hydroxyl (OH–) peak is present. Previous research indicates that this OH– peak results from an unstable distribution of atoms at the interface to contribute to interface trap sites.[15] Also, it has established that hydrogen can passivate such trap sites by diffusion during high-temperature annealing.

Based on these observations, we established a hydrogen diffusion model. **Figure 10**a shows how hydrogen out-diffusion is suppressed by Al_2O_3 PL in the straight-annealed case. Since the PL is in situ deposited on the active layer, there are smaller amounts of interface trap sites. However, the channel region doesn't exist on the interface of these oxides, making the hydrogen diffusion between these oxides less influential to the electrical performance of the device.

Figure 10b,c displays the hydrogen movements between the active layer and GI during straight and upside–down annealing,

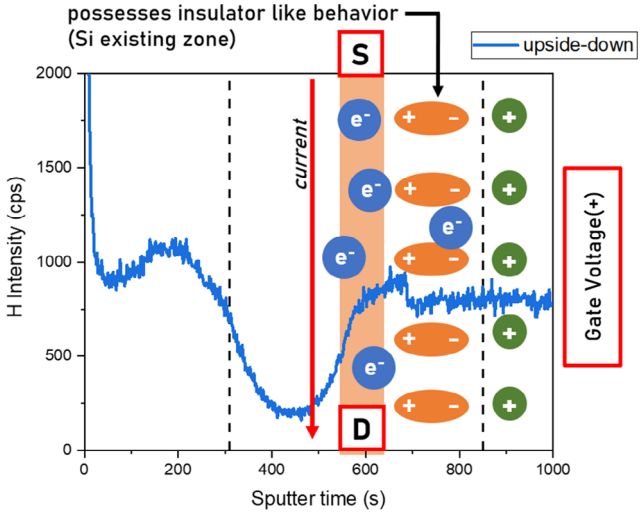


Figure 9. Movement of electrons when positive voltage is applied to the gate showing electrons stacked at the channel region.

respectively. Unlike the interface between PL and active layer, the hydrogen distribution on this region brings significant impact to the device's mobility because the channel region is formed between these oxides. Analysis from SIMS data revealed a higher hydrogen content within the GI, leading to an in-diffusion from the GI to active layer due to the concentration differences. The orientation difference results that this hydrogen in-diffusion flux points upward in the straight-annealed case. Meanwhile, it points downward in the upside–down annealed case. Simultaneously, out-diffusion into the vacuum takes place mainly in the upward direction due to the vacuum environment formed above the TFT while annealing. Consequently, in the straight-annealed sample, it is easier for the hydrogen to pass from the GI to the active layer, where both out-diffusion flux and in-diffusion flux points the same up-ward direction. In contrast, in the upside–down annealed sample, the hydrogen out-diffusion flux encounters extensive resistance as the in-diffusion flux between the GI

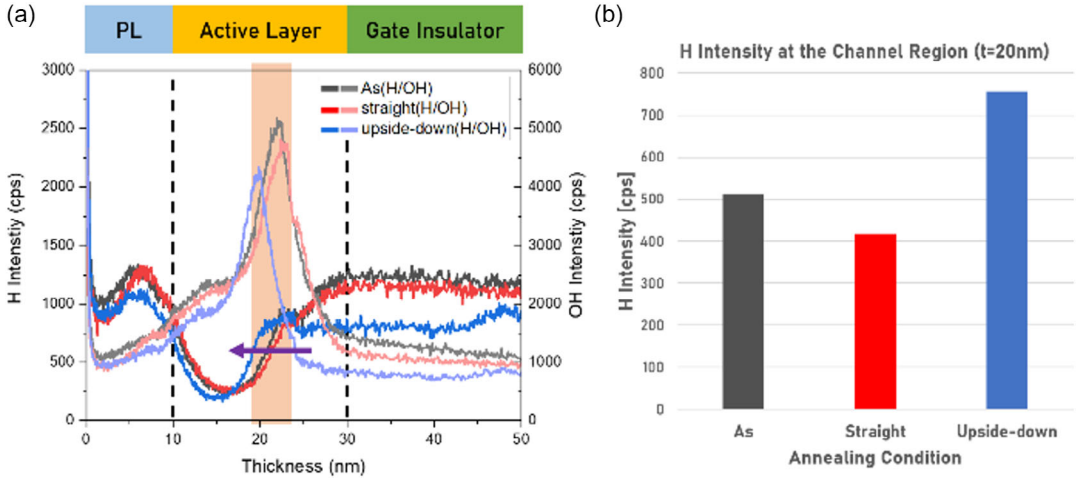


Figure 8. a) Highlight of channel region inside an active layer which coincides with the OH peak; b) the hydrogen intensity at this channel region specifically where thickness = 20 nm point in hydrogen depth profile.

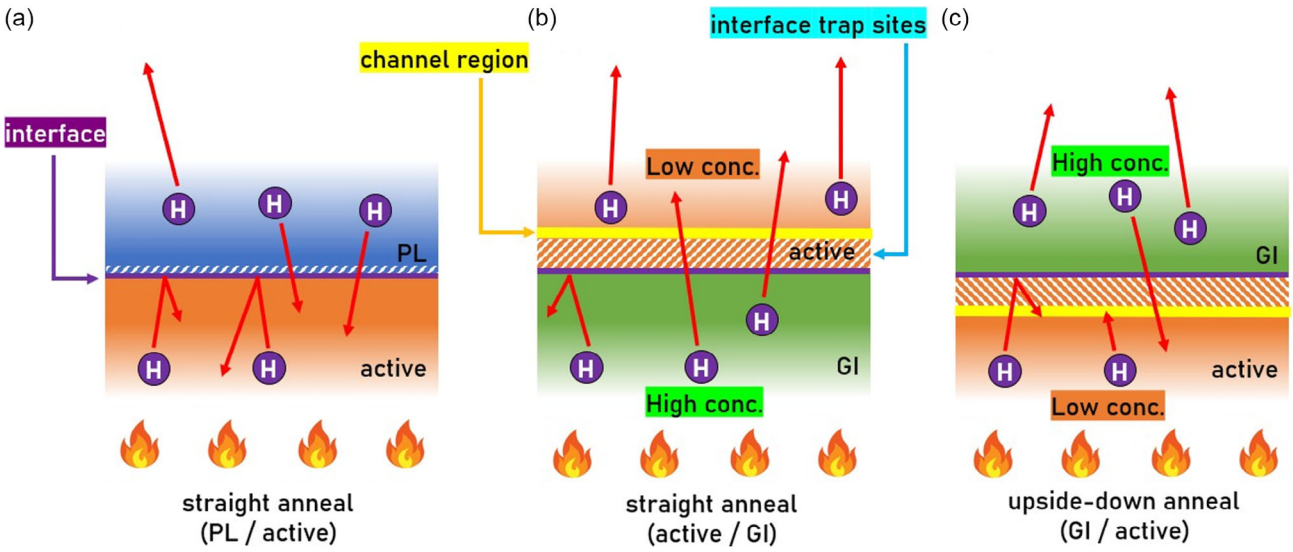


Figure 10. Hydrogen-diffusion model inside oxide layers of TFT, depicted between a) PL and active, b) active and GI layers during straight annealing, and c) GI and active layers during upside-down annealing.

and active layer is pointing in the opposite direction, blocking the desorption of hydrogen at the interface between the two oxides. This is why more hydrogen, passing through the interface traps, accumulates in these interface trap sites during upside–down annealing.

As a result, the upside–down annealed sample exhibits higher hydrogen content near the center of the active layer, primarily due to the hydrogen stacking in the interface trap sites. The passivation of these trap sites by hydrogen reduces trap density effectively to enhance the stability of the TFT and to reduce the hysteresis. Furthermore, since the stacked region also corresponds to the channel region, the increased presence of hydrogen, acting as a shallow donor, results in higher carrier mobility.

5. Conclusions

Our research on upside–down annealing has yielded remarkable results, yet it still needs several improvements. First, additional experiments and data from TFTs with different structures and material compositions will be required to establish upside–down annealing as a universally applicable method for the enhancement of TFT performance. Second, more precise surface analysis methods that could overcome the limitations of SIMS measurement are necessary. Lastly, the incorporation of supplementary analysis methods, such as investigating trap densities and hydrogen bonding states, will complement our interpretation of the hydrogen-diffusion model.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

hydrogen diffusions, interface trap sites, oxide thin film transistors, secondary ion mass spectrometries, vacuum annealings

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