Comparative Study on Light-Induced Bias Stress Instability of IGZO Transistors With SiN_x and SiO_2 Gate Dielectrics

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***Abstract*—This letter examines the effect of the gate dielectric material on the light-induced bias-temperature instability of an In–Ga–Zn–O (IGZO) thin-film transistor (TFT). After applying positive and negative bias stresses, the SiN_x-gated TFT exhibited inferior stability to the SiO_2-gated TFT, which was explained by the charge trapping mechanism. However, light illumination under a negative bias stress accelerated the negative displacement of the threshold voltage (V_{th}) of the SiN_x-gated IGZO TFT compared to that of the SiO_2-gated TFT. This was attributed to the injection of photocreated hole carriers into the underlying gate dielectric bulk region as well as the hole trapping at the gate/channel interface.**

***Index Terms*—a-InGaZnO, amorphous semiconductor, bias stability, multicomponent oxide semiconductor, thin-film transistors (TFTs).**

I. Introduction

RECENTLY, In–Ga–Zn–O (IGZO) thin-film transistors (TFTs) have attracted considerable interest for applications to the active-matrix (AM) backplane of LCD and OLED displays [1]–[4]. Although high-performance IGZO TFTs have been fabricated, light- and bias-induced instability is still a critical issue to be resolved because the exposure of the switching transistor to backlight or ambient light would be inevitable during the operation of the display panel. In this regard, there have been several reports, including the effect of moisture [5], device configuration [6], and channel cation composition [7], on the light-induced bias instability. However, there are no reports of the effect of the gate dielectric material on the photoreliability of IGZO TFTs. This letter reports the degradation mechanism of the threshold voltage (V_{th}) under photon-irradiated gate bias stress conditions for IGZO TFTs. In particular, the impact of the different gate dielectrics on the light-induced bias-thermal instability of IGZO TFTs was investigated. The fabricated device had SiN_x and SiO_2 films as a gate dielectric due to their large area scalability in flat panel AM displays.

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II. Experimental Procedure

A 200-nm-thick SiN_x film as a gate dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on a patterned Mo (2000-nm-thick)/glass substrate at 380 °C. An a-IGZO film, 50 nm in thickness, was grown by dc sputtering at room temperature. After defining the IGZO channel using photolithography and wet etching, a 200-nm-thick SiO_2 etch stopper was deposited by PECVD and patterned by dry etching to define the source/drain contact hole. A Mo source/drain electrode (200 nm) was formed using a conventional sputtering system and patterned by photolithography and dry etching.

The fabricated TFTs had a bottom-gate and top-contact configuration [3]. For comparison, a PECVD-derived SiO_2 film as a gate insulator was also deposited before active channel deposition. The thickness of the SiO_2 gate insulator was designed to be 120 nm to have a similar gate capacitance: The gate capacitances per unit area of the SiN_x- and SiO_2-gated devices were 2.66×10^{-8} and 2.88×10^{-8} F/cm^2, respectively. Finally, the samples were subject to thermal annealing at 350 °C for 1 h. The electrical measurements were carried out in air using an Agilent B1500 A precision semiconductor parameter analyzer.

III. Results and Discussion

Fig. 1(a) and (b) shows the transfer characteristics of the IGZO TFTs with SiN_x (device A) and SiO_2 (device B) as a gate insulator ($W/L = 24/10\ \mu$m), respectively. The μ_{FE} value was calculated from the maximum transconductance ($\mu_{FE} = Lg_m/WC_iV_{DS}$, where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively) [4]. The threshold voltage (V_{th}) was determined by adjusting the gate voltage, which induces a drain current of $L/W\times$ 10 nA at a V_{DS} of 15.1 V. In addition, the subthreshold gate swing [$SS = dV_{GS}/d\log I_{DS}$ (V/dec)] was extracted from the linear portion of the $\log(I_{DS})$-versus-V_{GS} plot. Device A exhibited a μ_{FE} of

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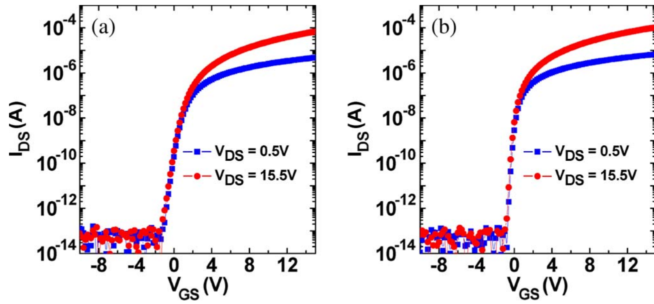

Fig. 1. Transfer characteristics of a-IGZO TFTs with a bottom-gate and top-contact structure ($W/L = 24/10\ \mu$m). (a) SiN_x-gated device (device A). (b) SiO_2-gated device (device B).

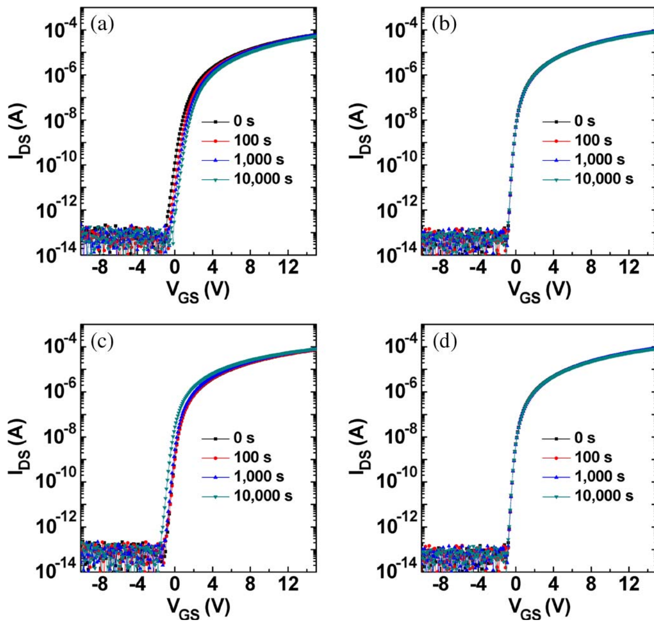

Fig. 2. Evolution of the transfer characteristics of (a) device A and (b) device B with increasing PBS time under the dark condition. Evolution of the transfer curves of (c) device A and (d) device B with increasing NBS time under the dark condition.

13.7 ± 0.08 cm^2/V · s, SS value of 0.38 ± 0.01 V/dec, $V_{\rm th}$ of 0.7 ± 0.17 V, and $I_{\rm ON/OFF}$ ratio of $> 10^9$. On the other hand, device B showed significantly improved performance: The $\mu_{\rm FE}$ and SS values were enhanced to 16.9 ± 0.12 cm^2/V · s and 0.16 ± 0.006 V/dec, respectively, with a similar $V_{\rm th}$ (0.1 V) and $I_{\rm ON/OFF}$ ratio ($> 10^9$). The device performance reported herein is comparable to the state-of-the-art characteristics for the IGZO TFTs with various novel gate insulators, including Y_2O_3 [2], Al_2O_3 [8], and ZrO_2 [9].

Fig. 2(a) and (b) shows the evolution of the transfer curve as a function of the applied positive gate bias stress (PBS) time for devices A and B, respectively. The devices were stressed under the following conditions: $V_{\rm GS}$ was set to 20 V at room temperature, and the stress duration was 10 000 s. For device A, a parallel $V_{\rm th}$ shift of 0.77 V to a higher voltage with increasing PBS time occurred without an accompanying change in $\mu_{\rm FE}$, SS, and the $I_{\rm ON/OFF}$ ratio. This positive $V_{\rm th}$ shift after the application of the PBS has been attributed frequently to the charge trapping of accumulated electron carriers in the channel region at/near the gate dielectric and channel interface [10], [11]. The ambient effect, such as oxygen or water molecules,

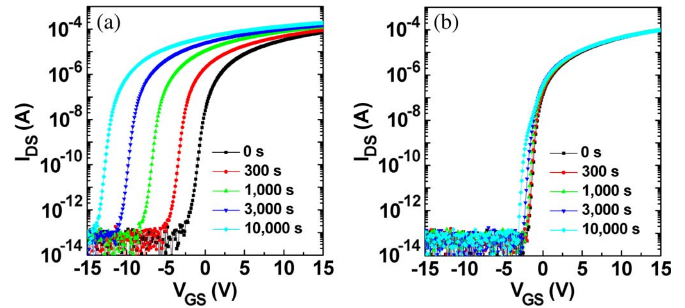

Fig. 3. Evolution of the transfer characteristics of (a) device A and (b) device B with increasing NBS time under white light illumination.

can be excluded because high-quality SiO_2 films (etch stop layer) were coated on the channel region as a passivation layer [12]. The $V_{\rm th}$ stability of the IGZO TFTs under the PBS was improved dramatically by replacing the gate insulator with a PECVD-derived SiO_2 film [see Fig. 2(b)]. A $V_{\rm th}$ shift of only 6 mV was observed for device B after an identical PBS application for 10 000 s. If it is assumed that the $V_{\rm th}$ instability of the IGZO TFTs is due to the charge trapping at/near the gate/channel interface, the interfacial trap density ($N_{\rm it}$) should adversely affect the bias stability. The maximum $N_{\rm it}$ value can be extracted from the SS value ($N_{\rm it} = (SS \log(e)/(kT/q) - 1)C_i/q$, where k is the Boltzmann's constant, T is the absolute temperature, and q is the elementary electron charge) [13], which assumes that there is no semiconductor bulk trap in the IGZO thin film. The calculated $N_{\rm it,max}$ (3.0×10^{11}/cm^2) for device B was much smaller than that (8.9×10^{11}/cm^2) for device A. This lower $N_{\rm it,max}$ for device B would explain why only a negligible $V_{\rm th}$ shift caused by the charge trapping was observed for device B. The effect of the gate dielectric material on the negative gate bias instability of the resulting IGZO TFTs was examined. The devices were stressed under the following conditions: $V_{\rm GS}$ was set to -20 V, and the stress duration was 10 000 s. The application of a negative gate bias stress (NBS) to devices A and B at room temperature caused negative $V_{\rm th}$ shifts of 0.26 and 0.20 V, respectively. At an elevated temperature of 60 °C, the negative movements of $V_{\rm th}$ for devices A and B were increased to 0.53 and 0.29 V, respectively, as shown in Fig. 2(c) and (d). Therefore, the NBS-induced instability of device A was inferior to that of device B at 60 °C and room temperature. This is consistent with the aforementioned charge trapping model. Hole carriers, which may be created in the channel region under NBS conditions, tend to be trapped at the interfacial defect states. Therefore, device A with a larger $N_{\rm it}$ would suffer from a larger charge trapping phenomenon leading to enhanced $V_{\rm th}$ instability.

To double check this interpretation, the TFTs were irradiated with white light during the application of the NBS ($V_{\rm GS} = -20$ V). A white halogen lamp was used as a light source, which consisted of visible light ranging from 400- to 700-nm wavelengths. The intensity of the light source was ~1 mW/cm^2, which was calibrated by photometry. The intensity of 1 mW/cm^2 was chosen to meet the required brightness for the practical application of flat panel displays [14]. Fig. 3(a) and (b) shows the time evolution of the transfer curves for both devices as a function of the light-illuminated NBS condition

for devices A and B, respectively. The inferior stability of the nitride device was manifested more clearly under the light-illuminated NBS condition. Although the V_{th} value for device A was shifted significantly to the negative direction by 11.6 V, device B exhibited only V_{th} movement of -0.78 V. The consistent inferior stability of the TFT with the SiN_x gate dielectric is believed to originate from its higher N_{it} value, which is reconciled with the aforementioned charge trapping model. Under the light-illuminated NBS condition, electron-hole pairs in the channel region would be generated by light. The photocreated electron carrier will be repelled to the back channel surface, whereas the photogenerated hole carriers are attracted to the gate dielectric layer by the negative gate voltage and become trapped at the interfacial trap state. This has been suggested as a plausible explanation for the light-enhanced negative bias instability of oxide TFTs [5], [6]. However, it is not obvious that the approximately 14-fold increase in the amount of the V_{th} movement for device A (device A: $\Delta V_{\mathrm{th}} = -11.6$ V; device B: $\Delta V_{\mathrm{th}} = -0.78$ V) under the light-illuminated NBS condition can be attributed entirely to the approximately three times higher $N_{\mathrm{it,max}}$ of device A. Indeed, the hole carriers near the channel region feel the hole potential barrier (i.e., valence band offset) at the interface between the gate dielectric and channel layer. Interestingly, the valence offset between the SiN_x and IGZO film can be estimated as $\sim$0.15 eV, which is much smaller than ($\sim$2.80 eV) that between the SiO_2 and IGZO film [15], [16]. Therefore, the photocreated hole carriers can be injected easily into the SiN_x gate dielectric due to its lower valence band offset value, which would be partly responsible for the inferior stability of device A. Therefore, the possibility of hole injection into the gate dielectric bulk region cannot be excluded. It is noted that the fast recovery of V_{th} was observed for device A. Without any thermal annealing, device A exhibited a significant recovery of V_{th} by $\sim$8 V after the 10-h exposure to the air ambient, suggesting that most of the photocreated trap states ($\sim$70%) are temporal traps. On the other hand, the 250 °C thermal annealing was found to result in the full recovery of V_{th}, which indicates that the hole carrier injection indeed cannot be neglected.

Finally, we noted that the stretch-out of the subthreshold drain current region was observed for only the SiO_2 device, as shown in Fig. 3(b), suggesting that the light and bias combination stress can create some trap states at the interface between the IGZO and SiO_2. The reason that the SiN_x device did not exhibit such behavior is not clear at this time.

IV. Conclusion

An IGZO TFT with a PECVD-derived SiO_2 gate dielectric exhibited greater bias stability and light-induced bias stability than the device with the SiN_x gate dielectric. This phenomenon has been discussed based on a charge trapping mechanism. Therefore, the SiO_2-gated IGZO TFTs can be implemented as backplane electronics in the next-generation AM flat panel displays.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[2] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, “High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering,” *Appl. Phys. Lett.*, vol. 89, no. 11, p. 112 123, Sep. 2006.

[3] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K. Jeong, Y. G. Mo, and H. D. Kim, “High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper,” *Appl. Phys. Lett.*, vol. 90, no. 21, p. 212 114, May 2007.

[4] J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, “Comprehensive studies on the transport mechanism of amorphous InGaZnO transistors,” *J. Electrochem. Soc.*, vol. 155, no. 11, pp. H873–H877, Sep. 2008.

[5] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, and S. Lee, “The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors,” *Appl. Phys. Lett.*, vol. 95, no. 23, p. 232 106, Dec. 2009.

[6] J.-Y. Kwon, K. S. Son, J. S. Jung, K.-H. Lee, J. S. Park, T. S. Kim, K. H. Ji, R. Choi, J. K. Jeong, B. Koo, and S. Lee, “The impact of device configuration on the photon-enhanced negative bias thermal instability of GaInZnO thin film transistors,” *Electrochem. Solid-State Lett.*, vol. 13, no. 6, pp. H213–H215, Jun. 2010.

[7] J.-Y. Kwon, K. S. Son, J. S. Jung, K.-H. Lee, J. S. Park, T. S. Kim, K. H. Ji, R. Choi, J. K. Jeong, B. Koo, and S. Lee, “Investigation of light-induced bias instability in Hf–In–Zn–O thin film transistor: Cation combinatorial approach,” unpublished.

[8] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X.-H. Zhang, and B. Kippelen, “Low-voltage InGaZnO thin-film transistors with Al_2O_3 gate insulator grown by atomic layer deposition,” *Appl. Phys. Lett.*, vol. 94, no. 12, p. 142 107, Apr. 2009.

[9] J. S. Lee, S. Chang, S.-M. Koo, and S. Y. Lee, “High-performance a-IGZO TFT with ZrO_2 gate dielectric fabricated at room temperature,” *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 225–227, Mar. 2010.

[10] R. B. M. Cross and M. M. De Souza, “Investigating the stability of zinc oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 89, no. 26, p. 263 513, Dec. 2006.

[11] Y. Vygranenko, K. Wang, and A. Nathan, “Stable indium oxide thin-film transistors with fast threshold voltage recovery,” *Appl. Phys. Lett.*, vol. 91, no. 26, p. 263 508, Dec. 2007.

[12] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, “Origin of threshold voltage instability in indium–gallium–zinc oxide thin film transistor,” *Appl. Phys. Lett.*, vol. 93, no. 12, p. 123 508, Sep. 2008.

[13] J. Kanicki and S. Martin, *Thin-Film Transistor*, C. Kagan and P. Andry, Eds. New York: Marcel Dekker, 2003.

[14] P. Gorrn, M. Lehnhardt, T. Riedl, and W. Kowalsky, “The influence of visible light on transparent zinc tin oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 91, no. 19, p. 193 504, Nov. 2007.

[15] Y.-N. Tan, W.-K. Chim, B. J. Cho, and W.-K. Choi, “Over-erase phenomenon in SONOS-type flash memory and its minimization using a hafnium oxide charge storage layer,” *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1143–1147, Jul. 2004.

[16] D.-Y. Cho, J. Song, C. S. Hwang, W. S. Choi, T. W. Noh, J.-Y. Kim, H.-G. Lee, B.-G. Park, S.-Y. Cho, S.-J. Oh, J. H. Jeong, J. K. Jeong, and Y.-G. Mo, “Electronic structure of amorphous $InGaO_3(ZnO)_{0.5}$ thin film,” *Thin Solid Films*, vol. 518, no. 4, pp. 1079–1081, Dec. 2009.