Vertical Channel ZnO Thin-Film Transistors Using an Atomic Layer Deposition Method

Chi-Sun Hwang, Sang-Hee Ko Park, Himchan Oh, Min-Ki Ryu, Kyoung-Ik Cho, and Sung-Min Yoon

***Abstract*— Vertical channel ZnO thin-film transistors (TFTs) were fabricated on glass and flexible substrates. Conformally deposited thin films prepared using atomic layer deposition were used for the active layer, gate insulator, and gate electrode. Owing to the very short channel (0.5 μm) and very thin (20 nm) gate insulator layer, the ON-current of the vertical channel ZnO TFT was 57 μA at the gate and drain voltages of 3 and 4 V, respectively. Vertical channel oxide TFTs may be promising for device applications with low power consumption.**

***Index Terms*— Oxide semiconductor, vertical channel, In-Ga-Zn-O (IGZO), thin-film transistor (TFT).**

I. Introduction

OXIDE semiconductor thin-film transistors (TFTs) are employed as backplane devices for high performance display panels, such as active-matrix organic light emitting diode (AMOLED) televisions and a high-speed driving TFT-liquid crystal display (LCD) panels. Additionally, oxide TFTs can be utilized for various integrated circuit applications. Thus, low operation voltage is one of the most important requirements for achieving good performance of these applications. In general, reducing the driving voltages can be accomplished by scaling down the device geometric factors, such as the thickness of the gate insulator and channel length, which is occasionally performed using electron-beam lithography [1]. The reported work indicated that the oxide semiconductor can be scaled to a very short channel without deteriorating the device performances. However, considering that oxide semiconductors are inexpensive and have large-area compatible processes, it will be better to find a method for achieving low driving voltages with conventional optical lithography machines used for large-area display panels. Vertical channel TFTs (V-TFTs) are proposed as an effective approach to reduce the driving voltage. There have been some investigations of amorphous Si and organic TFTs [2]–[4]. The fabrication of oxide V-TFTs were recently reported [5], [6], in which oxide semiconductors were deposited using sputtering methods. However, sputtering deposition is not suitable for preparing a vertical channel owing to its poor conformality. We have reported highly stable oxide TFTs with Al_2O_3/ZnO gate stacks deposited by an atomic layer deposition (ALD) method [7], [8]. Such features as the high density and excellent electrical properties of thin films could be obtained with ALD methods even at low deposition temperature. Nearly ideal conformal deposition is another merit of ALD. Thus, the ALD method is one of the best ways for preparing thin films for V-TFTs. Consequently, a high current drivability even at a low operating voltage and a small footprint to obtain required drain current would be attractive impacts for the proposed V-TFTs compared with the conventional planar channel TFTs. In this letter, the structure of ZnO V-TFTs and their fabrication procedures are presented. The device performances of V-TFTs fabricated on glass and flexible substrates were evaluated.

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II. Device Fabrication

A 150-nm-thick ITO film was deposited by radio-frequency sputtering at room temperature. After patterning the ITO layer, an Al_2O_3 film (180 nm) was deposited using ALD at 180 °C. Trimethylaluminum and water vapor were used as Al and O precursors, respectively. Another layer of 150-nm-thick ITO was deposited on the Al_2O_3 layer. The bilayered structure of the top ITO/spacer Al_2O_3 was patterned by photolithography and a wet etching processes. Throughout these patterning processes, the sidewall of the top and bottom ITO layers was eventually exposed as source/drain (S/D) regions. ZnO, Al_2O_3, and Al-doped ZnO (AZO) were successively deposited as an active, gate insulator, and gate electrode, respectively, by ALD at 150 °C. The film thicknesses of the three layers were 6, 20, and 150 nm, respectively. The channel structures were completely fabricated by patterning the AZO/Al_2O_3/ZnO layers.

For fabrication on the flexible substrate, the ITO S/D electrode and spacer dielectric layers were changed into Ti and polyimide (PI) films to provide the flexibility of the fabricated devices. Glass-fabric reinforced coating film on a surface-treated substrate (GreCoSS) was used as a flexible substrate. General characteristics and technical merits of the GreCoSS were previously documented [9]. A bilayered buffer layer composed of spin-coated organic film and ALD-grown Al_2O_3 was initially prepared on the GreCoSS. The film thickness of S/D Ti and spacer PI layers were 10 and 500 nm, respectively. The baking temperatures for the PI spacer and buffer layers were 150 °C. The other process parameters were the same as

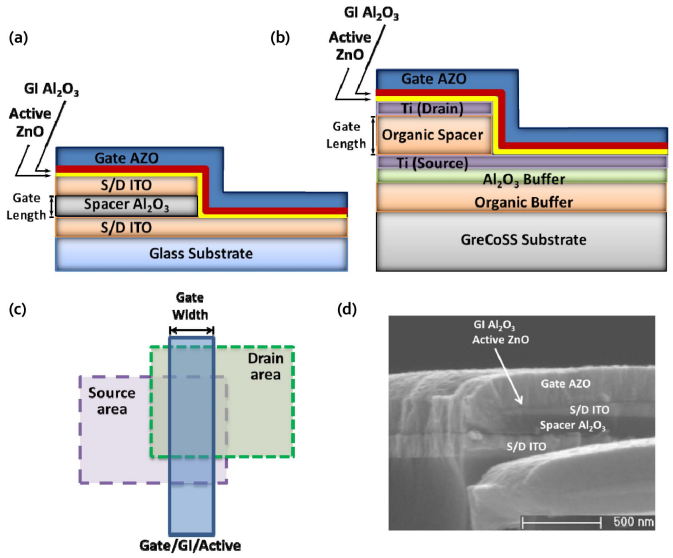

Fig. 1. Schematic cross-sectional diagrams of the proposed V-TFTs fabricated on (a) glass and (b) flexible GreCoSS substrates. (c) Simplified layout configuration among the source, drain, and gate/gate insulator/active regions for the V-TFT. (d) Cross-sectional SEM image of the V-TFT fabricated on glass substrate.

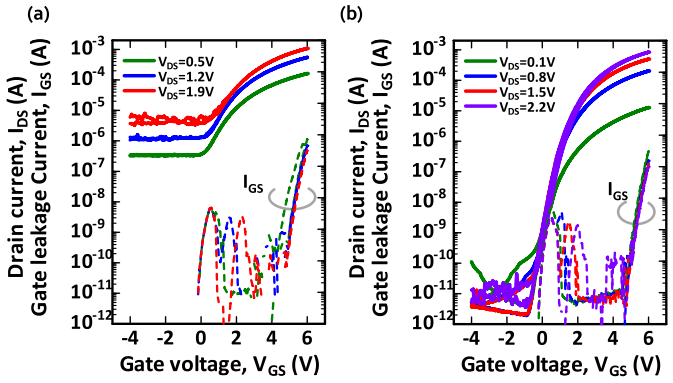

Fig. 2. I_{DS}-V_{GS} characteristics and I_{DS} gate leakage currents of the ZnO V-TFTs fabricated on the glass substrate (a) before and (b) after O_2 plasma treatment on the back-channel region. The measurements were performed in double sweep mode of V_{GS}.

those for the TFTs fabricated on the glass substrate. Schematic cross-sectional views of the proposed ZnO V-TFT on the glass and flexible substrates are shown in Figs. 1(a) and (b), respectively. The layout for the V-TFT was designed as shown in Fig. 1(c), in which source and drain layers were initially shifted to stably secure the misalign margin. Although the design rule for the flexible device should be greater than that for the device on the glass substrate owing to the high thermal expansion coefficient of the flexible substrate, a sufficient align margin could be obtained using this layout configuration. The electrical characteristics of the fabricated V-TFTs were evaluated using a semiconductor device parameter analyzer (Agilent B1500A) at room temperature in a dark box.

III. Results and Discussion

Figs. 2(a) and (b) show the drain current (I_{DS})-gate voltage (V_{GS}) characteristics of the fabricated ZnO V-TFT before

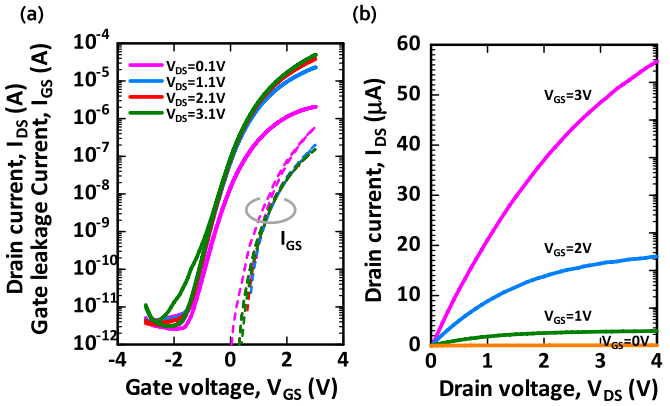

Fig. 3. (a) I_{DS}-V_{GS} transfer characteristics and I_{DS} gate leakage currents and (b) I_{DS}-V_{DS} output characteristics of the ZnO V-TFTs fabricated on the flexible GreCoSS substrate.

and after plasma treatment on the back-channel, respectively. Large off-currents observed in Fig. 2(a) may originate from the back-channel effect. The damaged back-channel significantly affects the off-current level of the TFT because the reduced field across the gate stack at the back-channel region cannot effectively suppress the off-current. Furthermore, the Fermi-level pinning resulted from the large number of interface states and carriers caused by some defects such as oxygen vacancies near the back-channel may induce the large off-current for the V-TFT with a very short channel. While the back-channel region can be controlled to have a terminated surface for normal planar-type TFTs, the back-channel surface (sidewall of stacked films) exposed by the etching process remains crude and unstable for the proposed V-TFTs. To cure the damaged back-channel, the oxygen plasma treatment was prescribed for the V-TFT in a dry etching chamber. The off-currents were drastically reduced for the plasma-treated V-TFT, as shown in Fig. 2(b). This result suggests that the main origin for the large off-current was the damaged back-channel region. During the oxygen plasma treatment, oxygen vacancies could be effectively reduced by providing sufficient amounts of oxygen before the deposition of active layer. The on/off ratio and field-effect mobility at the saturation region (μ_{fe}) were estimated to be approximately 1.3×10^8 and 3.6 $cm^2V^{-1}s^{-1}$, respectively. Oxide TFTs do not exhibit short-channel effects, even for the TFT with a very short channel length [10]. This can be confirmed for the V-TFT due to the very short channel length. The threshold voltage (V_{th}) of the fabricated V-TFT typically was near 0 V of V_{GS}. This suggests that the oxide TFTs do not experience a marked short-channel effects even at very short channel lengths, even though the investigation on the roll-off of V_{th} with the decrease in the channel length is necessary for careful analysis. The gate leakage currents remained markedly high for both V-TFTs before and after the plasma treatment. A very thin film thickness of the Al_2O_3 gate dielectric layer and a surface roughness of the vertical channel can induce the leakage path of the tunneling currents. Furthermore, a high V_{DS} sometimes may induce a breakdown within an active channel owing to the self-heating effect caused by excessively large drain current. The constant-current stress test was also confirmed to examine

the operational reliabilities of the device, in which the drain current did not show any remarkable changes with a lapse of 5000 s.

The device performances of the V-TFT fabricated on the flexible substrate were compatible with those of the V-TFT on the glass substrate, as shown in Fig. 3(a). The calculated values of V_{th}, μ_{fe}, subthreshold swing (SS), and on/off ratio were 0.8 V, 3.3 $cm^2V^{-1}s^{-1}$, 0.4 V/dec, and 8.8×10^6, respectively. Considering that the processes were performed below 150 °C, the obtained results were very encouraging for the flexible electronic applications. Even though the μ_{fe} of the ZnO V-TFT was not large, the current drivability was very high (ca. 6 A/μm) due to the very short channel length. Fig. 3(b) shows the output characteristic of V-TFT when the V_{GS} was varied from 0 to 3 V. The V-TFT exhibited good behaviors in the linear region without marked contact resistance. Excellent gate-bias modulation of the drain current was also confirmed for the saturation region. The V-TFT fabricated on the flexible substrate has another merit in that the channel area is not affected by bending or stretching of the substrate because the direction of the change in the substrate during bending is perpendicular to the direction of the channel region. Therefore, the V-TFTs are expected to be intrinsically immune to the change or failure of the device performance during the bending situations. The device characteristics of the V-TFTs were confirmed to exhibit no marked changes under the bending situations.

IV. Conclusion

Vertical channel TFTs employing a ZnO active channel, Al_2O_3 gate insulator, and AZO gate electrode were successfully fabricated on glass and flexible substrates by exploiting the ideal conformal deposition of the ALD process. A channel length of 500 nm was achieved using a conventional photolithography apparatus. The values of μ_{fe} for the V-TFTs on the glass and flexible substrates were 3.6 $cm^2V^{-1}s^{-1}$ and 3.3 $cm^2V^{-1}s^{-1}$, respectively. Large off-currents, which were caused by the damaged back-channel, was improved by O_2 plasma treatment on the back-channel region and an on/off ratio greater than 10^6 was obtained, even for the V-TFT on the flexible substrate. The proposed V-TFTs are very suitable for the applications of transparent and flexible integrated circuits demanding higher density of devices and/or driving currents due to specified advantages of the V-TFT, such as a high current drivability and a small footprint.

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