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Influence of gate dielectric/channel interface engineering on the stability of amorphous indium gallium zinc oxide thin-film transistors

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We report the simultaneous improvements of the threshold voltage (V_{th}) stabilities under the prolonged positive gate bias stress (PBS) and negative gate bias under illumination stress (NBIS) by employing the gate dielectric/channel interface engineering in the bottom-gate, DC-sputtered amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFT). In the interfacial region, a-IGZO is grown under the low oxygen partial pressure (P_{O_2}) condition to minimize the damage from highly energetic oxygen anion bombardment into the substrate during sputtering. Meanwhile, high P_{O_2} is employed during the bulk growth of active film to reduce the oxygen vacancy (V_O) related defects in a-IGZO, which is known to be a main cause for the degradation of the electrical properties of TFT under NBIS. Owing to the lower damage of the gate dielectric by interface engineering during sputter deposition, the charge trapping or injection probability into the gate dielectric is diminished. Consequently, V_{th} instabilities due to both the electron trapping under PBS and the trapping of positively charged species under NBIS are alleviated simultaneously.

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1 Introduction Amorphous indium gallium zinc oxide (a-IGZO) has been gaining great attention due to its potential use as a channel material for switching and/or driving electronics in large-area active matrix liquid-crystal display (AMLCD) and active matrix organic light-emitting diode (AM-OLED) displays [1]. It provides excellent transfer characteristics such as high field-effect mobility of 10–30 $cm^2 V^{-1} s^{-1}$ and high on/off ratio exceeding 10^7–10^8 that are essential for high-resolution and high-speed applications in future displays. Also, good uniformity can be obtained utilizing current manufacturing facility of sputtering that makes the manufacturing cost effectively lower than that of low-temperature polysilicon (LTPS) thin-film transistors (TFT) used as the high-mobility TFTs [2]. For its real applications as a replacement for Si-based TFTs in the display backplane, it is critical to solve the electrical instabilities related with the prolonged gate bias stress, especially under illumination [3]. Much experimental [4–18] and theoretical [19–21] effort has been done to reveal the origin of the threshold voltage (V_{th}) instability in a-IGZO TFTs and improve the process conditions to minimize it. V_{th} instabilities under positive gate bias stress (PBS) or negative gate bias stress (NBS) are not severe [5]. Negative gate bias stress under visible-light illumination (NBIS), however, causes huge negative V_{th} shifts as much as a few volts within a few hours [6]. It has been suggested that the oxygen vacancy (V_O)-related defect states located 0–1.5 eV above the valence-band maximum (VBM) in the subgap region of a-IGZO are mainly responsible for the photoresponse even at optical energies smaller than the bandgap (~3.1 eV) [1, 20]. Neutral V_O can be changed into singly or doubly ionized metastable states (V_O^+, V_O^{2+}) via photoabsorption [16] or creating a hole in the valence band via thermal activation and thereafter positively charged species are migrated into the

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gate dielectric/channel interface under the constant negative electric field and trapped thereafter. Thus, the field-screening effect due to the fixed charge trapped in the gate insulator/active interface or bulk in the gate insulator results in parallel V_{th} shift without appreciable degradation of subthreshold swing (SS) and mobility.

The methods to reduce V_O related defects in oxide semiconductors to improve the electrical stability under NBIS are summarized as follows: post-treatment methods during TFT fabrication process such as post-annealing in water or oxygen environment [7], high-pressure annealing at oxygen atmosphere [8, 9], N_2O, or O_2 plasma treatment [10, 11], the application of passivation layer like as Al_2O_3 or SiO_X [12, 13], the insertion of blocking layer against migration of positively charged species [14], sputtering parameter optimization [15] such as high power and high oxygen partial pressure in the reactive sputtering, and the proper selection of gate dielectric material [17, 18]. In the case of the bottom-gate configuration, however, the reactive sputtering in a high-power and/or high oxygen partial pressure condition is very prone to result in PBS instability and large hysteresis due to the gate dielectric/channel interface damage from the energetic bombardment of negative oxygen ion accelerated by the negative potential of the cathode [22–25].

In this paper, we report that the interface engineering during the sputter deposition of a-IGZO in the bottom-gate configuration can enhance both PBS and NBIS instability simultaneously by minimizing electron and positively charged species trapping probability where a-IGZO thin film in the interfacial region is deposited under the low P_{O_2} and that in bulk region is deposited under the high P_{O_2}.

2 Experimental

The TFT structure used in this study has a bottom gate, bottom contact configuration on the glass substrate as shown in Fig. 1 and the fabrication process has been described elsewhere in detail [26]. The a-IGZO thin film of 40 nm thickness was deposited on the SD electrode by DC sputtering at room temperature under mixed Ar and O_2 environments using a single rotary IGZO target with 1:1:1 atomic ratio. For a comparative study of the effects of sputter deposition condition on TFT performance, an active layer was deposited using a single-layer scheme (device A, device C), or double-layer scheme (device B) where in a single-layer approach, 40% P_{O_2} and 20% P_{O_2} was employed in device A and device C, respectively, and a double-layer structure of 10 nm IGZO film deposited at 20% P_{O_2} in the gate dielectric/active interface region followed by 30 nm deposition at 40% P_{O_2} was applied to device B. To protect the backchannel from chemical attack during photolithography of the active film and the environmental effects such as O_2 and H_2O during electrical measurements, the protective layer (PL) of 10-nm thick Al_2O_3 was deposited by ALD at 200 °C on the IGZO film and patterned simultaneously with the active film with diluted hydrofluoric acid in deionized water. Finally, the device was annealed at 350 °C for 2 h in an oxygen atmosphere before electrical measurements. The electrical properties of TFT were characterized by an Agilent B1500A semiconductor parameter analyzer and the field effect mobility was extracted using transconductance (g_m) in the linear region from standard MOSFET equation at a gate voltage of $V_{on} + 15$ V, where V_{on} is defined to be a gate voltage that results in drain currents of $W/L \times 10$ pA where W, L are width and length of TFTs, respectively. The dimensions of W and L employed in this study were 80 and 20 μm, respectively. The threshold voltage is extracted by extrapolating the slope in the square root curve of drain currents at $V_{ds} = 10$ V versus gate voltage to the gate voltage axis. For NBIS test, the green light of 0.15 mW cm^{-2} filtered by a bandpass filter at 530 ± 10 nm from a halogen lamp was used and its intensity was measured by photometry (Newport, 1918-C). The pristine devices fabricated on the 100 by 100 mm^2 glass substrate were employed to measure the electrical stability under various stress conditions on each active layer scheme (devices A, B, and C) and their initial characteristics were assessed before stress measurements.

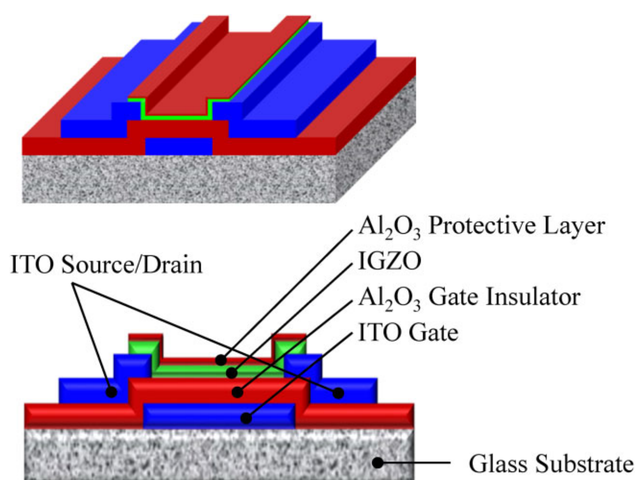

Figure 1 Schematic diagrams of bottom-gate, bottom-contact TFT structure with protective layer on the backchannel.

3 Results and discussion

The initial transfer curves of devices A, B, and C are shown in Fig. 2 and their TFT parameters are listed in Table 1. This shows that the higher P_{O_2} during active deposition gives much better initial TFT characteristics than the lower P_{O_2}. The large SS and very low mobility is observed in device C in which only low P_{O_2} is employed for the active growth. In the case of device B, it shows much better electrical characteristics than those of device C although it still has a lower mobility and a larger SS than device A. It seems that the high P_{O_2} is more favorable for good initial TFT characteristics than low P_{O_2} because it suppresses the formation of the high density of band-tail states below the conduction-band minimum (CBM) related to V_O near metal cations. Kamiya et al. [27] had shown that V_O generates the localized states just below CBM as well as

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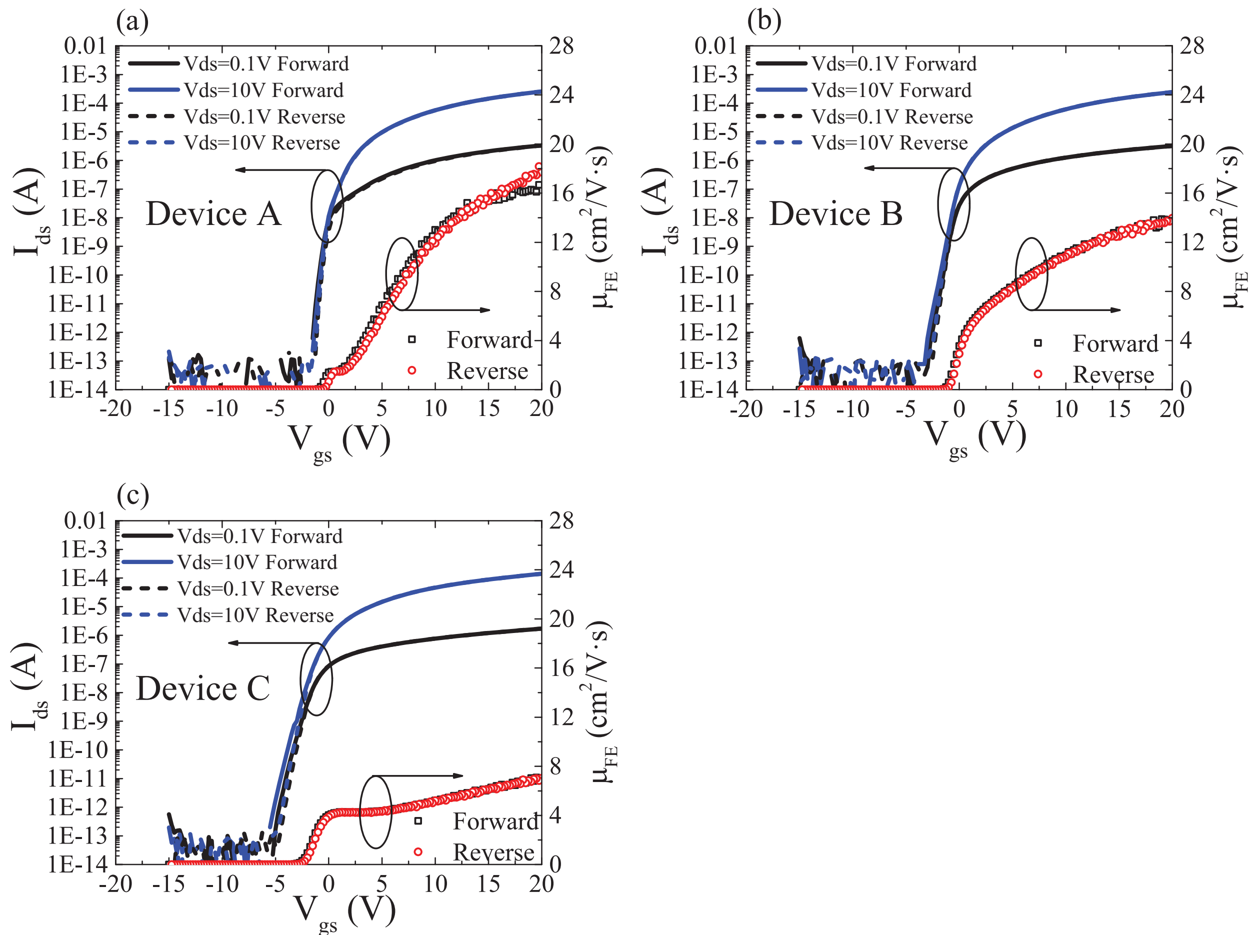

Figure 2 The initial transfer characteristics and field effect mobility of TFTs. (a) Device A, (b) device B, and (c) device C. Devices A and C have a single layer of IGZO 40 nm sputtered under 40% P_{O_2} and 20% P_{O_2}, respectively. Device B has a double active layer that consists of 10-nm IGZO sputtered under 20% P_{O_2} followed by 30-nm IGZO sputtered under 40% P_{O_2}.

Table 1 The initial TFT properties of devices A, B, and C.

	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	SS ($V dec^{-1}$)	V_{th} (V)	V_{on} (V)
device A (P_{O_2} 40%, single active layer)	14.96	0.29	1.16	−0.15
device B (double active layer)	12.19	0.47	0.03	−1.75
device C (P_{O_2} 20%, single active layer)	5.46	0.70	−1.63	−3.75

the localized states 0–1.5 eV above the valence-band maximum (VBM) by *ab initio* calculation. The larger density of V_O in device B and device C than that in device A is also reflected on the initial photo response of transfer characteristics under visible illumination, as shown in Fig. 3. The photoinduced subthreshold current increases in the order of device A, device B, and device C, in agreement with the results by Kim et al. [15] where they reported the higher P_{O_2} and high-power condition in sputter deposition of oxide semiconductor resulted in less photoinduced subthreshold current. Figure 3 also shows that the magnitude of the photoinduced subthreshold current is almost constant even after 10 000 s duration of prolonged NBIS stress at −0.57 $MV cm^{-1}$ and green-light illumination. When the illumination is switched off after NBIS stress of 10 000 s, the photoinduced subthreshold current disappears, as shown in Fig. 3. On the other hand, there exists an irreversible change of ΔV_{th} to the negative direction after stress. We suggest that the photoinduced subthreshold current does not involve the state creation or charge trapping in the active or gate dielectric/active interface due to the stress but the band-tail states below CBM are populated via photoabsorption from the valence band and the populations become equilibrated during visible-light illumination, which increases subthreshold currents, as illustrated in Fig. 4. Therefore, the high P_{O_2} in the reactive sputtering of IGZO in which V_O formation is

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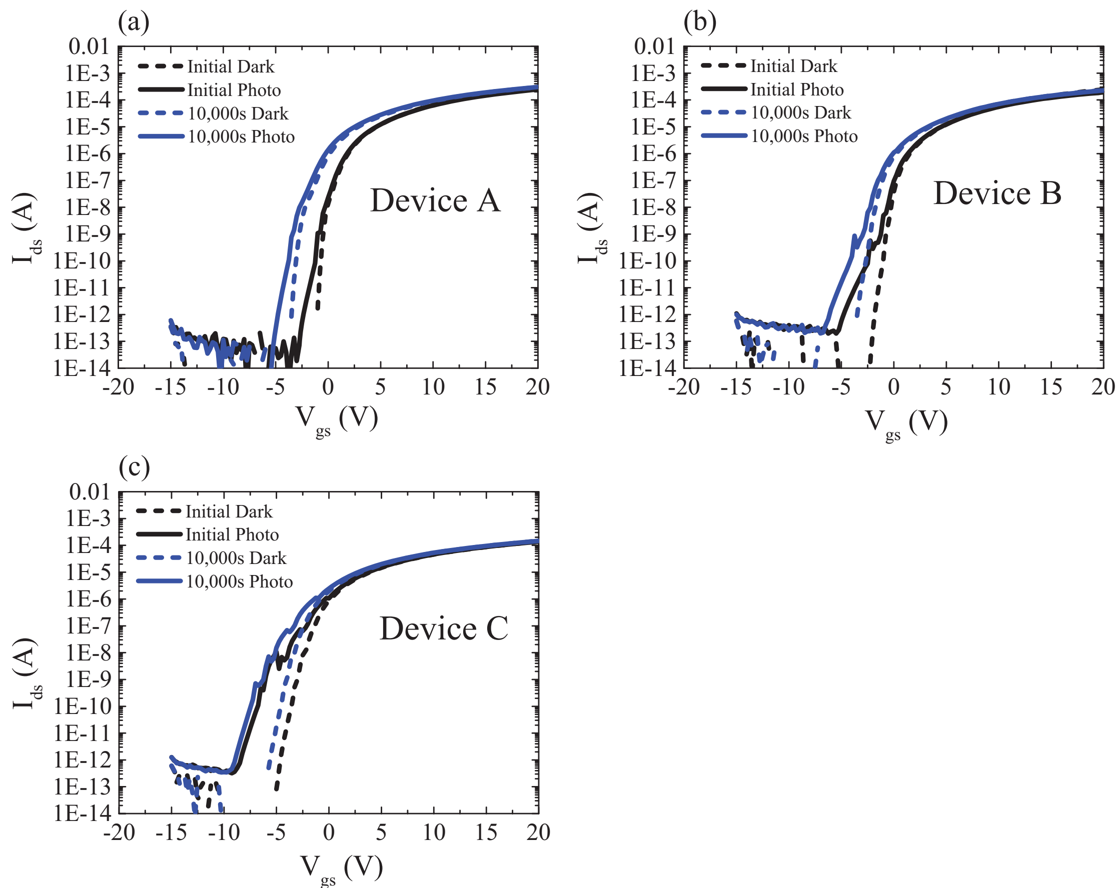

Figure 3 The change of transfer curves of devices A, B, and C measured before and after the negative gate bias stress ($V_g = -10$ V, $V_d = V_s = 0$ V) under green-light illumination of 0.15 mW cm^{-2} at 530 nm (NBIS). The black lines are measured prior to NBIS stress and the blue lines are measured after 10 000 s NBIS stress. The dashed lines are measured in the dark and solid lines under illumination.

minimized is effective in obtaining good electrical performances, such as high mobility and low SS in IGZO TFTs.

On the other hand, it has been reported that the bottom gate TFTs fabricated in the high P_{O_2} is more vulnerable to the V_{th} instability under PBS [28] due to the electron trapping by the acceptor-like states related with interstitial oxygen in the active bulk [29] or acceptor-like state generation in the upper half of the bandgap [30]. Figure 5, however, shows that device B with interfacial a-IGZO of 10 nm thickness deposited under low P_{O_2}, showed a dramatic improvement of V_{th} stability under PBS compared to that of device A. This suggests that the main origin of V_{th} instability by PBS in the bottom-gate configuration may not be related with bulk traps in the active film but with the interface trap. Recently, Jia et al. [25] have conducted *in situ* analysis on the kinetic energy distribution of negative oxygen ions in IGZO sputtering process and shown that the high P_{O_2} in sputter deposition of oxide semiconductor shifted the energy distribution of oxygen ions to the higher kinetic energy than did the low-P_{O_2} conditions. Therefore, we speculate that the damage in the interface or gate dielectric bulk near the interface by the negative oxygen ion bombardment is small and results in a lower density of states for electron trapping in device B than that in device A.

Interestingly, it is found that device B has a smaller ΔV_{th} than device A even under NBIS, as shown in Fig. 6, in spite of the larger V_O density in the interfacial region in device B, as evidenced in larger photoinduced subthreshold current (Table 2). This is also demonstrated in device C that has the smallest ΔV_{th} under NBIS stress although it has the largest photoinduced subthreshold current. This clearly shows that the sputter deposition under low P_{O_2} in the interfacial region gives much lower interface or bulk trap density in the gate dielectric than that under high P_{O_2} such that the number of trapping events in the interfacial region of photogenerated or photoinduced positively charged species such as V_O^+ or V_O^{2+} generated in the active bulk is diminished due to the lower interface damage in the gate insulator induced by oxygen ion bombardments. We note that the overall density of states in the IGZO including the interface states in the IGZO side would be much larger in the case of low-P_{O_2} conditions than high P_{O_2}, as revealed by the large SS of initial transfer curves, but the interface states caused by the damage in the gate insulator side seem to have a much more dominant

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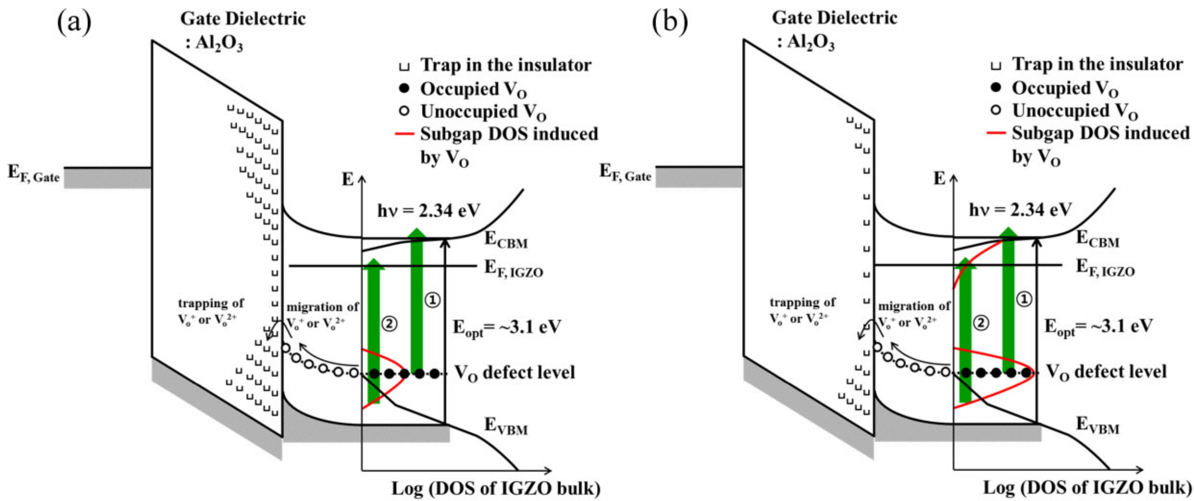

Figure 4 Schematic band diagrams of (a) highly damaged interface caused by oxygen-ion bombardments during sputter deposition under high-P_{O_2} conditions and of (b) low damaged interface under low-P_{O_2} condition. In process 1, the neutral oxygen vacancies are photoexcited into V_O^+ or V_O^{2+} and migrated into the gate dielectric interface under the negative gate bias, and the extra band-tail states near CBM induced by V_O in oxygen-poor a-IGZO are populated via photoabsorption in process 2.

Figure 5 Transfer curves as a function of stress time for 10 000 s under positive gate bias stress with $V_g = +20$ V ($+1.14$ MV cm^{-1}) and $V_d = V_s = 0$ V in the dark. (a) Device A, (b) device B, and (c) device C.

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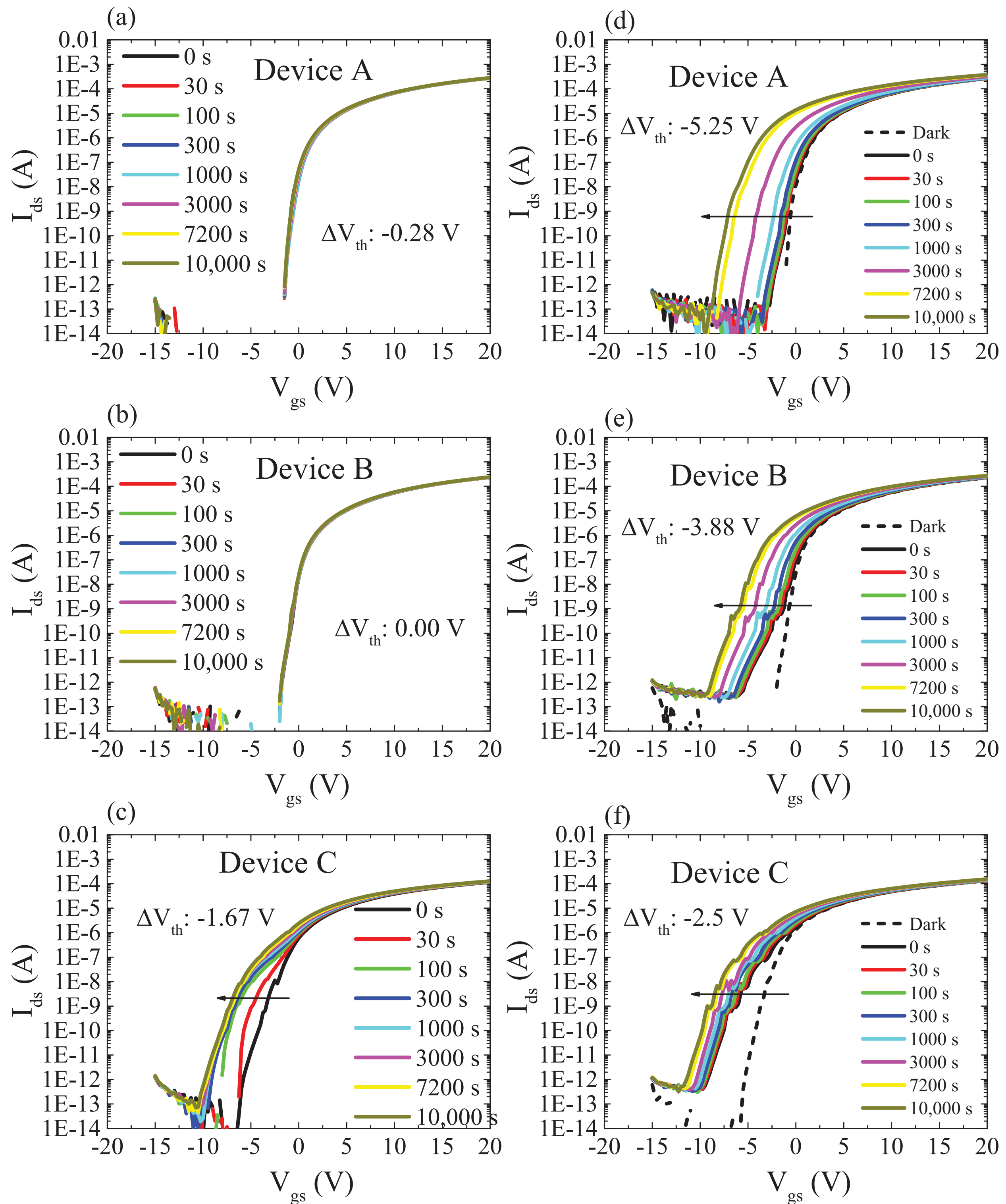

Figure 6 Transfer curves of (a) device A, (b) device B, and (c) device C as a function of stress time for 10 000 s under negative gate bias stress with $V_g = -20$ V (-1.14 MV cm^{-1}) and $V_d = V_s = 0$ V in the dark and (d) device A, (e) device B, and (f) device C under negative gate bias stress with $V_g = -20$ V (-1.14 MV cm^{-1}) and $V_d = V_s = 0$ V with green-light illumination of 0.15 mW cm^{-2} at 530 nm.

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Table 2 ΔV_{th} under various electrical and illumination stress tests for 10 000 s of device A and device B.

ΔV_{th} (V)	PBS $+1.14\,MV\,cm^{-1}$	NBS $-1.14\,MV\,cm^{-1}$	NBIS $-0.57\,MV\,cm^{-1}$	NBIS $-1.14\,MV\,cm^{-1}$
device A (P_{O_2} 40%, single active layer)	3.56	−0.28	−1.97	−5.25
device B (double active layer)	0.84	0	−1.09	−3.88

effect on the V_{th} instability related with charge trapping. When we tested pure Ar conditions in the interfacial region, a very low field effect mobility of $\sim$0.1 $cm^2\,V^{-1}\,s^{-1}$ with an on/off ratio of 10^4 was obtained. If the charge-trapping probability in the gate dielectric/active interface region is low, the migration of charged species by a gate electric field into the interfacial region will be delayed owing to the space-charge effect even if the more charged species are generated in the active bulk via photoabsorption due to the larger density of V_O, as in the case of device B and C. Oh et al. [14] recently demonstrated this by insertion of a stopping layer of ion migration in the active bulk film. We note that without illumination, no V_{th} shift under NBS is observed in both device A and device B which indicates there is no positively charged species in pristine devices but device C shows appreciable V_{th} instability under NBS, which may be originated from the trapping in the gate dielectric interface of considerable amounts of positively charged species that may exist already in the active bulk even without illumination. Recent *ab initio* calculation by Noh et al. [21] shows that the ionized V_O in oxygen-deficient a-IGZO can exist in equilibrium with neutral V_O depending on the configuration of metal cations around V_O due to the diverse neutral oxygen vacancy formation energy of 2.96–5.82 eV and the transition level. It is suggested that the thickness of the active film in the interfacial region deposited under low-P_{O_2} conditions should be optimized in order to prevent the generation of a high density of positively charged species such as ionized V_O and protect the gate dielectric interface or bulk from damage during the sputter deposition of the active bulk film under high P_{O_2}. We conclude that the high P_{O_2} in the sputtering process of the oxide semiconductor in the bottom-gate configuration generates interface or bulk states in the gate dielectric near CBM and/or VBM of a-IGZO that can trap electrons and/or holes, respectively, depending on the gate bias stress condition, as shown in Fig. 4.

4 Conclusions In summary, we performed the experiments to clarify the origin of the electrical instabilities under gate bias stress and/or under illumination for the IGZO TFTs fabricated by reactive sputtering in the bottom-gate configuration. The experimental results showed that the device instability accompanied by the increase of P_{O_2} in the reactive sputtering is mainly due to the charge traps in the gate insulator/active interface and/or bulk in the gate dielectric caused by negative oxygen ion bombardments and the electrical stability can be greatly enhanced by employing the graded-layer deposition method for sputtering of an oxide semiconductor.

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