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Nonvolatile memory thin-film transistors using an organic ferroelectric gate insulator and an oxide semiconducting channel

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Abstract

Organic–inorganic hybrid-type nonvolatile memory thin-film transistors using an organic ferroelectric gate insulator and an oxide semiconducting active channel are a very promising solution to the memory devices having both features of low-cost and high-performance, which are embeddable into the next-generation flexible and transparent electronics. In this paper, we discuss some important issues for this proposed device, such as device structure design, process optimization and memory array integration. Promising feasible applications and remaining technology issues to solve were also discussed.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The application of ferroelectric ceramics has been manifold and overspreading, covering all areas of our workplaces and homes over the present century. The need for useful and reliable devices has been closely related to the successful applications such as their piezoelectric, pyroelectric, ferroelectric, electrostrictive and electrooptic functions. By far the largest number of applications in ferroelectric ceramics remained to be associated with bulk ceramics, but a trend toward thin films for a specified application, which offers additional benefits including lower operating voltage, higher speed operations and scaling ability [1, 2], has been energetically developed. Among various applications of ferroelectric thin films, the development of the nonvolatile ferroelectric random access memory (FeRAM) has been most actively progressed since the late 1980s [3, 4] and has reached modest mass production for specific applications since 1995. These trends have been mainly motivated by the physical limitation and technological drawbacks of the Flash memory, which is a main character among the nonvolatile memories in the giant Si electronics industry. Beyond 15 nm generation, keeping the pace of device scaling with Moore's law will become more severe. Low program speed, limited program/erase endurance and power consumption should be also considered. With the same motivation, various alternative nonvolatile memory technologies such as magneto-resistance RAM (MRAM) [5, 6], phase-change RAM (PRAM) [7, 8], resistance-change RAM (ReRAM) [9, 10], solid-electrolyte-type memories [11, 12] and the likes have been developed. There are two types of memory cells in ferroelectric nonvolatile memories. One is the capacitor-type FeRAM, in which a ferroelectric material is used in storage capacitors of a dynamic random access memory (DRAM) structure. The other is the field-effect transistor (FET)-type FeRAM, in which the conventional gate oxide of SiO_2 in the MOSFET is replaced with a ferroelectric thin film. Although the FET-type FeRAM claims the ultimate scalability and nondestructive readout characteristic, the capacitor-type FeRAMs have been the main interest for the major semiconductor memory companies, because the ferroelectric FET has fatal handicaps of cross-talk for random

accessibility and short retention time. Toshiba demonstrated the highest density 128 Mb FeRAM fabricated with a 0.13 μm CMOS process at a conference in 2009 [13]. On the other hand, the memory density of the FeRAM under mass production is still at the level of 4 Mb (by Ramtron). The present main applications of the commercialized FeRAM are low-density nonvolatile memory embedded into radio-frequency identification (RFID) cards [14] and low-power battery backup memory replacing the static random access memory (SRAM). Eventually, the huge expectations for the FeRAM turned out to be somewhat different from what they had in prospect, to the contrary, the Flash memories keep the overwhelmingly dominant position in the nonvolatile memory-related industries thanks to their fascinating technology improvements and tremendously increasing needs for them.

Unlike these Si-based electronics demanding an ultra-high performance and an aggressive device scaling, the requirements for the nonvolatile memory components embedded into the large-area electronics implemented on glass or plastic substrates are considerably different. Above all, the memory devices employed in these fields should be provided at a low cost. Then, if we can additionally obtain such features as mechanical flexibility, transparency to the visible light, lower power operation and higher device reliability with a simpler process at lower temperature, it would have a great impact on the related industries. Various methodologies with different operating origins have been attempted to realize the most suitable memory element for these applications, which will be discussed in later sections in detail. Among them, the ferroelectric field-effect thin-film transistor (TFT) using a polymeric ferroelectric material, instead of oxide ferroelectrics, is a very promising candidate because it can be reproducibly operated with a definitely designable principle and be prepared by a very simple process. It is true that this type of nonvolatile memory transistor still has technological problems, especially in the retention performance, as confirmed for the oxide-FeFET. However, if the minimum specification can be satisfied for the target application, it gains a competitive advantage over other types of devices. In the introduction, firstly, the organic ferroelectric materials and their properties are briefly reviewed, and then the previous works performed by utilizing various channel materials are overviewed.

1.1. Organic ferroelectric material

Poly(vinylidene fluoride) (PVDF, $(CH_2CF_2)_n$) and a copolymer with trifluoroethylene (P(VDF-TrFE), $(CH_2CF_2)_n$-$(CHFCF_2)_m$) are the most well-known polymer ferroelectric materials [15–17]. Although various organic ferroelectric materials such as odd-nylon, cynopolymer derivatives, polyurea, polythiourea and ferroelectric liquid crystal polymers [15] have been introduced, PVDF-based ferroelectrics show superior properties of a relatively large remnant polarization, a short switching time and a good thermal stability. A recent report on croconic acid was very inspiring in that it exhibited the highest spontaneous polarization of approximately 20 μC cm^{-2} [18]. The ferroelectric nature of the PVDF originates from the dipole moments in the molecule which can be aligned with the applied electric field by a rotation of the polymer chain. The strongly electronegative fluorine atoms present in the molecule are the origin of dipole moments [16, 17]. Generally, most PVDF chains have head-to-tail configurations. However, other monomorphic additions of head-to-head and tail-to-tail defects mingle with each other to some extent. These characteristics in stereochemical formations in the PVDF mainly form three polymorphic crystals corresponding to the α, β and γ phases within the packing of polymer chains in the unit cell [19]. Because the α phase exhibits non-polar characteristics, some material processes such as thermal annealing, poling, epitaxy, compression and stretching have been performed in order to obtain other polar phases. These additional processes can be effectively skipped by copolymerizing with TrFE. The polar β phase with all-transconformation corresponds to the optimal alignment of the *C–F* dipoles and the copolymerization of P(VDF-TrFE) enhances the all-transconformation. The material properties such as the melting temperature, Curie temperature and crystallization temperature are varied with the composition of PVDF and TrFE. For example, for the 70/30 composition, those properties are known as 155 °C, 106 °C and 129 °C, respectively. The dielectric constant of P(VDF-TrFE) is in the range from 12 to 25 depending on the composition [15]. PVDF and copolymers are produced on an industrial scale and available on the market with product names such as Solef, KF polymer, Kynar by Solvay Solexis, Kureha and Arkema, respectively. Although the feasibility for realizing a nonvolatile memory device using the P(VDF-TrFE) was already proposed over two decades ago, the main applications have been protection coatings owing to the durability [15]. During these 5 years, there have been very encouraging results on memory device behaviors of metal-ferroelectric-metal (MFM) capacitors [20–25] and metal-ferroelectric-(insulator)-semiconductor (MF(I)S) diodes or FETs [26–33] using the P(VDF-TrFE) thin film. P(VDF-TrFE) thin film can be simply formed by a solution-based spin-coating method and be crystallized at a lower temperature of around 140 °C, in which the solution was synthesized by melting the powder source of P(VDF-TrFE) into various suitable organic solvents such as dimethylformamide, methylethylketone, cyclohexanone and diethyl carbonate. Figures 1(*a*) and (*b*) show the basic ferroelectric properties of polarization–electric field (*P–E*) hysteresis for the Al/P(VDF-TrFE)/Pt capacitors when the film thickness of the P(VDF-TrFE) was varied to 150 and 80 nm, respectively. While the remnant polarizations (P_r) show similar values for two capacitors, the coercive field (E_c) significantly increased from 540 to 730 kV cm^{-1} with the decrease of film thickness. These observations were also clearly confirmed for the polarization saturation behaviors with the increase of applied electric field at various measurement frequencies, as shown in figures 1(*c*) and (*d*). The electric field required to obtain the full saturation in the ferroelectric polarization increased with the decrease in film thickness. This trend was remarkably observed at higher signal frequency. These problems were reported to be markedly improved by

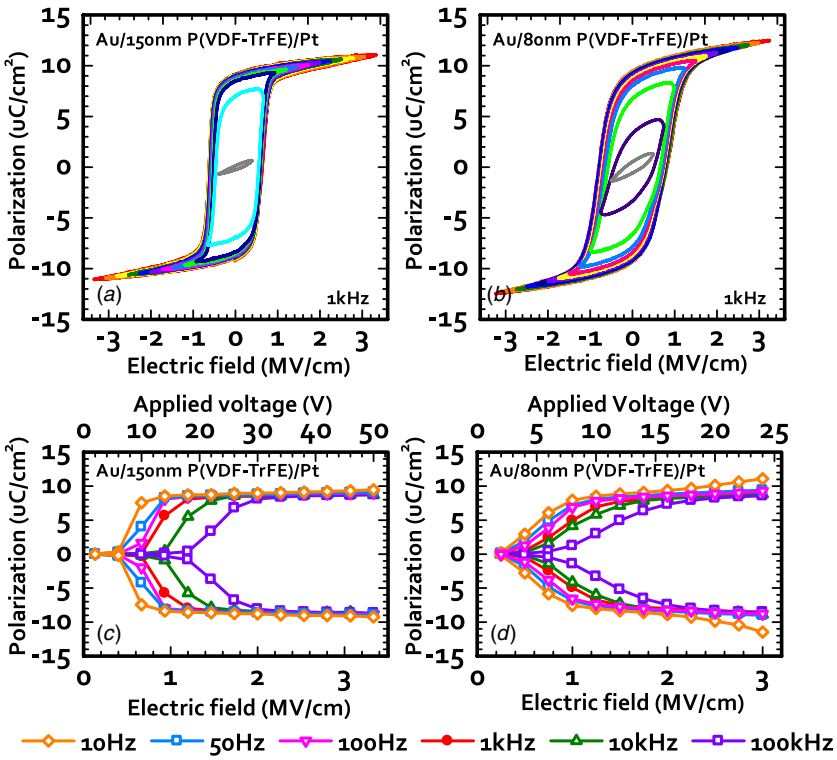

Figure 1. *P–E* characteristics for the (*a*) Au/150 nm-P(VDF-TrFE)/Pt and (*b*) Au/80 nm-P(VDF-TrFE)/Pt capacitors. The measurement frequency was 1 kHz. Polarization saturation behaviors with the increase of applied electric field for the (*c*) Au/150 nm-P(VDF-TrFE)/Pt and (*d*) Au/80 nm-P(VDF-TrFE)/Pt capacitors at various measurement frequencies from 10 Hz to 10 kHz. The top electrode size was 200 μm in diameter.

the introduction of suitable interlayers [20, 24, 25] and the choice of appropriate electrodes [34, 35]. Consequently, comprehensive considerations including the material and process parameters should be taken into account in designing the TFTs with nonvolatile memory function. Ferroelectric-driven nonvolatile bistability of the P(VDF-TrFE) has been examined with various active materials such as a Si substrate (section 1.2), organic semiconductor (section 1.3), oxide semiconductor (section 1.4) and graphene [36, 37].

1.2. Si channel field effect devices

The one-transistor-type memory composed of a single ferroelectric-gate field effect transistor (FeFET) has been extensively researched owing to its excellent scalability and nondestructive readout characteristics, in which various oxide ferroelectric materials such as $Pb(Zr,Ti)O_3$ [38–42], $SrBi_2Ta_2O_9$ (SBT) [43–48], $(Bi,La)_4Ti_3O_{12}$ [49–51], $PbGeO_3$ [52–54], $YMnO_3$ [55], $LiNbO_3$ [56, 57] and $BiFeO_3$ [58, 59] have been employed as the gate insulator (GI) for the FeFET. However, the use of oxide ferroelectrics is decisively unfavorable especially from the two viewpoints of (1) the high crystallization temperature (typically higher than 650 °C) and (2) the high dielectric constant (typically 100 or higher). The first issue is related to the unexpected interfacial reaction with the Si substrate during the crystallization process, which seriously degrades the interface quality. Although the interface degradation can be suppressed by inserting an insulating buffer layer between the ferroelectric GI and Si, the mismatch of the maximum induced charge between the ferroelectric and inserted insulator layers occurs in the resultant MFIS structure [60]. That is, we cannot apply a sufficient voltage to the ferroelectric layer during the programming events before the insulator experiences its dielectric breakdown owing to the high dielectric constant of the ferroelectric GI. For the case of conventional Si-based memory devices, organic ferroelectrics offer an attractive solution to these problems because their crystallization temperature and the dielectric constant are much lower than those of oxide ferroelectrics. Early fabrications of the FeFET with the $Al/SiO_2/P(VDF\text{-}TrFE)/SiO_2/Si$ structure showed the program/erase characteristics with the *on*/*off* ratio of 10^6, even though the program voltage was as high as 200 V [61, 62]. The studies on the MFIS diodes with various interface buffer layers, such as SiO_2 [63–66], Ta_2O_5[67], HfTaO [68] and Al_2O_3 [69], have been carried out in order to stabilize the interfacial behaviors and optimize the process conditions. Furukawa *et al* [70] reported the ferroelectric switching dynamics of P(VDF-TrFE) GI on the Si substrate, in which an important insight that the switching dynamics under the *off* state is controlled at the rate of minority carrier generation in the depletion layer was experimentally claimed. Salvatore *et al* [71] successfully demonstrated the FeFET using 40 nm thick P(VDF-TrFE) GI to be operated with program voltage as low as 6 V. The ms-order program time, the *on*/*off* ratio of 10^5 and the retention time up to few days

are encouraging characteristics for the P(VDF-TrFE)-based FeFETs. Recently, another interesting approach exploiting the FeFET was proposed. The negative capacitance caused by the ferroelectric layer provides the function of voltage amplification. In this approach, the ferroelectric layer can behave as a step-up voltage transformer which can amplify the gate voltage [72, 73]. As a result, the subthreshold swing (SS) can be lower than the theoretically defined value of 60 mV dec^{-1}, and hence the power consumption of the conventional CMOS can be reduced. The feasibility of this proposal has been experimentally demonstrated for the FeFET using the P(VDF-TrFE) [74], although following verifications will be necessary.

1.3. Organic semiconductor active channel

Most works on the fabrication and characterization for the nonvolatile memory devices employing the organic ferroelectrics have been mainly focused for realizing the all-organic memory TFTs with organic semiconducting active layers. Special demands for the integration of memory elements with the organic TFT circuitry on the flexible substrates are significant motivation for the fields of organic electronics. Various combinations of organic ferroelectric GI and organic active layers have been demonstrated, in which the active layers can be classified into (1) the evaporated pentacene [27–29, 32, 33, 75, 76], (2) solution-processed polymeric semiconductors [25, 26, 30, 31, 77–81] and (3) soluble pentacene [82, 83]. For these studies, regioregular poly(3-hexylthiophene) and poly(2-methoxy-5-(2-ethyl-hexyloxy)-1,4-phenylene vinylene) were chosen as polymeric semiconductors. The P(VDF-TrFE) was typically used as the ferroelectric GI. The detailed discussion on these device characteristics can be referred to comprehensive review articles [84, 85]. One of the representative works by Naber *et al* [26], who made a great contribution to this field, demonstrated excellent device characteristics. Although the program voltage range (around ±80 V) was rather high, a large memory *on*/*off* ratio of approximately 10^6, a long retention time of 10^4 m, a high repetitive programming endurance of more than 1000 cycles and a short programming time of 300 μs were successfully claimed. The employment of an organic active channel, especially a soluble polymer, for the organic memory TFTs can be very suitable for low-cost disposable applications with a lower specification. However, the weaknesses of a low field-effect mobility, an unsatisfactory ambient stability and a difficult device integration with the organic-based TFTs seriously restrict the real application within narrow limits.

1.4. Oxide semiconductor active channel

A powerful alternative for enhancing the device performance is to utilize the oxide semiconductor channel for the TFT. Actually, oxide channel TFTs have recently attracted huge interest for use in the active matrix (AM) backplane of liquid-crystal display (LCD) [86] or organic light-emitting diode (OLED) display [87, 88]. These technology trends are attributed to the fact that the TFTs employing the oxide semiconductor channel show such beneficial features as high field-effect mobility, excellent uniformity and robust device stability [89–95], compared to the conventional backplane devices of low temperature polycrystalline and amorphous Si. Polycrystalline ZnO and amorphous indium-gallium-zinc oxide (IGZO) correspond to typical oxide semiconductors and other oxides with various compositions were verified as active channel layers for the oxide TFTs. A transparency of the oxide semiconductor to the visible light can be another benefit of expanding the applications to the transparent electronic devices including the transparent display [96]. These features can be applied for the ferroelectric-based nonvolatile memory TFTs. Although the oxide ferroelectrics have been chosen as GI for the memory transistors using oxide semiconductor channels of indium–tin oxide thin film [97] and ZnO nanowire [98], they seem to be somewhat distant from practical viewpoints owing to their too high thermal budget (700–750 °C).

On the basis of the considerations discussed above, the combination of an organic ferroelectric gate insulator and an oxide semiconducting channel will be the best choice for the high performance nonvolatile memory transistors embeddable into the various electronic systems implemented on large-area glass or plastic substrate. However, it is unexpected that there are not so many studies on the memory TFTs (MTFT) with this organic ferroelectric-oxide (OfeOx) gate stack. In this paper, we provide a specially focused overview on the technical progress and issues for the OfeOx-MTFTs. In section 2, we explain the device design issues for optimizing the memory operations and effects of the device structure on the memory functions. Section 3 highlights some important issues related to the TFT fabrication process, in which the patterning of the polymeric ferroelectric layer, the role of the interface-controlling layer and the solution process for the active channel will be discussed. Promising applications of the proposed memory TFTs are extensively introduced in section 4. In section 5, we deal with the issues of memory array integration, especially in which a disturb-free memory cell composed of switching and memory TFTs using an oxide channel will be proposed. Remaining technical issues for commercial applications are picked up in section 6. Finally, future perspectives and outlooks for these memory TFTs are summarized in section 7.

2. Issues of the device structure design

In fabricating the OfeOx-MTFTs, it is general to employ the top-gate and bottom-contact structure, as shown in figure 2. Because the organic ferroelectrics such as P(VDF-TrFE) are vulnerable to the plasma-induced process for the oxide channel layer, it is very difficult to fabricate the bottom-gate structure with an excellent ferroelectric-semiconductor interface. Sometimes, the post-annealing process at a temperature of higher than 200 °C should be performed to enhance the transistor behaviors after the deposition of the oxide channel. However, for the bottom-gate structure, an available thermal budget after the formation of GI is typically restricted to below 150 °C because of the low

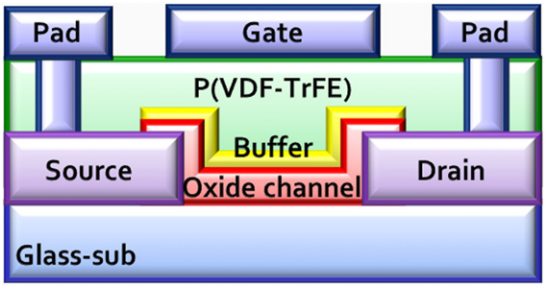

Figure 2. Typical example of a schematic cross-sectional diagram for the proposed OfeOx-MTFTs.

melting temperature of organic ferroelectric materials. In the proposed top-gate structure shown in figure 2, an interface buffer layer can be introduced between the P(VDF-TrFE) and oxide channel layer, which can be prepared with the organic [99] or inorganic oxide layer [100–102]. This buffer layer is very effective for protecting the oxide channel during the spin-coating and etching processes of P(VDF-TrFE). The chemical solvent of P(VDF-TrFE) and O_2 plasma employed for the P(VDF-TrFE) etching might critically degrade the electrical natures of the oxide semiconductors such as ZnO and IGZO. A well-selected interface buffer layer also plays a role in reducing the gate leakage current of P(VDF-TrFE). In order to guarantee the sound device behaviors of the OfeOx-MTFTs with the structure proposed in figure 2, it is very important to optimize some parameters such as thicknesses of interface buffer and oxide channel layers. The details are discussed in the following section.

2.1. Device design scheme

When we compare the OfeOx-MTFT with the ferroelectric FET with the Si channel, the difference in channel material makes their operation mechanisms totally different. While the Si channel FET operates between the inversion and accumulation mode, for the OfeOx-MTFT, the switching between depletion and accumulation should be considered. Here, we have to note that the oxide channel is fully depleted and remains as an insulating layer when the sufficient negative voltage is applied to the gate stack. This is related to the fact that a thinner layer (below 50 nm) of the oxide semiconductor is generally employed for the TFT applications, and that the inversion layer is very difficult to form for the wide band gap oxide semiconductor. The formation of a fully depletion layer is expected to be definitely unfavorable in reducing the operating voltage, because the insulating channel layer makes a loss in applied voltage owing to the capacitance coupling of the gate stack. The load-line analysis is very useful in estimating the programming voltages and the depolarization fields during the retention period for the OfeOx-MTFT. Figure 3(*a*) schematically describes the load-line in the Q–V plane for the OfeOx-MTFT having an interface buffer layer. The gate stack is composed of serially connected ferroelectric (P(VDF-TrFE)) and insulator (buffer layer such as Al_2O_3 [101]) capacitors. Total induced charge density (Q) can be expressed by $Q = Q_F = Q_O = C_O(V - V_F)$, where Q_F and Q_O are the corresponding induced charge densities across the ferroelectric (P(VDF-TrFE)) and insulator capacitors. Therefore, a load-line formed by the insulator capacitor can be described in the V_F axis by the red straight line plotted in figure 3(*a*). On the other hand, at the negative voltage side, C_O is given by the geometric average of C_{OX} (for the insulator capacitor) and C_{dep} (for the depletion capacitor of an oxide channel). Therefore, the slope of the load-line has different values between the positive and negative sides in the voltage axis. Because the operating points at each programming event are determined by the interceptions of ferroelectric Q–V_F hysteresis and the load-line deduced in figure 3(*a*), as shown in figure 3(*b*), different voltage levels are required to completely program both *on* and *off* states. The programming voltages for the *on* ($V_{W,\mathrm{on}}$) and *off* ($V_{W,\mathrm{off}}$) operations of the OfeOx-MTFT can be estimated to be with equations (1) and (2). Here we assume that the ferroelectric polarization in the P(VDF-TrFE) film should be fully saturated for each programming action. It relates to the fact that the use of a saturated ferroelectric hysteresis loop is absolutely desirable to obtain the stable memory operations. The minor loops having partial ferroelectric polarization generally show a very weak immunity against the depolarization field during the data retention period [60]. Therefore, $V_{W,\mathrm{on}}$ and $V_{W,\mathrm{off}}$ are generally decided to be larger than the operating voltages of ordinary TFTs with the same oxide channels:

$$V_{W,\mathrm{on}} = \frac{P_s \cdot d_{\mathrm{ox}}}{\epsilon_0 \cdot \epsilon_{\mathrm{ox}}} + V_{F,\mathrm{sat}} \tag{1}$$

$$V_{W,\mathrm{off}} = \frac{P_s}{C_{\mathrm{ox}}}\left(1 + \frac{\epsilon_{\mathrm{ox}} \cdot d_s}{\epsilon_s \cdot d_{\mathrm{ox}}}\right) + V_{F,\mathrm{sat}} \quad \text{where}$$

$$C_{\mathrm{ox}} = \frac{\epsilon_0 \cdot \epsilon_{\mathrm{ox}}}{d_{\mathrm{ox}}}, \tag{2}$$

where P_s and $V_{F,\mathrm{sat}}$ are saturated polarization charge per unit area of the P(VDF-TrFE) film and corresponding applied voltage across the P(VDF-TrFE) capacitor. ϵ_{ox}, ϵ_s, d_{ox}, d_s are dielectric constants and film thicknesses of the buffer insulator and oxide channel layers, respectively. Because the depletion width (d_{dep}) of the oxide channel layer is related to the applied voltage and the carrier concentration of the oxide channel (N_D), we can estimate the critical voltage value (V_{FD}) at which the oxide channel layer is fully depleted from the delta-depletion analysis [103]. If N_D and d_s are 1×10^{18} cm^{-3} and 10 nm, respectively, the V_{FD} can be estimated to be only about -0.2 V. In other words, the OfeOx-MTFT always operates in the fully depletion mode at the *off*-programmed state. As a result, we cannot minimize the programming voltage for the *off*-state only with the reduction in the thickness of the buffer insulator. The increase in d_s linearly increases $V_{W,\mathrm{off}}$, as expected in equation (2). Consequently, the reduction in the film thickness of both layers of the buffer insulator and oxide channel is necessary for realizing lower-voltage programming in the OfeOx-MTFT. Data retention time of the ferroelectric-based memory transistors is known to be very sensitively affected by the depolarization field induced during the retention period. The depolarization field is

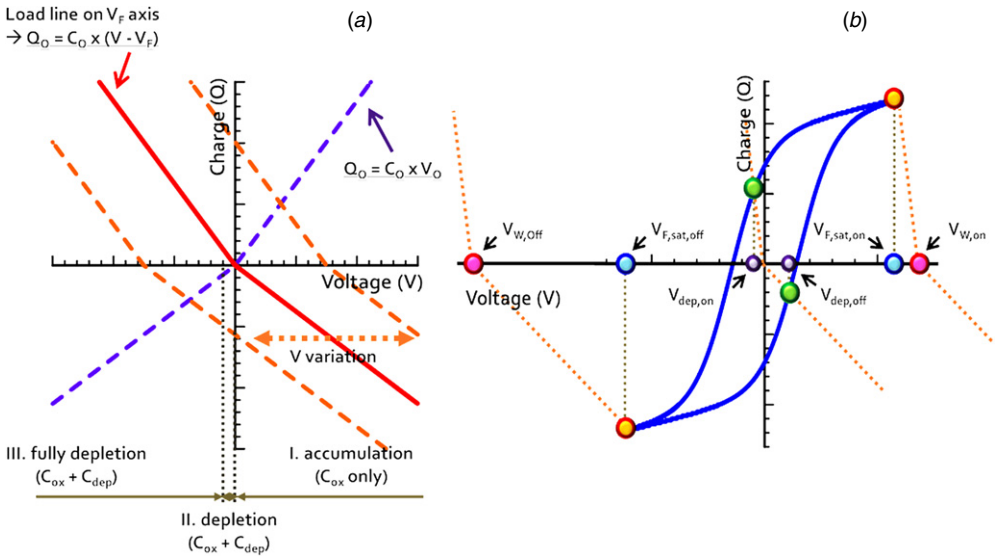

Figure 3. (*a*) Load-line in the *Q*–*V* plane for the determination of operating points for the proposed OfeOx-MTFT [101]. The dotted line in the first and third quadrants shows the variation in the total induced charge density as a function of applied voltage. The load-line determined in the second and fourth quadrants moves on the V_F with the change in the total applied voltage as described by dashed lines. C_{OX} and C_{dep} correspond to the capacitance induced in the interface buffer layer and the depletion layer of the oxide semiconductor channel, respectively. (*b*) The programming voltages for *on* ($V_{W,on}$) and *off* ($V_{W,off}$) operations are determined by the interceptions of ferroelectric *Q*–V_F hysteresis and the load-line deduced in (*a*), in which it is assumed that the $V_{F,sat,on}$ and $V_{F,sat,off}$ are applied to the ferroelectric capacitor at *on* and *off* operations, respectively. During the data retention periods for *on* and *off* states, the depolarization fields of $V_{dep,on}$ and $V_{dep,off}$ are subject to be generated, respectively.

defined as the electric field generated in the ferroelectric layer when the gate is maintained at 0 V [46], as can be seen in figure 3(*b*). Therefore, the film thicknesses of the buffer insulator and oxide channel should also be reduced for minimizing the undesirable depolarization field for the proposed OfeOx-MTFT. It is also interesting to note that the depolarization field for the *off* ($V_{dep,off}$) is determined to be larger than that for the *on* ($V_{dep,on}$).

Although these insights discussed by using the load-line can be a big help for optimally designing the device structure of the OfeOx-MTFT, we should remember that the actually fabricated devices can experience various situations with the difference in process conditions and/or oxide channel materials. In the following section, the device performance of the OfeOx-MTFTs using ZnO or IGZO channel layers is discussed and compared between them.

2.2. ZnO or IGZO-based memory TFTs

A report in 2007 demonstrated the first OfeOx-MTFTs using a ZnO active channel with a poly-4-vinylphenol (PVP) organic buffer layer on the glass substrate [99]. The device showed a ferroelectric-driven memory window (MW) and a field-effect mobility of 0.36 $cm^2\ V^{-1}\ s^{-1}$ owing to the marked reduction of gate leakage current by introducing the interface PVP layer. However, a PVP thickness as thick as 450 nm resulted in an undesirable increase in the programming voltage to ±70 V without any improvement in the subthreshold swing (SS). The device performances were much improved by performing a unique quenching technique for the preparation of P(VDF-TrFE), in which the leakage component of the P(VDF-TrFE) was observed to be remarkably reduced without introducing any interface buffer layer [104]. The effects of thickness variations in the interface buffer and oxide channel layers on the device characteristics were systematically studied by Yoon *et al* [105, 106]. They fabricated the OfeOx-MTFTs using atomic-layer-deposited (ALD) Al_2O_3 and ZnO as the interface buffer and oxide channel layers, respectively. Figures 4(*a*) and (*b*) show the drain current (I_D)-gate voltage (V_G) transfer curves and the gate leakage currents (I_G) for the OfeOx-MTFTs when the ZnO (5 and 20 nm for 4 nm thick Al_2O_3) and Al_2O_3 (4 and 9 nm for 5 nm thick ZnO) thicknesses were varied. I_G as low as 10^{-11} A, steep SS of approximately 400 mV dec^{-1} and seven orders of magnitude *on*/*off* ratio were obtained for these OfeOx-MTFTs. Figure 4(*c*) summarizes the MW values at the same V_G sweep range for each device. The largest MW was obtained for the OfeOx-MTFT with 5 nm ZnO/4 nm Al_2O_3 and the MW showed a decreasing trend as the increase of ZnO and Al_2O_3, which is in agreement with the load-line analysis discussed in figure 3. Here, we can be aware of the fact that there is a significant tradeoff in optimizing the device performances between the available MW and sound TFT behaviors. Actually, the enhancement of SS and the reduction in I_G were obtained for the OfeOx-MTFT when the thickness of Al_2O_3 was controlled to be 9 nm, as shown in figure 4(*b*). It is also interesting to compare the turn-on voltages (V_{on}) for each device, as summarized in figure 4(*d*). The V_{on} is generally expected to be determined at a more positive range in V_G for the device with the thinner ZnO channel owing to its lower carrier concentration. While the OfeOx-MTFTs with 9 nm thick Al_2O_3 comply with this trend, abnormal behaviors were observed for the case of 4 nm

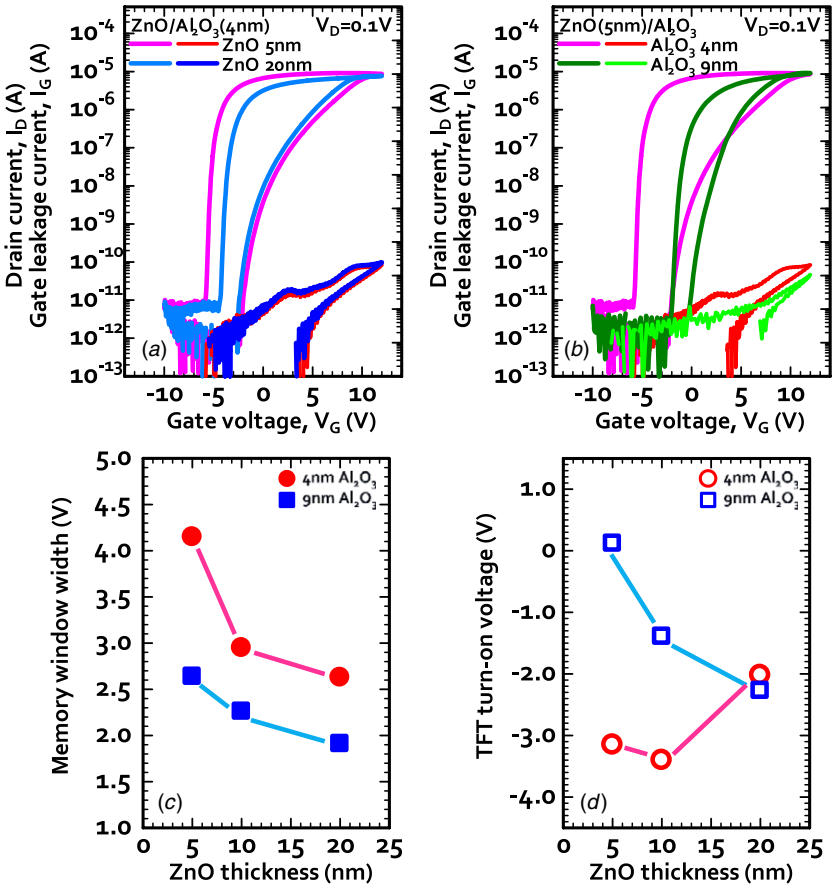

Figure 4. I_D–V_G transfer characteristics and gate leakage currents of the OfeOx-MTFTs using P(VDF-TrFE)/Al_2O_3/ZnO structures with (*a*) ZnO thickness variation (4 nm thick Al_2O_3) [101] and (*b*) Al_2O_3 thickness variation (5 nm thick ZnO). Dependence of ZnO and Al_2O_3 film thicknesses on (*c*) the memory window width and (*b*) turn-on voltage of each OfeOx-MTFT [106].

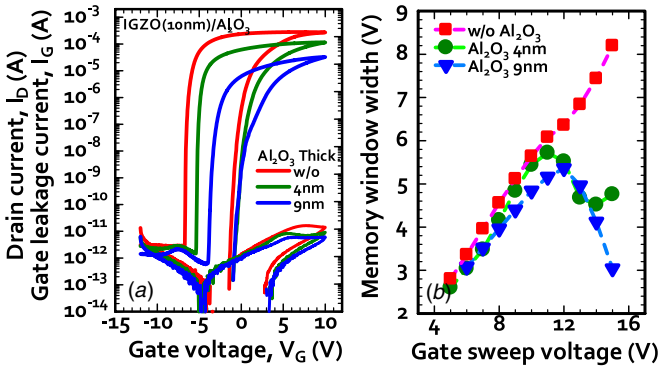

Figure 5. (*a*) I_D–V_G transfer characteristics and gate leakage currents of the OfeOx-MTFTs using P(VDF-TrFE)/Al_2O_3/IGZO structures with the variation in Al_2O_3 thickness. (*b*) Variations in the memory window width with the increase in applied V_G for each device with different Al_2O_3 thicknesses [102].

thick Al_2O_3. This result significantly suggests that there is an optimum thickness of the interface buffer layer for effectively protecting the ZnO channel during the fabrication process, and that the Al_2O_3 thickness should be carefully controlled for obtaining a sufficient MW as well as a good interface quality.

The detailed design schemes for the device structure may depend on the oxide channel material. When the IGZO, which is a typical amorphous oxide semiconductor, was chosen as the oxide channel for the OfeOx-MTFT instead of ZnO, excellent device characteristics were successfully obtained [102]. Figure 5(*a*) shows I_D–V_G transfer curves and I_G for the OfeOx-MTFTs using the IGZO channel when the thickness of the Al_2O_3 buffer layer was controlled to be 0, 4, 9 nm. While the fact that the MW decreased with the increase in the thickness of Al_2O_3 was confirmed as expected from the above-mentioned discussions, it was very impressive to note that the smallest SS value could be obtained for the device without the Al_2O_3 layer. This is completely different from the case when the active channel of ZnO was used for the OfeOx-MTFT. Amorphous IGZO active channel can be concluded to be very robust for guaranteeing the excellent transistor performances, unlike the ZnO with vulnerable natures to the fabrication processes. The variations in MW for the IGZO-based OFeOx-MTFTs with various Al_2O_3 thicknesses at different sweep ranges in V_G were summarized in figure 5(*b*). Although the MWs for all devices were observed to be monotonically increased until the sweep range approached to ±11 V, the MWs for the devices having the Al_2O_3 buffer layer inversely decreased passing through the maximum points. This result indicates that additionally formed interfaces between IGZO

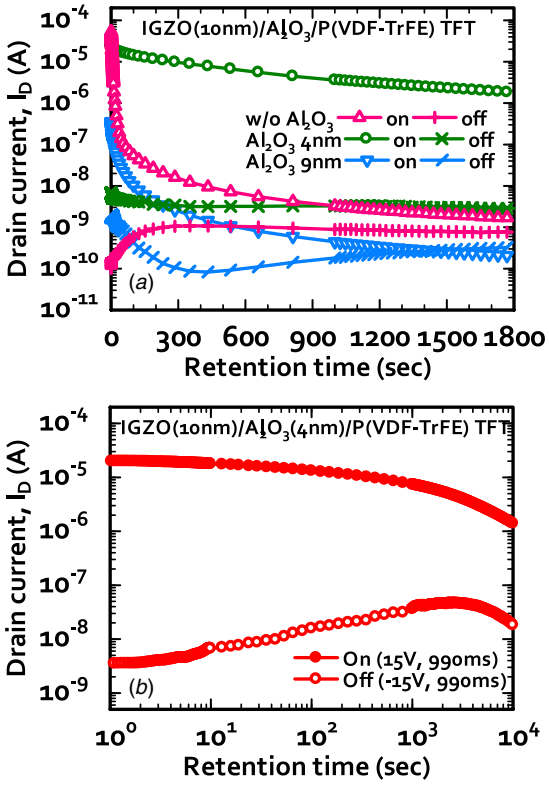

Figure 6. (*a*) Variations in the programmed I_Ds in *on* and *off* memory states were compared among the fabricated OfeOx-MTFTs with different thicknesses of the Al_2O_3 buffer layer with the lapse of time. (*b*) Data retention behaviors of the OfeOx-MTFT using the structure of Al/P(VDF-TrFE)/4 nm thick Al_2O_3/10 nm thick IGZO with a lapse of 10^4 s [102].

and Al_2O_3 or Al_2O_3 and P(VDF-TrFE) might act as trap sites for charge injection at a relatively large V_G owing to the electrical damages to the Al_2O_3 layer as thin as 4 or 9 nm. The field-effect mobility at a linear regime of 60.9 $cm^2\ V^{-1}\ s^{-1}$, the SS of 120 mV dec^{-1}, the MW of 6.4 V at $\pm$12 V programming, the *off*-current as low as 10^{-11} A, which were obtained for the OfeOx-MTFT without the Al_2O_3 layer, can be said to be the best performances among the previously reported memory TFTs using P(VDF-TrFE). However, it was also found that there was an important trade-off in introducing the Al_2O_3 buffer layer when they examined the data retention properties. Figure 6(*a*) shows the variations in programmed I_Ds of the OfeOx-MTFTs with different Al_2O_3 thicknesses with the time evolution. The memory retention time was remarkably improved by introducing the Al_2O_3 buffer layer with an appropriate thickness of 4 nm and the *on*/*off* ratio of more than 70 could be confirmed after the lapse of 10^4 s, as shown in figure 6(*b*). Similar results have been demonstrated for the OfeOx-MTFT employing the ZnO active channel [100, 107], in which the thickness of the Al_2O_3 interface-controlling layer was varied from 1 to 20 nm. These results evidently suggest that the device structures of the OfeOx-MTFTs including the film thicknesses of the interface buffer and oxide channel layers should be systematically investigated to compromise both TFT performance and memory retention time.

For the practical applications of the OfeOx-MTFTs, such considerations as (1) lower voltage operation, (2) higher speed programming, (3) longer data retention and (4) easier integration with peripheral driving circuit should be totally reflected in the design scheme for the device structures. However, because there have not been so many reports concerning the OfeOx-MTFT so far compared to the P(VDF-TrFE)-based memory TFTs using an organic semiconductor, some issues are still under investigation, which will be extensively discussed in section 6. The choice of the oxide channel material is also one of the most important factors for optimizing the device structure of the OfeOx-MTFTs.

3. Issues of process optimization

In this section, some issues related to the fabrication process for the OfeOx-MTFTs are picked up. Actually, the device characteristics were sensitively dominated by the employing process conditions. The first and the second issues correspond to the urgent problems for the memory devices employing other semiconducting channels such as Si or organics as well as for the OfeOx-MTFT to facilitate the fabrication processes and to improve the device performance. The third issue is still challenging but very impacting for the next-generation large-area electronics.

3.1. Lithography compatible patterning process of P(VDF-TrFE)

Most researches on the micro- or nano-patterning for the PVDF-based ferroelectric copolymers have been focused for realizing the nonvolatile memory devices with high integration density. Nanoimprint lithography can provide a good solution to obtain the regularly ordered high-density array and/or the nanoscopic trench structure of the ferroelectric polymer film [108–110]. Z Hu *et al* [110] have reported that the ferroelectric domains nanopatterned by the imprint technique were potentially available not only for realizing the integration densities of higher than 33 Gbit in^{-2} but also for markedly reducing the coercive field to approximately 100 kV cm^{-1}, which provides a meaningful insight for the lower voltage programming operations for the highly integrated memory devices using P(VDF-TrFE). Kang *et al* [111] have demonstrated an interesting approach to patterning the non-polar α phase and ferroelectric γ phase under suitable conditions of temperature and pressure. Ferroelectric nanodomains with the nanomesa structure with approximately 100 nm in diameter were also reported to be patterned by the Langmuir–Blodgett method [112]. Another approach to obtain the patterned regions of nanoscale ferroelectric polarization for the PVDF-based copolymers was to employ the direct writing method by piezoresponse force microscopy [113–116]. Although these methods apparently present very useful techniques for realizing the nanopatterns of ferroelectric domains and for physically understanding the ferroelectric natures in a confined geometry, they do not provide practical solutions for the conventional lithography-based device

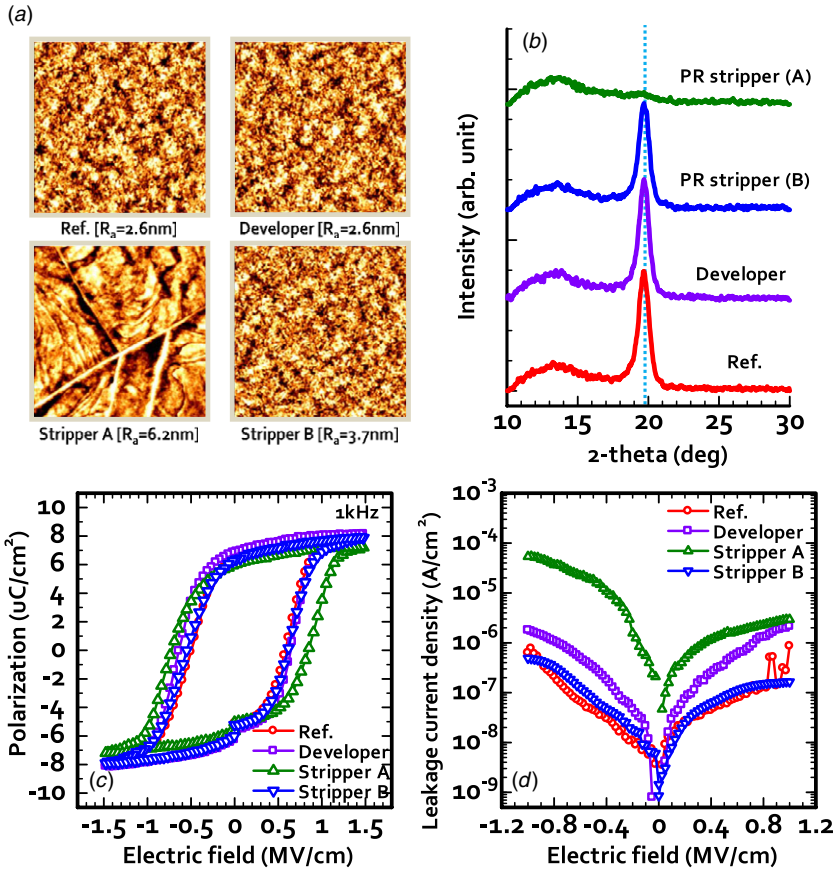

Figure 7. (*a*) AFM surface morphology images in the size of 5 × 5 μm^2 and (*b*) XRD patterns for the P(VDF-TrFE) films treated with the developer and photo-resist strippers. Single peaks at 19.7° correspond to the ferroelectric β phase of the P(VDF-TrFE). Comparisons of (*c*) the *P*–*E* ferroelectric hysteresis and (*d*) the leakage currents of the P(VDF-TrFE) capacitors between before and after the chemical treatments of the developer and photo-resist strippers [117].

fabrication procedures using various chemicals. In order to ensure the sound ferroelectric behaviors of the P(VDF-TrFE) after various fabrication processes routinely carried out for the device fabrication, the effects of chemicals on the electrical and physical properties of P(VDF-TrFE) should be investigated to confirm and optimize the process compatibility of OfeOx-MTFTs. However, systematic studies related to this issue have hardly been dealt with in publications reporting the fabrications of ferroelectric polymer GI-based memory devices. Yoon *et al* [117] have proposed that the use of a photo-resist stripper in the lithography process have something to do with the degradation of the P(VDF-TrFE). Figures 7(*a*) and (*b*) compare the atomic-force microscopy (AFM) observations and x-ray diffraction (XRD) patterns of the P(VDF-TrFE) films treated by some developer and strippers with those of untreated reference film. The deterioration in surface roughness and crystallinity were confirmed for the stripper A-treated film, which is one of the typical commercial strippers. The coercive field and leakage current were also observed to eventually increase for the same controlled film, as shown in figures 7(*c*) and (*d*), respectively. In contrast, it can be found that the suitable choice of stripper (for the case of stripper B) was very important to minimize the degradation effects. Although direct pattern transfer techniques employing x-rays have been proposed to form the microstructures in the polymer film [118, 119], the ferroelectric copolymer film including P(VDF-TrFE) can be easily etched away by using an O_2 plasma in a conventional dry etching system. Figures 8(*a*) and (*b*) show scanning electron microcopy (SEM) images of the P(VDF-TrFE) patterns when it was patterned by the conventional lithography method proposed in [117] and etched by the O_2 plasma. The *P*–*E* hysteresis loops of the Al/P(VDF-TrFE)/p^{++}-Si MFM capacitors and *C*–*V* properties of the Al/P(VDF-TrFE)/Al_2O_3/p-Si MFIS capacitors were characterized when the pattern size was varied, as shown in figures 8(*c*) and (*d*). Considering that the devices with a smaller size did not experience a relatively harder degradation owing to the damage to larger edge areas, it is found that the process engaged with P(VDF-TrFE) can be designed in a very compatible manner to the conventional lithography if the chemicals to use are suitably chosen.

3.2. *Interface buffer layer*

Although interface buffer insulators have been often introduced to various memory devices using the ferroelectric P(VDF-TrFE) layer, types and roles were different for different cases. For the MFIS structures employing the Si substrate as an active semiconducting layer, oxide-type interlayers, such as SiO_2 [65, 66], Ta_2O_5 [67], HfTaO [68]

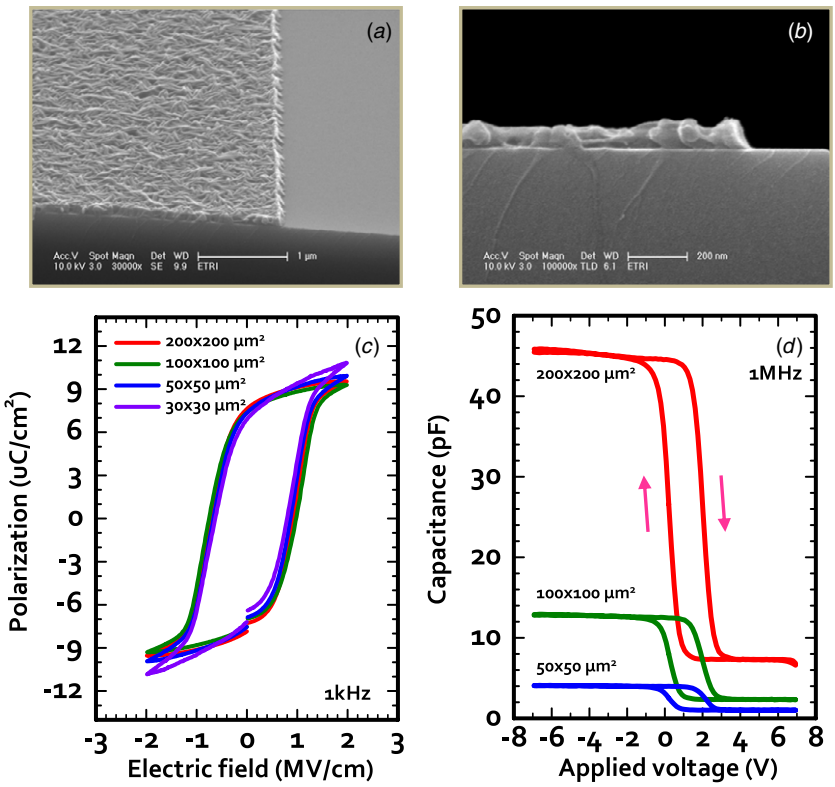

Figure 8. SEM images of (*a*) a plane view and (*b*) a cross-section for the patterned P(VDF-TrFE) film. (*c*) Sets of *P–E* hysteresis loops for the capacitors with Al/PVDF-TrFE)/p^{++}-Si structures when the capacitor pattern sizes were varied from 200 × 200 to 30 × 30 μm^2. (*d*) *C–V* characteristics of the MFIS diodes with Al/P(VDF-TrFE)/Al_2O_3/p-Si structures when the pattern sizes were varied from 200 × 200 to 50 × 50 μm^2. The arrows shown in the figure represent the direction of hysteresis [117].

or Al_2O_3 [69], were inserted between the P(VDF-TrFE) and Si substrate in order to reduce the leakage current and to prevent the formation of the interdiffusion layer. Similarly, for the organic semiconductor-based MFIS structures, various organic insulator layers such as PVP [82, 120], poly(vinyl alcohol) (PVA) [120] or poly(styrene-γ-methylmethacrylate) [121] were introduced for obtaining the same effect. These roles of inorganic and organic interlayers are completely different from those of organic interlayers introduced to the P(VDF-TrFE)-insulator structures fabricated on the metal electrodes. In these structures, such organic layers as poly(3,4-ethylenedioxythiophene):poly(styrenesulfonicacid) (PEDOT:PSS) [20, 79], polypyrrole-poly(styrene sulfonate acid) (PPy-PSSH) [25] or polyethylenedioxythiophene/poly(stylene sulfonate acid) (PEDOT/PSSH) [24] were chosen to enhance the ferroelectric properties and/or to control the crystal orientation of the P(VDF-TrFE). On the other hand, for the cases of OfeOx-MTFTs, one of the most demanding roles of the interface buffer layer is to efficiently protect the surface of the oxide semiconductor channel during the fabrication procedures and to guarantee the interface quality, as mentioned above. Actually the device characteristics and reliabilities for the oxide-based TFTs are known to be significantly enhanced by the suitable preparation of an interface-controlling layer, the first GI. From this point of view, it can be sometimes called the 'protection layer' (PL) [122]. Park *et al* [96] reported the successful fabrication of transparent and photo-stable ZnO TFTs by preparing the Al_2O_3 PL layer, which was deposited by the ALD method using water vapor as the oxygen precursor. In these approaches, it was confirmed that the ALD process conditions for PL had a very critical impact on the interfacial properties [123, 124]. Figures 9(*a*) and (*b*) show cross-sectional transmission electron microscopy (TEM) images when the oxygen source of Al_2O_3 PL layers prepared on the ZnO were varied to water vapor and *in situ* O_2 plasma, respectively. As can be seen in the figures, while very smooth and clean interfaces between the layers could be obtained for the case of water-derived PL, the interfaces were considerably mixed and the ZnO surface was very rough for the case of plasma-induced PL. These observations were similarly reflected to the electrical properties for both cases, as shown in figures 9(*c*) and (*d*). When the PL was prepared by the O_2 plasma on the ZnO, large hystereses were measured in the *C–V* curves and the hysteresis width decreased with the evolution of successive voltage sweeps owing to the charge trapping/detrapping process at the interface. Consequently, in order to optimize the device and memory behaviors of the OfeOx-MTFTs, preparation methods as well as thickness condition for the interface buffer layer should be carefully controlled.

3.3. Solution process for the oxide channel

In the fabrication of the oxide semiconductor-based TFTs, the oxide channel layers have been mainly deposited by

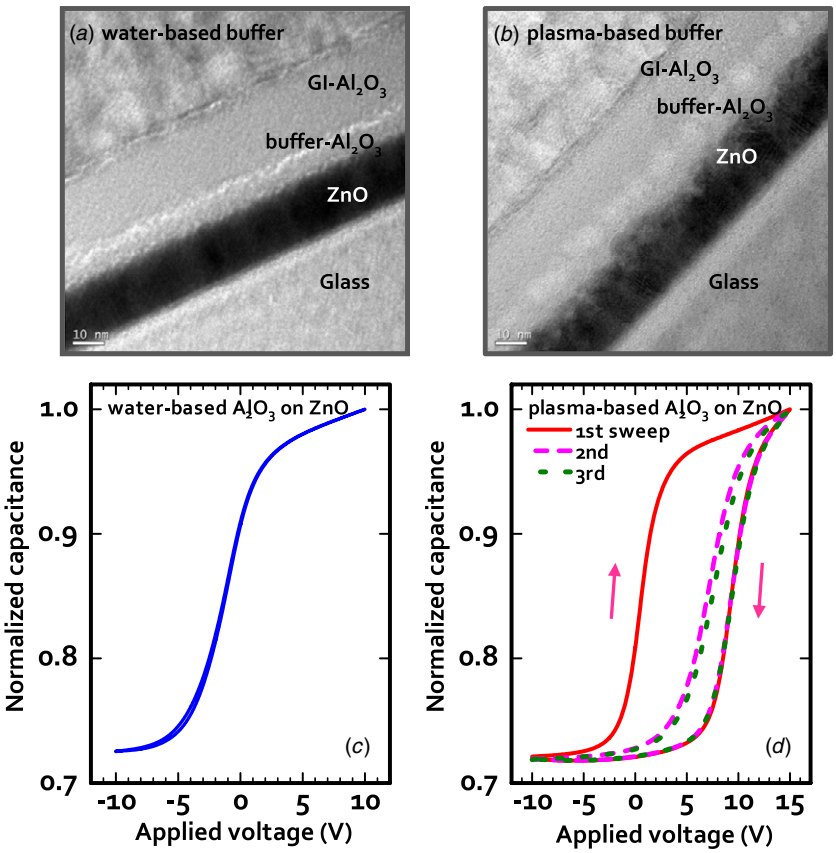

Figure 9. Cross-sectional TEM views of channel regions for the cases (*a*) when both insulator buffer and gate insulator layers of ALD-grown Al_2O_3 were prepared by using water vapor as the O_2 source and (*b*) when the insulator buffer was deposited by using *in situ* O_2 plasma [124]. Normalized *C*–*V* characteristics of MIS capacitors of Al/Al_2O_3 (GI)/buffer Al_2O_3/ZnO when the ALD-grown buffer Al_2O_3 was prepared by (*c*) water vapor and (*d*) O_2 plasma. In (*d*), the measurements were repeated three times to confirm the charge trapping/detrapping process at or near the interface. All measurements were performed at 1 MHz [123].

sputtering [125–130] and pulsed-laser deposition (PLD) [89, 94] methods. Sometimes ALD [122, 131] or metal-organic chemical vapor deposition (MOCVD) [132] methods were employed for the deposition of the ZnO active channel. These deposition techniques are basically classified into vacuum-deposition-based processes. On the other hand, the solution-based process for the oxide channel layer can be an alternative powerful approach for the next-generation large-area electronics, because it provides a simpler process design, lower process cost and higher throughput with shorter turnaround time. Recently many publications have reported successful demonstrations of the oxide TFTs using the solution-processed oxide channel layers such as ZnO [133–135], IGZO [136–138], indium-zinc oxide (IZO) [139, 140], zinc-tin oxide (ZTO) [141–143], aluminum-indium oxide (AIO) [144], zinc-indium-tin oxide (ZITO) [145], hafnium-indium-zinc oxide [146], yttrium-indium-zinc oxide [147] and aluminum-indium-tin oxide [148]. Samsung Electronics demonstrated their first prototype AM-OLED display panel using solution-processed IZO TFT [149]. It is also very attractive to apply the solution-processed oxide active channel to the OfeOx-MTFTs, in which the formations for the semiconducting channel and the ferroelectric gate insulator can be successively processed in a very simple manner. Successful combinations of the spin-coated P(VDF-TrFE) GI with the solution-processed oxide channel have recently been attempted by Yoon *et al* [150–152] as one of the challenging issues for OfeOx-MTFTs. Figure 10(*a*) shows the XRD patterns of the solution-processed ZTO films treated at various temperatures, which indicates that the prepared films are basically amorphous phases. The surface of 400 °C-annealed ZTO film was also confirmed to be very smooth and homogeneous without any crystalline grains, as shown in figure 10(*b*). The OfeOx-MTFTs employing the spin-coated ZTO films showed marked differences in device and memory behaviors with the variations in channel composition and annealing temperature. As shown in figure 10(*c*), significant improvement in OfeOx-MTFT performances could be obtained for the 50/50 mol% ZTO channel annealed at 500 °C, in which the field-effect mobility and *on*/*off* ratio were measured to be 15.8 $cm^2\ V^{-1}\ s^{-1}$ and 6.4×10^7, respectively [152]. Furthermore, it was also found that the initial carrier concentration of the oxide channel had an important effect on the memory margin, which was expressed as the MW and memory *on*/*off* ratio (figure 10(*d*)). One of the critical problems for the conventional oxide TFTs as well as the OfeOx-MTFTs fabricated by the solution process is that the post-annealing process at a temperature of higher than 400 °C is required for deducing applicable device performances, even though the devices operate even at a 300 °C process [150].

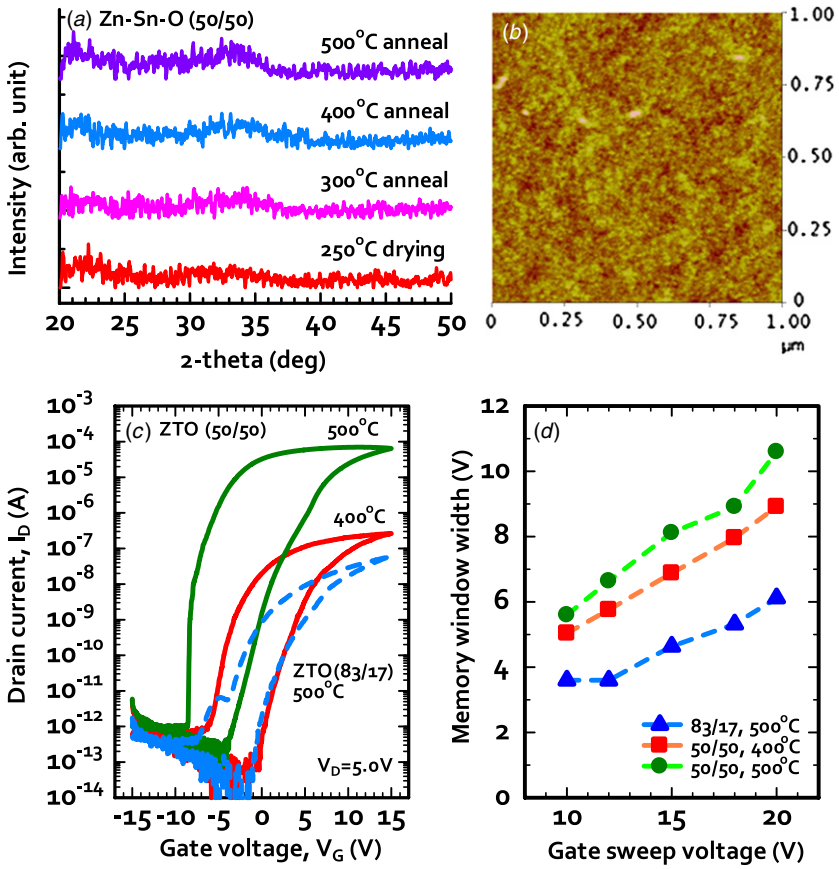

Figure 10. (*a*) XRD patterns for the solution-processed ZTO films at different annealing temperatures of 250, 300, 400 and 500 °C. The molar ratio of Zn/Sn was 50/50 mol%. (*b*) AFM images of surface morphologies for the 400 °C-annealed ZTO films with 50/50 molar ratio. (*c*) I_D–V_G characteristics of the fabricated OfeOx-MTFT with the 50/50 mol% solution-processed ZTO channel, in which the annealing temperature for the ZTO channels were varied to 400 and 500 °C. (*d*) Variation in memory window width for each OfeOx-MTFT when the molar ratio of the ZTO channel and the annealing temperature were varied [152].

Therefore, in order to employ the solution-based process for the large-area electronics implemented on low-cost glass or plastic substrates, new materials and process techniques to reduce the thermal budget should be intensively investigated as future works.

4. Issues of promising applications

It is important to define the suitable applications for the proposed OfeOx-MTFTs. Because the different specifications may be required for each application, the device performances should be appropriately developed to meet them. In this section, some feasible and promising fields to apply the embeddable OfeOx-MTFTs are introduced.

4.1. Transparent memory

In the field of highly functionalized 'consumer electronics', fresh design concepts also become an impressive demanding factor. In this viewpoint, 'see-through' electronic devices featuring transparency to visible light can provide us with a totally new experience and specified functions. These approaches also have a significant meaning in that transparent electronic appliances can be completely harmonized with our ambient. A transparent display panel composed of AM-OLED and oxide TFT backplane is one of the most typical examples [153–156]. In realizing highly functional transparent integrated systems having such features as lower power consumption, information storage and interactive networking, embeddable transparent memory devices are strongly required. Although some types of transparent memory devices have been demonstrated so far, several technical drawbacks and issues still remain for practical applications. Typically, charge-trap-type TFTs using an oxide semiconductor channel exhibited nonvolatile memory functions [157, 158], in which a thin layer or nanoparticles for the charge-trapping were prepared within the gate stack. However, they generally require a very complicated fabrication process to prepare the charge-trap sites and strict program/erase conditions to precisely control the quantity of trapped charges. An asymmetric program/erase characteristics with a small erase window and a very difficult hole injection into the IGZO make for a critical limitation in memory operations. Resistive-change-type devices with sandwiched structures of transparent conducting oxide (TCO)/oxide layer/TCO [159–161] or TCO/organic layer/TCO [162, 163] were proposed. Because these devices just operate as resistors having variable conductance controlled by applying voltage signals, driving circuitry should be suitably devised for the cross-point array integration. On the

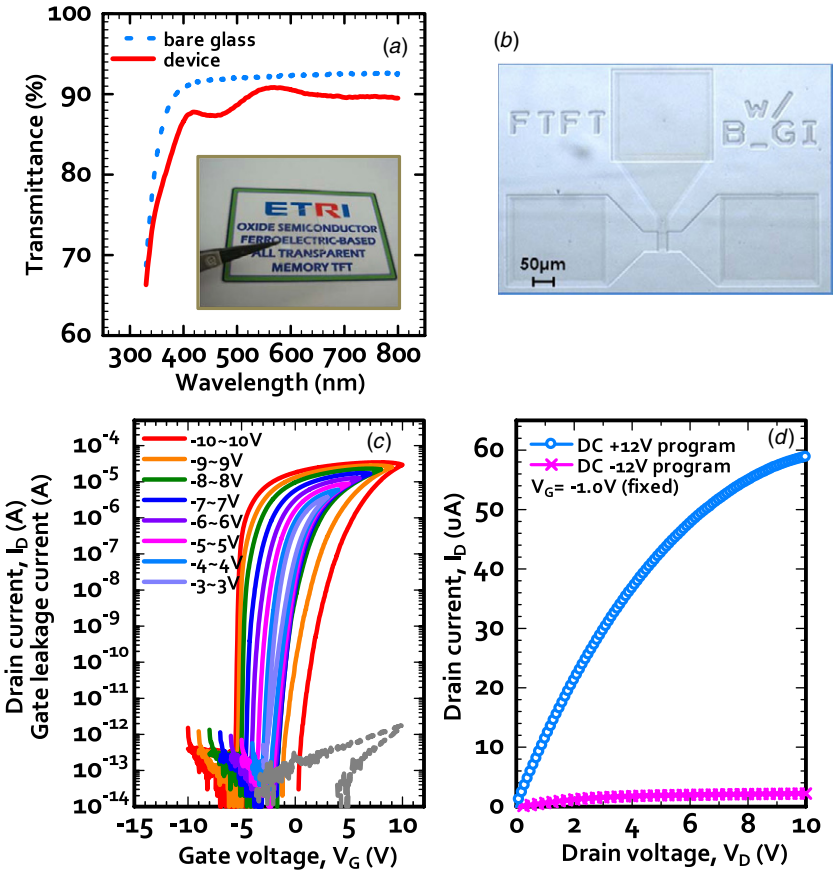

Figure 11. (*a*) Transmittance of the transparent OfeOx-MTFT fabricated on the glass substrate in the visible range. The inset shows the optical image of the transparent glass substrate on which the transparent OfeOx-MTFTs were fabricated. The substrate size was 2×2 cm^2. (*b*) Photograph of the OfeOx-MTFT with ITO/P(VDF-TrFE)/Al_2O_3/AZTO/ITO S/D structure, which was taken under the illumination from the backside of the substrate. (*c*) Sets of I_D–V_G transfer curves of the transparent OfeOx-MTFT when the V_G sweep ranges increased from ± 3 to ± 10 V. (*d*) I_D–V_D output characteristics after the V_G sweeps from 0 to 12 V (circle) and from 0 to -12 V (cross) at the same V_G of -1.0 V [167].

other hand, the OfeOx-MTFTs can be sufficiently feasible for the nonvolatile memory devices embeddable into the transparent electronic systems when the TCO is used for metal electrodes and interconnections. Prins *et al* [164, 165] presented pioneering works on the transparent memory transistors using $PbZr_{0.2}T_{0.8}O_3$, Sb-doped SnO_2 and $SrRuO_3$ as an oxide ferroelectric GI, an n-type active channel, and a gate electrode, respectively. However, a relatively high temperature around 600 °C was inevitably necessary for the crystallization of the oxide ferroelectric insulator, substrate availabilities were very limited to be $SrTiO_3$ single crystal or sapphire (c-Al_2O_3) [166].

Fully transparent nonvolatile OfeOx-MTFT was successfully demonstrated by Yoon *et al* [167]. Optical transmission spectra of the OfeOx-MTFT fabricated on the glass substrate exhibited a transmittance of approximately 90% at a wavelength of 550 nm, as shown in figure 11(*a*), in which aluminum-zinc-tin oxide (AZTO) [126] and ITO were chosen as the oxide active channel and transparent electrodes, respectively. The test vehicle including the OfeOx-MTFTs is quite transparent. Figure 11(*b*) shows an optical microscope image for the fabricated transparent device, which was taken by illuminating from the backside of the substrate. The OfeOx-MTFT showed excellent device operations, as can be seen from the measurement of transfer curves shown in figure 11(*c*). The field-effect mobility at the linear region, SS, *on*/*off* ratio, MW at the V_G sweep of ± 10 V and gate leakage current were successfully obtained to be 32.2 cm^2 V^{-1} s^{-1}, 450 mV dec^{-1}, 1×10^8, 7.5 V, and 10^{-13} A, respectively. It was also observed that the MW increased in almost a symmetrical way toward both directions with the V_G sweeps, which reveals that undesirable charge trapping at the interfaces was negligible. The memory operations could also be confirmed by the variations in I_D between the *on* (12 V) and *off* (-12 V) programming from the measurements of output curves, as shown in figure 11(*d*). Park *et al* [168] also reported the transparent OfeOx-MTFT, in which ZnO and IZO were used as the oxide active channel and gate electrode. The transmittance and field-effect mobility were reported to be approximately 80% and 0.1 cm^2 V^{-1} s^{-1}, respectively. One of the most critical issues for the fabrication of the transparent OfeOx-MTFTs is to form the transparent gate electrode patterns on the surface of P(VDF-TrFE). Because the polymeric film of P(VDF-TrFE) might be easily degraded by the plasma process engaged into the sputtering of TCO [169, 170], plausible plasma damage should be minimized. The second issue is related to the photo-response of the transparent OfeOx-MTFTs. Electrical characteristics of the

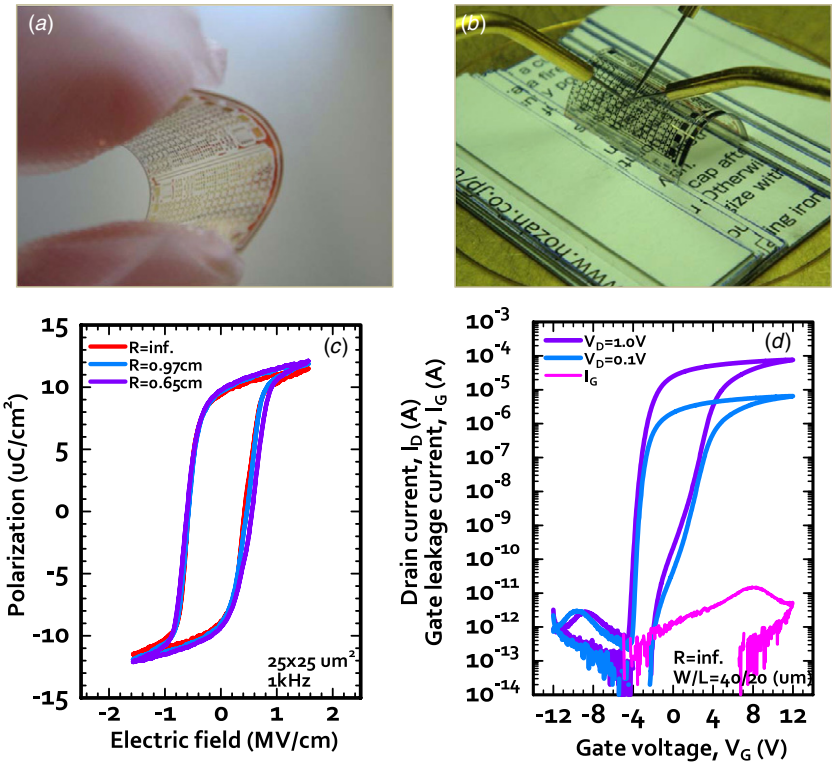

Figure 12. A typical photo image of the PEN substrate under a bending situation after the device fabrication process was completed. (*b*) Photo-image of the situation for electrical evaluation when the processed PEN substrate was bent with R of 0.65 cm. (*c*) Comparisons of the ferroelectric P–E characteristics of the Au/P(VDF-TrFE)/Au capacitor at the applied voltage of 30 V when the R was varied to ∞, 0.97 and 0.65 cm [193]. The capacitor size was 25 × 25 μm^2. (*d*) I_D–V_G characteristics and gate leakage current of the OfeOx-MTFT with the Au/P(VDF-TrFE)/IGZO/PEN structure. The gate width and length were 40 and 20 μm, respectively.

device may be significantly affected even by the visible light owing to their transparency. Therefore, the photo-induced effects under various illuminated environments should be systematically investigated as future works. On the condition that device physics and fabrication processes are optimized, the OfeOx-MTFTs can be expected to provide novel technical solutions to future transparent electronics.

4.2. Flexible memory

Flexible electronic systems integrated on a bendable or rollable plastic substrate configure another important application field of a new paradigm of modern 'consumer electronics'. In recent times, various interesting approaches in this field have been actively researched and developed. Radio-frequency identification tags [171–173], flexible sensor arrays [174–176], flexible and stretchable displays [87, 177, 178], flexible electronic circuits [179–181] and sheet-type communication systems [182] correspond to feasible examples. These systems necessarily need an embeddable nonvolatile memory element. Therefore, if the memory devices having features of mechanical flexibility, lower power operation, simpler process at lower temperature and higher device reliability can be successfully provided, it would have a great impact on the related fields. So far, several approaches using different material combinations and operating origins have been tried to realize the memory devices on the flexible plastic substrates. They can be classified into (1) resistance change types using the redox reaction in organic layers [183, 184] or filament formation within organic layers between the electrodes [185], (2) resistance change types using binary oxide thin films [160, 186], (3) charge injection types with specified device structures as the organic bilayer [184, 187], organic composite [188] or nanoparticle-embedded organic layers [189, 190], (4) floating-gate-type transistors using organic semiconducting channels [191, 192] and (5) ferroelectric-based TFTs [64, 82] being discussed in this paper. Although, in this application, the polymer or pentance-based organic semiconductors have been mainly chosen as active channels for the case of the ferroelectric-based TFTs, the OfeOx-MTFT can also be a good candidate. Because the oxide channels are patterned into only small gate areas on the substrate, a relatively brittle nature of oxide film will no longer be a fatal problem for flexible electronic devices. Figure 12(*a*) shows the photo image of the processed plastic polyethylene naphthalate (PEN) substrate on which Au/P(VDF-TrFE)/Au capacitors and Au (gate)/P(VDF-TrFE)/IGZO/Au (S/D) TFTs were fabricated [193]. The substrate was bendable and a series of electrical measurements could be performed by setting the proving system, as shown in figure 12(*b*). The sound characteristics of the ferroelectric capacitors fabricated on the PEN were well confirmed and the ferroelectric properties were not so changed with the variation at the curvature radius under the

substrate bending, as described in figure 12(*c*), which was also demonstrated by Matsumoto *et al* [194]. Figure 12(*d*) shows the transfer curve for the OfeOx-MTFT fabricated on the PEN substrate. The device characteristics cannot be said to be sufficiently good yet owing to the back-channel effect caused by the rough surface of PEN and the unavailability of high temperature annealing at around 250 °C for the IGZO channel. Consequently, the critical issues for enhancing the performances of the flexible OfeOx-MTFTs can be summarized as follows. The suitable choice of a plastic substrate with such features as high temperature compatibility, low thermal expansion coefficient and low coefficient of moisture absorption is very important, which are common and general issues in launching the flexible electronics. The oxide channel material should be developed and optimized so as to obtain the best performances in both current drivability and device stability even at a temperature of lower than 200 °C. The improvement in device performance of the OfeOx-MTFT loaded onto the flexible substrates is now in progress.

4.3. Other feasible applications

In the flat-panel display (FPD) field, the reduction of power consumption is one of the most urgent problems to solve. This requirement is attributed to the fact that TFT-LCD constantly pursues a higher contrast ratio and a faster response time for a larger panel size in the major FPD industries, and that the mobile information display with an ultra-low power is strongly demanded for recent 'consumer electronics'. The integration of memory cell into a pixel of display panel can be a very promising approach for lower power driving [195–199]. For the cases of previously proposed methods, the memory cell is composed of many transistors which occupy a large area and need some refreshing operations owing to their volatility. Eventually, merits of power reduction could not be sufficiently promoted for practical FPD applications. If we can integrate a nonvolatile memory cell with a simple structure into the pixel with driving circuitry, the power consumption of the panel could be effectively reduced. Considering that the oxide TFT backplane is very promising for the next-generation TFT-LCD or AM-OLED panels, OfeOx-MTFT is one of the best candidates for the power-saving memory component integrated with the pixel.

From the viewpoint of transparent electronics, CMOS configuration is very attractive, even though the p-type oxide TFT is as challenging as ever [200–203]. Oxide TFTs-based electronics featuring transparency are expected to be launched at a major scale if the oxide-CMOS technology is well established. The OfeOx-MTFTs can be utilized as nonvolatile memory elements in various applications for this oxide electronics. Especially, they can give a nonvolatility to the conventional logic circuits so that the system power of the integrated circuits employing the oxide-CMOS can be greatly saved. These logic-in-memory concepts have become very popular for realizing lower-power VLSI in the conventional Si-based electronics [204–206].

5. Issues of memory array integration

In order to fully make use of the proposed OfeOx-MTFTs, as discussed in the previous sections, the next considerations are to construct the array configuration and to integrate them with driver and logic circuitry. Although similar approaches using all-organic [182] or all-inorganic [207] material combinations have been proposed to provide the nonvolatile memory cell, they are not compatible for both transparent and flexible electronic devices. In advance, the establishment of the integration process for the memory cell composed of memory and switching devices is very essential. The memory cell should be so designed as to carry out the random access functions without cross-talk problems. In this section, we discuss the issues of memory array integration from those viewpoints.

5.1. Memory cell integration process

Two transistor-type nonvolatile memory cells were demonstrated by Yoon *et al* [208], in which the integration process of the memory cell composed of OfeOx-MTFT and oxide access TFT was proposed. Figure 13 provides the process flow for fabricating the OfeOx-MTFT-based memory cell and array by integrating with the oxide TFT-based peripheral circuitry on the same glass substrate. First, after the patterning of ITO for the formation of source and drain regions, the oxide active channel (ALD-ZnO in this work) and interface buffer (ALD-Al_2O_3 in this work) layers were deposited and patterned into the channel regions by wet etching (figure 13(*a*)). The ferroelectric GI film was formed by the spin-coating using a diluted solution of the P(VDF-TrFE). The prepared film was crystallized by performing the thermal annealing process at 140 °C for 1 h in an air ambient. Then given areas of the P(VDF-TrFE) layer were removed to prepare the space of oxide GI for the oxide TFT regions and to form the contact holes for the S/D contacts by O_2 plasma etching, in which the lithography compatible process was optimized as discussed in section 3.1 (figure 13(*b*)). Then, it was time to prepare the oxide GI (ALD-Al_2O_3 in this work) with an appropriate film thickness and to pattern it into the only channel region of oxide TFT (figure 13(*c*)). Here, we have to recall that the process temperatures and deposition methods after defining the P(VDF-TrFE) layer should be carefully designed, because the temperature of higher than 160 °C and/or the plasma-induced process may deteriorate the physical and chemical properties of P(VDF-TrFE). Finally, the metal or TCO layer was deposited and patterned as the gate electrodes and S/D pads. The temperature of the overall process could be designed to be below 200 °C. Figures 14(*a*) and (*b*) show a schematic circuit diagram and a microscopic photo image of the fabricated 2T-type memory cell, respectively. The *write* and *read-out* operations of the proposed 2T memory cell were evaluated as shown in figure 14(*c*). V_{GO} of the access oxide TFT and V_{GF} of the OfeOx-MTFT play roles of driving and programming gates for the memory cell, respectively. The memory states of *on* and *off* were initially programmed by applying the voltage pulses

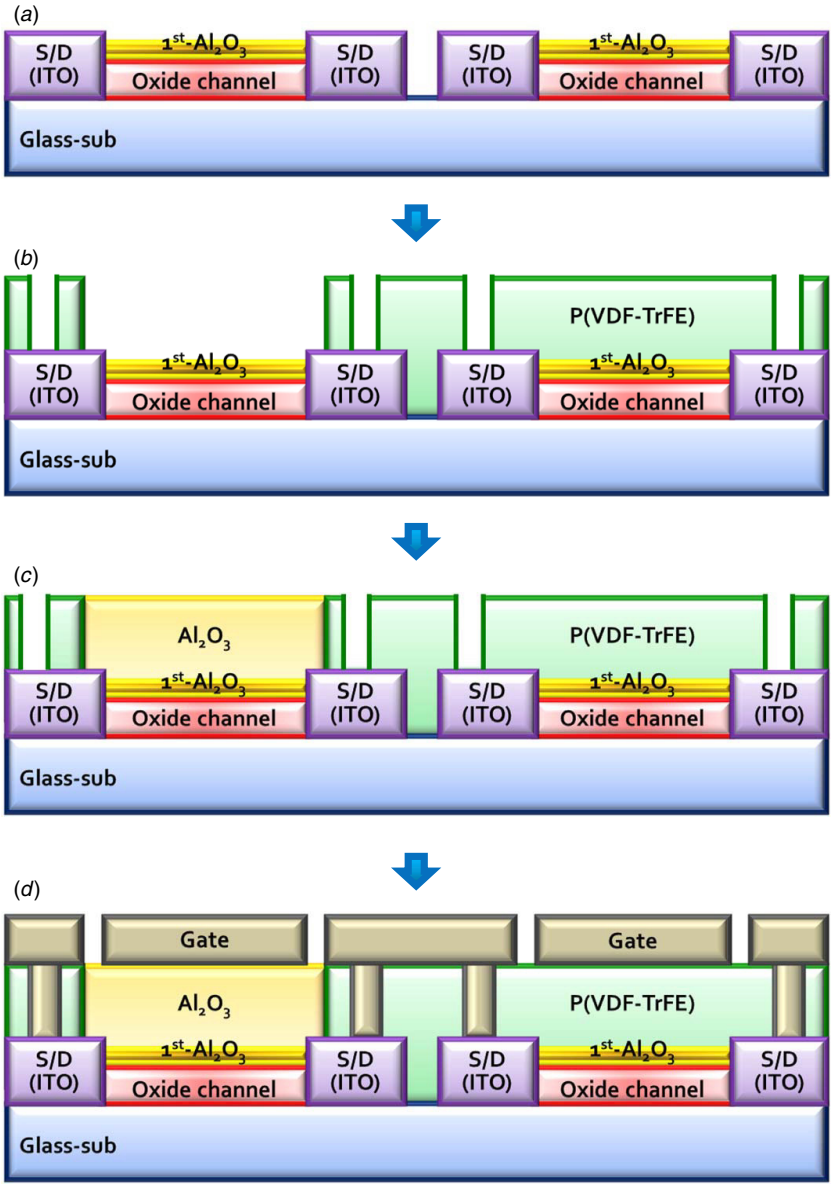

Figure 13. Process flow for the nonvolatile memory cell composed of OfeOx-MTFT and oxide TFT on the same substrate. (*a*) Oxide channel and insulator buffer (the first GI) layers were deposited and patterned into the gate areas of both TFTs. (*b*) Ferroelectric GI for the OfeOx-MTFT was coated and patterned. (*c*) Oxide GI (ALD-Al_2O_3 in this work) for the oxide TFT was prepared and patterned. (*d*) Gate electrodes and pads were finally formed [208].

of 20 and −20 V to the V_{GF}, respectively. The programmed I_{out} could be successfully modulated when the clock voltage signals applied to the V_{GO} were switched from −5 to 15 V. The I_{out}s of *on* and *off* states were observed to be approximately 10^{-7} and 10^{-10} A, respectively. Nondestructive *read-out* operations (NDRO) were also well confirmed for the 40 times repetitive measurements, as shown in figure 14(*d*).

5.2. *Disturb-free memory cell*

Because the previously demonstrated 2T-type memory cell is not suitable for the *write* and *read-out* operations in the memory array, the cell structure should be modified so that the data stored in the selected cell are not destroyed while accessing the other neighboring cells. Kim *et al* [209] proposed a new cell structure composed of two access oxide TFTs (MA and MB) and one OfeOx-MTFT (FM), as shown in figure 15(*a*). Figure 15(*b*) shows the timing diagram for the proposed memory array. To *write* a datum into the FT, V_{SCAN} goes high and the TA and TB are turned on. $V_{PROGRAM}$ conveys the datum to be stored in FT, maintaining the $V_{Ref.}$ and V_{OUT} at ground during the programming period. Data '1' or '0' are stored when $V_{PROGRAM}$ is set to be positive or negative voltage, respectively, by changing the polarization of the P(VDF-TrFE) GI. When V_{SCAN} goes low, TA and TB are turned off and the stored data are retained against further voltage fluctuations in $V_{PROGRAM}$ and V_{OUT}. To *read-out* the datum stored in FT, the potentials of $V_{Ref.}$ are set to be slightly above the ground level and V_{OUT} is fixed at the ground. Then V_{SCAN} goes high. While the current may flow through FT and the resultant potential rise

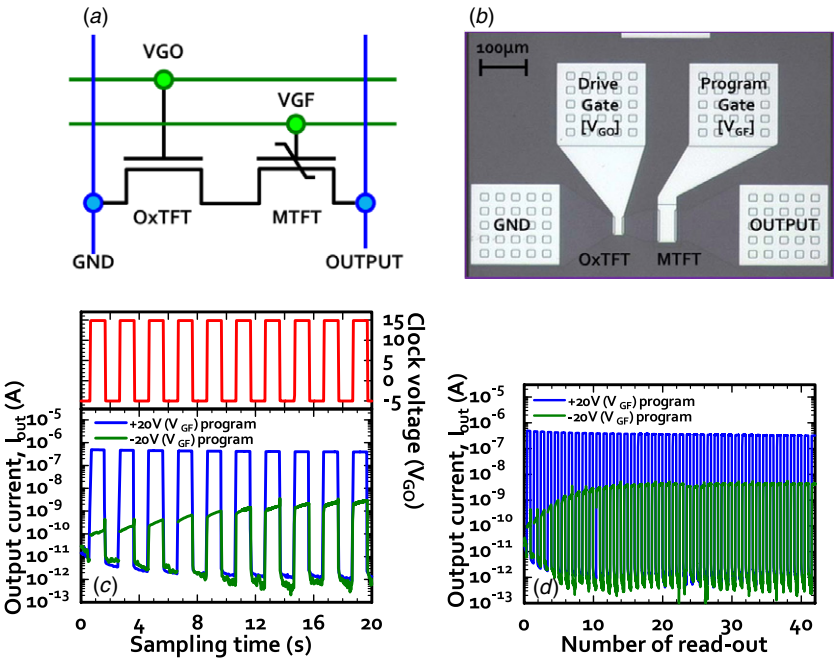

Figure 14. (*a*) Schematic circuit diagram of the proposed 2T-type memory cell composed of one OfeOx-MTFT and one OxTFT. V_{GO} and V_{GF} correspond to the drive gate of the OxTFT and program gate of the MTFT, respectively. (*b*) Photograph of the fabricated 2T-type nonvolatile memory cell. The gate widths and lengths (W/L) of OxTFT and MTFT were 40/20 μm and 80/40 μm, respectively. (*c*) Variations in I_{out}s of the memory cell with the time evolution when the gate clock voltage signal was continuously applied to the V_{GO}, which was switched from -5 to 15 V with the duration of 1 s as described in the upper graph. The programming events for *on* and *off* were previously performed by applying the *write* voltages of 20 and -20 V, respectively. (*d*) Example of NDRO for the *on* and *off* memory states, which were measured with an interval of 1 s by applying the gate clock signal shown in (*b*) [208].

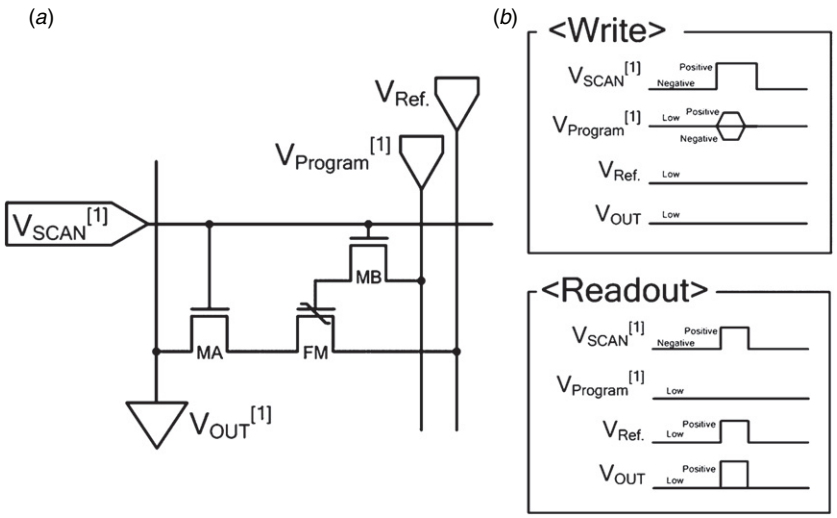

Figure 15. (*a*) Circuit diagram of the proposed memory array for the disturb-free *write* and *read-out* operations and (*b*) timing diagrams for each operation. MA and MB correspond to two oxide TFT switches and FM is the OfeOx-MTFT [209].

in V_{OUT} is detected by an external sense amplifier for the case of '1', no potential rise may be observed for the case of '0'. When it was compared to the previously proposed 3T memory cell [182], the number of long-line per pixel can be reduced from 5 to 3.5 by introducing this proposed cell structure. Figures 16(*a*) and (*b*) show the photo images of actually fabricated memory cell. The *write* and *read-out* operations were well confirmed when the programming signals of $\pm$10 V and 1 s were applied, as shown in figure 16(*c*). The output current was modulated between the range from approximately 10^{-12} to 10^{-7} A by performing the alternate *write* operations from '0' to '1' memory state. The disturb-free memory operations were also evaluated by carrying out intentional cross-talk tests. Figures 16(*d*) and (*e*) represent the *read-out* output currents for the '0' and '1' memory states after applying the signals to program the opposite memory states

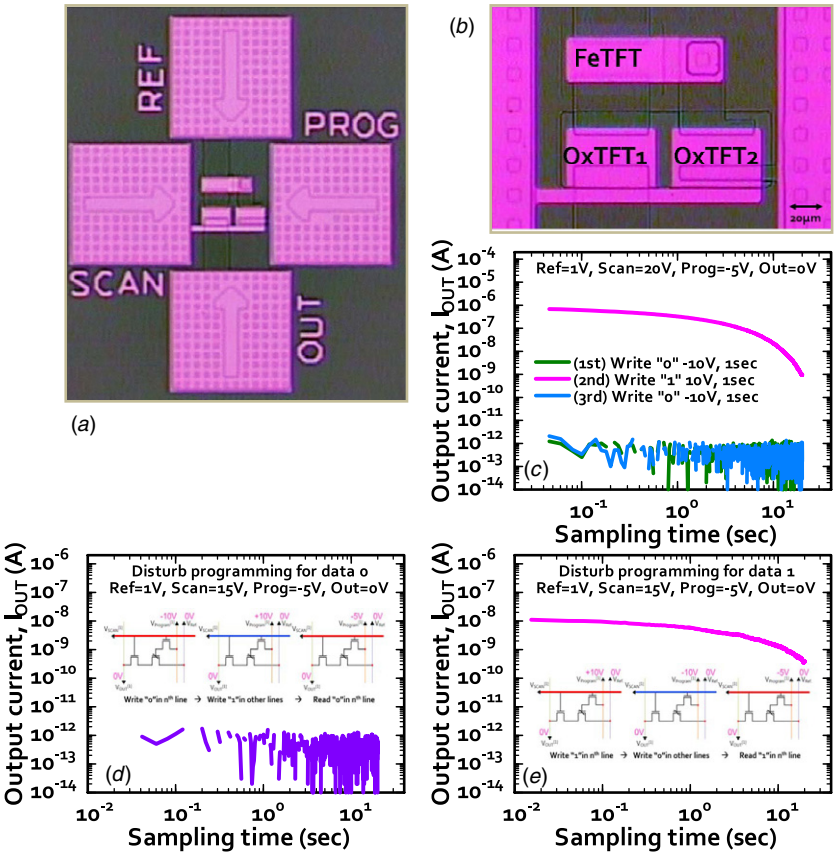

Figure 16. (*a*) Microscopic optical image and (*b*) its magnified view of the fabricated memory cell with two oxide switch TFTs and one OfeOx-MTFT. (*c*) Typical *write* and *read-out* operations of the proposed memory cell. Programming events for the '0' and '1' states were carried out by applying the voltage signals of −10 V, 1 s and 10 V, 1 s, respectively, in which the voltage biases for $V_{\mathrm{Ref.}}$, V_{SCAN}, V_{PROGRAM} and V_{OUT} were set to be 1, 20, −5 and 0 V, respectively. Cross-talk tests for (*d*) data '0' and (*e*) data '1' were evaluated, in which the programmed I_D for the selected cell was monitored after the neighboring cells were written in the opposite state [209].

to the neighboring cell in other lows, respectively, which were initially stored in the selected cell. It was very inspiring to confirm that the previously stored data into the selected cell were disturb-free for the proposed memory array configuration.

6. Remaining issues

In previous sections, the technical feasibilities and promising methodologies for utilizing the proposed OfeOx-MTFTs as core memory devices of the future transparent and flexible electronics were discussed. However, some challenging issues remain to satisfy the specifications required as the practical-level nonvolatile memory element for commercialized applications. Such remaining issues as lower voltage operation, higher programming speed and better device reliabilities including the data retention are discussed and appropriate solutions are considered in this section.

6.1. Low voltage operation and turn-on voltage control

The reduction of programming voltage for the OfeOx-MTFT is one of the most important issues for most practical applications. For these memory devices, the definition of the operating or programming voltage is somewhat ambiguous. Here, we define it as the voltage with which we can guarantee a given memory *on*/*off* ratio in programmed I_Ds of the OfeOx-MTFT. Sometimes, it is defined as the voltage required to obtain a given MW in transfer curves measured in forward and reverse sweeps in V_G. Anyway, assuming that the memory *on*/*off* ratio of more than at least 100 is required, the programming voltage of the OfeOx-MTFT has been reported to be in the range from ±20 to ±15 V [100–102, 104, 105, 168]. Although these values are lower than those for the organic channel-based memory TFTs [26, 120, 182], an aggressive reduction to below 10 V is strongly demanded. Sekitani *et al* [176] correctly pointed out that it would be very difficult to obtain a large enough MW with the program voltage below about 20 V owing to the large coercive field of organic ferroelectrics. Nevertheless, we still have some available strategies for realizing the lower voltage operations of the OfeOx-MTFTs by carefully designing the device structures, as discussed in section 2.1. Especially, it can be expected that the use of the oxide-based channel extends the design margins thanks to the established deposition techniques dealing with a thinner film. It was also good news that the coercive field of the nanopatterned ferroelectric domain could be greatly reduced to about 100 kV cm^{-1} [110], which is comparable to those for the conventional oxide ferroelectrics. To replace the PVDF-based copolymers by the new organic ferroelectric material with a

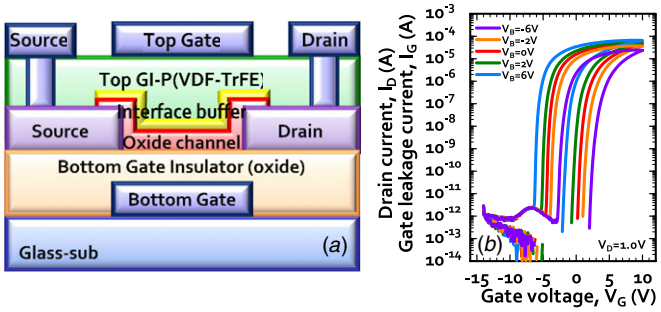

Figure 17. (*a*) Schematic cross-sectional diagram of the proposed dual-gate OfeOx-MTFT. (*b*) Variations in I_D–V_{TG} characteristics of the dual-gate OfeOx-MTFT when the fixed bias of BG was changed from −6 to 6 V [211].

lower coercive field will also be a good approach to reduce the programming voltage. Croconic acid, which has recently been reported to have the coercive field of approximately 30 kV cm^{-1} at the frequency of 100 Hz [18], can be a promising candidate.

On the issue of transistor behaviors, the control of V_{on} is also important. The OfeOx-MTFTs are absolutely desirable to be operated in an enhancement mode. Otherwise, it is very difficult to design the driving circuits for the memory array configuration owing to the unwanted current components from unselected memory cell even at the V_G of 0 V. This requirement is also significant in that the MW of the OfeOx-MTFT is preferred to be located with centering around 0 V in V_G, which is very favorable to obtain a longer retention time for the programmed data, as also will be discussed in section 6.3. Unfortunately, the V_{on}s of oxide TFTs as well as the OfeOx-MTFTs are typically determined below than 0 V. Post-annealing process is one of the good methods to shift the V_{on} to the positive direction in V_G [101, 210]. The implementation of the OfeOx-MTFT with a dual-gate (DG) structure enables us to control the V_{on} in a more systematic way [211]. Figure 17(*a*) shows the schematic cross-section of the proposed DG-structured OfeOx-MTFT, in which 10 nm thick IGZO and 70 nm thick ALD-grown Al_2O_3 were chosen as the common oxide channel and bottom GI, respectively. The V_{on} of this DG-OfeOx-MTFT could be dynamically controlled from −2.1 to 2.0 V when the bias voltage of the bottom gate was varied from 6 to −6 V without any change in MW, as shown in figure 17(*b*). As discussed in this section, suitable countermeasures should be considered so that both program voltage and V_{on} could be optimized for given applications.

6.2. Programming speed

The required voltage pulse width for the stable programming event is directly related to the programming speed of the OfeOx-MTFT. According to many works, the ferroelectric-driven programming actions were examined by applying the voltage pulses of longer than 1 s [27, 29, 102, 120] or by sweeping the dc voltages [30]. Although some publications have reported relatively short switching times of the P(VDF-TrFE)-based memory TFTs in the range from 50 μs to 40 ms [26, 79, 182], even these values are considerably larger than those obtained for the P(VDF-TrFE) capacitors sandwiched by top and bottom electrodes [20, 23, 212]. These long switching time for the cases of TFT can be explained by combining two factors of (1) the formation of a fully depletion layer in the semiconducting channel (as discussed in section 2.1) and (2) the RC time constant generated by the product of the S/D channel resistance and gate capacitance [35, 79, 164]. We have to note that the switching time for the polarization reversal of P(VDF-TrFE) thin film is very sensitively dependent on the amplitude of the electric field across the film [23, 70, 212–214]. Actually, for the case of ultra-thin P(VDF-TrFE) capacitor, the fastest observed switching time of 25 ns at a higher electric field of 8.4 MV cm^{-1} was reported by Nakajima *et al* [35]. The strong dependence of the programming speed of the memory TFTs on the programming electric field was also apparently observed, irrespective of the active channel types of organic or oxide semiconductor thin films. Because the switching time is known to exponentially decay with 1/E [70], a slight reduction in the amplitude of programming voltage may markedly impede the switching events. Eventually, this discussion reveals that it is very difficult to simultaneously optimize both important issues of lower voltage and higher speed operations. The employment of a thinner P(VDF-TrFE) gate insulator can be desirable in enhancing the program speed as well as in reducing the program voltage. However, this approach is based on the premise that the ferroelectric nature of the thin film can be well optimized even when its thickness is reduced. The increase in the gate leakage current for the case of a thinner film should also be considered.

For the OfeOx-MTFT with the structure of Al/P(VDF-TrFE)/Al_2O_3/ZnO, which was discussed in figure 4 before, the programming characteristics were systematically investigated [105]. The obtained programmed I_Ds in the *on* and *off* states and the programmable memory *on*/*off* ratio were summarized in figures 18(*a*) and (*b*), respectively, when the voltage amplitudes were varied to ±10, ±15 and ±18 V. If the memory margin is required to be no less than 10, the minimum duration of programming voltage of ±15 V could be estimated to be 50 ms. As expected, it was found that the programming pulses with higher amplitudes and longer durations were more effective to correctly program. However, it is also important to remember that there was a better condition to maximize the memory *on*/*off* ratio by avoiding undesirable charge injection, as can be seen from the results obtained for the ±18 V programming. In other words, it suggests that we cannot employ the excessively large programming voltages to enhance the switching event for the OfeOx-MTFTs, which is sometimes overlooked because it was not so easy to efficiently separate two phenomena of ferroelectric field-effect and charge injection for the memory TFTs using P(VDF-TrFE). These insights are also closely related to the evaluation of data retention behaviors for these devices. Anyway, at this stage, we have to admit that we do not have the best solution to improve the programming speed to be below several μs at a sufficiently low program voltage as high as 10 V. The variations in device structures such as the implementation of the DG device and/or the control of carrier

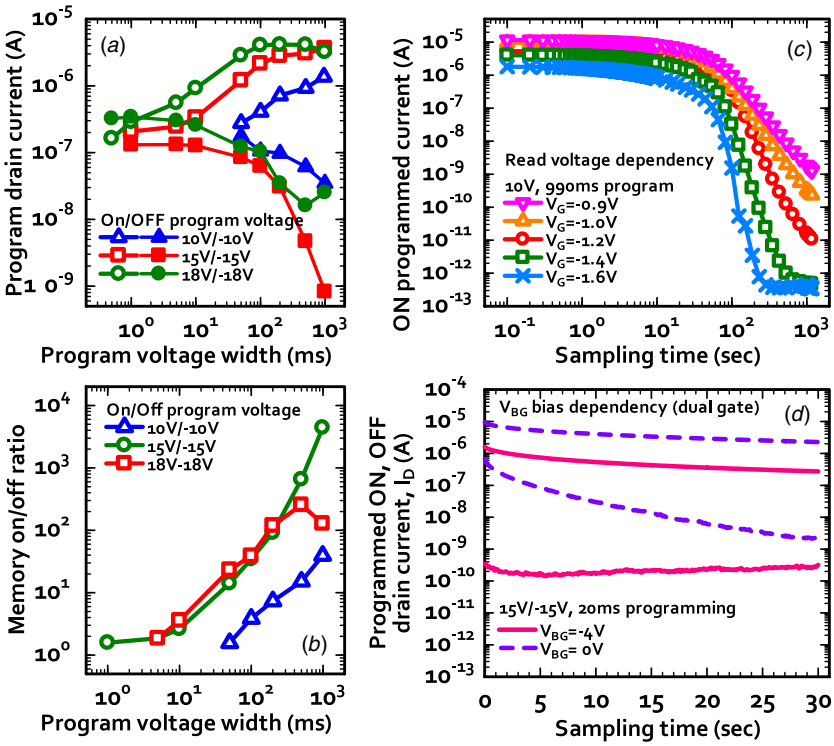

Figure 18. (*a*) Variations in the initially obtained I_D values for various programming conditions and (*b*) corresponding memory *on*/*off* ratios as a function of the pulse width of the programming voltage signal. The programming pulse amplitudes for *on*/*off* were changed to ± 10, ± 15 and ± 18 V. In these evaluations, the OfeOx-MTFT with the Al/P(VDF-TrFE)/4 nm thick Al_2O_3/5 nm thick ZnO structure was employed [105]. (*c*) Changes in the programmed *on* current with the time evolution at various bias conditions of $V_{G,\mathrm{read}}$. The *on* programming was performed by applying the voltage signals with 10 V and 990 ms. (*d*) For the dual-gate OfeOx-MTFT, variations in the programmed I_Ds of *on* and *off* states with the lapse of sampling time when the voltage bias of BG was changed from 0 to -4 V. While the stable memory ratio of 4.7×10^3 was obtained at the V_{BG} of -4 V, the *off* operation could not be conducted at the V_{BG} of 0 V [211].

concentration in the oxide channel layer can be effective for improving the operation speed issue.

6.3. Data retention

In fact, the retention property for the programmed data is the most demanding specification for using the OfeOx-MTFT as the nonvolatile memory device. For the case of oxide ferroelectric-based FeFET, the retention time has been continuously improved with the progress [51, 215, 216] and the longest retention times of approximately 30 days have been reported [217, 218]. The evaluated retention times for the reported OfeOx-MTFT are still in the range of 2 or 3 h [99, 100, 102, 104, 167, 168]. For the cases of ferroelectric-based memory TFTs using an organic semiconducting channel, which have been mainly proposed so far, the reported retention times were widely dispersed in the range from 200 s [80] to 15 h [82], although the longest retention time of 150 h was demonstrated by Naber *et al* [26]. Significant factors affecting the retention behaviors are classified into the intrinsic depolarization field, the gate leakage components and the interface quality. The depolarization field is subject to be naturally determined by the device structure, as illustrated in figure 3(*b*), and hence fatalistic detrimental effect was given to the device. This is one of the reasons why one-transistor-type FeFET could not be finally commercialized in replacement of the capacitor-type ferroelectric memory cell. Figure 18(*c*) clearly shows that even a slight variation of the depolarization field makes a big difference in the retention behavior of the OfeOx-MTFT [105, 169], in which the *read-out* and retention condition for V_G was varied to modulate the amplitude of the depolarization field during the retention phase. Therefore, it is very important to use a fully saturated ferroelectric saturated hysteresis loop for obtaining more stable memory operations with the lapse of retention time [46, 60], as explained above. Consequently, it is absolutely desirable to correctly program the memory states with the best programming conditions of pulse amplitude and duration, as discussed in section 6.2, so that the ferroelectric polarization could be completely switched at each programming event. However, unfortunately, for the OfeOx-MTFTs, the employment of the saturated loop is not so simple because of the large coercive field of P(VDF-TrFE) and the formation of the depletion layer within the oxide channel. Eventually, the operating points for the OfeOx-MTFTs at programming phases are likely to set up on the minor loops. The fact that the fully depleted semiconductor channel is unable to supply the compensation charges at the *off* state also works as a bad pill for the retention performance. The formation of thinner P(VDF-TrFE) films without degrading their performance is also important for the improvement of retention as well as for the reduction of program voltage. On the other hand, the effects of the organic ferroelectric material on the retention behavior have not been clearly understood, because most works have been focused on the use of the

P(VDF-TrFE). Nevertheless, if we can secure any new material having a good interface with the oxide channel, the retention property can be remarkably improved. A low dielectric constant, a low coercive voltage and an appropriate remnant polarization are required factors for using the fully saturated ferroelectric hysteresis loops during the programming events.

Sometimes, well-designed MFMIS structures can provide a useful solution to enhance the retention time [46, 60], if the increase in the device size is allowed. The OfeOx-MTFT with a DG structure was confirmed to obtain larger initial *on*/*off* ratio and more stable time evolution in the programmed I_Ds even at a relatively short signal of 20 ms by controlling the bias voltage of the bottom gate, as shown in figure 18(*d*) [211]. The introduction of the interface buffer layer, as discussed in section 3.2, is related to the reduction of the gate leakage and the improvement of the interface quality for better retention performance. The approaches to improve the insulating property of P(VDF-TrFE) by blending poly(methylmethacrylate) (PMMA) were also tried to enhance the retention performance of the MFIS diodes prepared on the Si substrate [68, 219]. On the other hand, the hypothesis that the use of the n-type oxide channel might be more unfavorable for obtaining good retention properties than the use of the p-type organic channel was mentioned in [102]. This is attributed to the fact that the P(VDF-TrFE) has n-type semiconducting characteristics, and hence the Fermi level is formed near the lowest unoccupied molecular orbital [220, 221].

Accurate evaluations for the OfeOx-MTFTs are also very important in the end because the analyses on programming operations exploiting the ferroelectric field-effect are sometimes very tricky. Memory hysteresis observed in the transfer curves of ferroelectric-based MTFTs (all-organic and hybrid) should be exactly distinguished from those obtained for the typical charge-trap nonvolatile memory devices, although the different origin can be figured out from the hysteresis direction with forward and reverse sweep in V_G [222]. The problem is that the ferroelectric GI-based MTFTs can also operate as if the ferroelectric polymer traps and detraps the injected charges at a typically higher program voltage and longer charging/discharging time [105]. For the oxide-based FeFET, the investigations on the variations in memory *on*/*off* ratio with the decrease in the pulse width of program voltage signal clearly show the types of source for the bistability, because the switching times of oxide ferroelectrics are in the range of several ns. In contrast, the slow switching time typically observed for the OfeOx-MTFT, as discussed in section 6.2, makes it difficult to show the ferroelectricity from the charge-trapping actions. Eventually, the ferroelectric-based data retention behaviors may be overestimated due to the working of charge trapping, because the injected charges are not easily discharged unless the large erase voltage is applied. Although, from this viewpoint, charge-trap-based MTFTs can also be said to be promising candidates with longer retention time for related nonvolatile memory applications, the origin itself is thermodynamically metastable and difficult to be correctly designed. Consequently, careful attention should be paid to the experimental data claiming the ferroelectric-driven nonvolatile memory actions if they were obtained by excessively large and long program voltage signals. As discussed in this section, there exist many complicated points of consideration related to the retention behaviors of the OfeOx-MTFT.

7. Outlook and summary

In this paper, the organic–inorganic hybrid-type nonvolatile memory TFT using a ferroelectric polymer and an oxide semiconductor as a gate insulator and an active channel, respectively, which was termed OfeOx-MTFT, was particularly overviewed from the device and process-related points of view. Such important issues as the device structure design, process optimization, promising feasible applications and memory array integration were comprehensively discussed and remaining technological issues were also picked up. In order to make the most of the superiority for the OfeOx-MTFT to all-organic memory devices, the device performance should be more improved from now on. Extension to the transparent and flexible memory array fabricated on plastic substrates or the specially functionalized circuit elements embedded into large-area electronic systems can be ultimate goals for the OfeOx-MTFTs. Perhaps, some breakthroughs in techniques should be made for reducing the operation voltage and for enhancing the retention and programming time characteristics. Because the organic ferroelectric GI has an important impact on the required behaviors of the OfeOx-MTFTs, the activity for the development of a new material is potentially effective and well directed.

However, considering a high level of difficulties to solve these problems, the exploration and determination of appropriate application fields may be the first thing that needs to be taken care of from a practical viewpoint. For the case of pentacene-based MTFT, some pioneering works [182, 223] by the Professor Someya and Professor Sakurai group provided excellent benchmarks. That is, it would be important that the performance improvements go side by side with developing killer applications suitable for already guaranteed device characteristics of the OfeOx-MTFT. It is natural that the applicable fields are differently defined as the systems demanding extremely low cost/low performance and relatively high performance between all organic-based MTFTs and the OfeOx-MTFTs, respectively. From this viewpoint, the solution-based printing methodologies [173, 224] including roll-to-roll techniques may be an essential process for the all-organic devices for effectively decreasing the process cost. The reviewed organic–inorganic hybrid OfeOx-MTFT is an interesting approach for the field of alternative nonvolatile memory and its advances in technologies are quite hopeful.

Acknowledgments

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