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Electrical Characterization of Metal-Insulator-Semiconductor Capacitors Having Double-Layered Atomic-Layer-Deposited Al_2O_3 and ZnO for Transparent Thin Film Transistor Applications

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The electrical characteristics of metal-insulator-semiconductor (MIS) capacitors with $Al/Al_2O_3/ZnO$ structures were investigated by capacitance–voltage (*C-V*) measurements. The ZnO films were prepared by plasma-enhanced atomic layer deposition as a common semiconducting layer. The insulators of Al_2O_3 were composed of a thin protection layer (PL), a first gate insulator, directly deposited on ZnO, and a main gate insulator by changing the oxygen sources (water vapor, in situ generated O_2 plasma, and ozone) during atomic layer deposition (ALD). When the PL was prepared by water, good electrical behaviors in *C-V* measurements such as no voltage hysteresis and normal flatband voltage (V_{FB}) were observed for the capacitors, regardless of the ALD condition for the deposition of the main gate insulator. For the MIS containing a PL deposited with O_2 plasma or ozone, the Al_2O_3/ZnO interfaces were markedly degraded, in which large hystereses and positive shifts of V_{FB} were observed.
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Oxide thin film transistors (TFTs) have great potentials for realizing future information-technology-related consumer electronics such as transparent displays,[1] ubiquitous electronic devices,[2] and transparent integrated circuits[3] owing to their transparency in visible range and compatibility to lower temperature process. Among them, the wide bandgap ZnO thin film, which has beneficial features of eco-friendly nature and low cost, has been one of the promising materials of semiconducting active channel layers for the aforementioned applications.[4-7] In TFT applications, one of the most important requirements is to obtain good reliabilities in device actions with guaranteed sufficient value of field-effect mobility. It demands careful consideration in overall aspects such as the deposition method of ZnO and device structures of the TFTs.

In optimizing the electrical properties of ZnO TFTs, the selection of a gate insulator (GI) is one of the most critical issues because the bulk and interface properties of the GI have important effects on the carrier concentrations, interface trap states, and field-effect mobilities of oxide TFTs. Several types of GIs such as SiO_2,[8,9] SiN,[9-11] high-*k* oxide insulators,[12-15] multilayered high-*k* dielectrics,[16,17] polymeric insulators,[18] and self-assembled nanohybrid dielectrics[19,20] have been employed to realize the low voltage and stable operations of the ZnO TFTs so far. Al_2O_3 prepared by atomic layer deposition (ALD) can also be a promising GI for the oxide TFTs including ZnO due to its low leakage currents, high dielectric constant, and high breakdown field.[21-24] A damage-free deposition mechanism at a lower process temperature during the ALD process can be desirable for improving the interfacial qualities between the ZnO especially for the top-gate structured TFTs. So far, the ALD-grown Al_2O_3 films have also been energetically investigated and adopted as a GI for the applications of conventional Si-based complementary metal-oxide-semiconductor field effect transistors (FETs),[25-27] FETs using wide bandgap semiconductors (InGaAs, GaN, and SiC),[28-30] and organic TFTs.[31,32]

However, in the fabrication process of ZnO TFTs, it was found from previous studies that the application of a thin first GI deposited before the formation of the main GI was very effective in improving the device characteristics because it protected the ZnO surface not to generate defects therein from the following patterning process using several organic solvents.[33,34] Thus, we call this first GI as a protection layer (PL) of ZnO. This PL, first GI, with thickness of less than 10 nm can control the interface properties between the ZnO and the main GI layers. The surface and bulk behaviors of ZnO may be sensitively affected by changing the process conditions of the PL. Therefore, the optimization of the ALD conditions for the PL and GI layers deposited on the ZnO is very demanding not only in realizing high performance ZnO TFTs but also in understanding related device physics. Irrespective of the technical importance for the TFT applications, the studies on the metal-insulator-semiconductor (MIS) systems, which are employed for the essential gate stack for TFTs, have not been much dedicated so far, for it is very difficult to clearly examine their behaviors due to the large quantities of intrinsic or extrinsic defects contained in the ZnO and the complicated interfacial situations between the oxide insulator.

In this study, we systematically investigated the electrical properties of MIS capacitors with Al/ALD-grown Al_2O_3/ZnO structures, in which the insulators were composed of double-layered PL and GI layers by choosing the combinations of oxygen sources for Al_2O_3 layers among water vapor, in situ generated O_2 plasma, and ozone. ZnO films were deposited by plasma-enhanced atomic layer deposition (PEALD) method in common. The influences of the combinations in process conditions for the PL and GI layers on the capacitance–voltage (*C-V*) characteristics of the MIS capacitors were mainly examined, in which those of the MIS capacitors using a p-type Si substrate as a semiconductor were also investigated for the comparison of the interfacial properties between two types of MIS capacitors. The *C-V* method can be a very effective tool to analyze the MIS capacitors having multiple interfaces between the ZnO and insulators. The choice of water vapor as an oxygen source during the ALD especially for the PL of Al_2O_3 could provide suitable conditions for guaranteeing excellent electrical behaviors of the $Al/Al_2O_3/ZnO$ capacitors.

Experimental

The stacked structure of the MIS capacitors using ZnO as a semiconducting layer was described in Fig. 1. A 150 nm thick indium tin oxide (ITO) film was deposited on the glass substrate by dc magnetron sputtering at room temperature for the bottom ohmic contact, followed by patterning using conventional lithography. ZnO thin films were deposited on ITO by PEALD at 200°C with diethylzinc (DEZ) and O_2 plasma as the Zn and oxygen sources, respectively. The oxygen plasma was generated in situ by applying a radio-frequency power of 130 W. The O_2 flow rate was 60 sccm and the reactor pressure was kept at 3 Torr. The pulsing times were 2.5 s for the DEZ, 4 s for Ar purge, 1.5 s for O_2 plasma, and 1 s for Ar purge. The thickness of the ZnO thin films was approximately 20 nm. The

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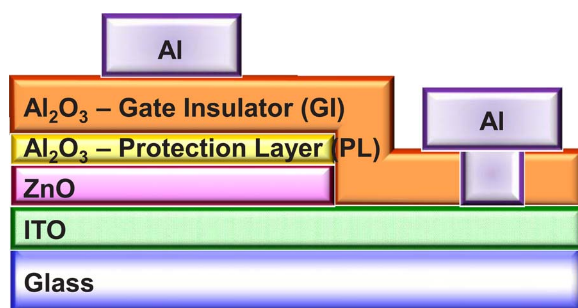

Figure 1. (Color online) Schematic cross-sectional diagram of the fabricated MIS capacitors using ZnO as semiconducting layers.

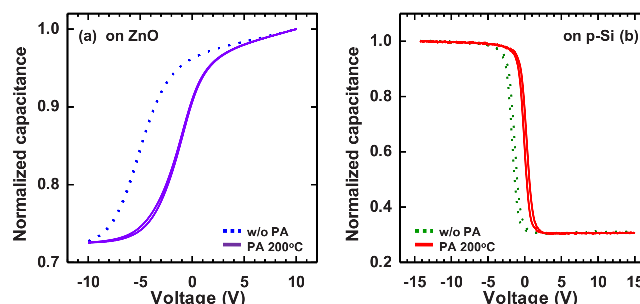

Figure 2. (Color online) Normalized *C-V* characteristics of MIS capacitors (termed as WW) using (a) ZnO or (b) p-Si as a semiconductor, in which the PL and GI layers of Al_2O_3 were prepared by using water vapor as oxygen source. All measurements were performed at the frequency of 1 MHz. The dotted and solid lines correspond to the behaviors before and after the post-annealing process at 200°C.

9 nm thin PL of Al_2O_3 was initially deposited on ZnO channel as the first GI with three different oxygen precursors at 200°C: water vapor, in situ generated oxygen plasma, and ozone. In each case, trimethylaluminum (TMA) was commonly used as an Al precursor. In the process of Al_2O_3 PL film deposition with water vapor, the pulsing times were 0.3 s for the TMA, 2 s for Ar purge, 1.5 s for H_2O, and 4 s for Ar purge, and the total number of process cycles was 90. In the process of Al_2O_3 PL film deposition with oxygen plasma, the pulsing times were 0.3 s for the TMA, 2 s for Ar purge, 1.0 s for O_2 plasma, and 2 s for Ar purge, and the total number of process cycles was 60. In the process of Al_2O_3 PL film deposition with ozone, 500 sccm O_2/2.5 sccm N_2 gas mixture was introduced into the O_3 generator and an O_3 gas at a concentration of 280 g/m^3 was obtained. The pulsing times were 0.8 s for the TMA, 4 s for Ar purge, 6 s for ozone, and 4 s for Ar purge, and the total number of process cycles was 108. After the pattering of ZnO and PL at once, 20 nm thick GI Al_2O_3 films were deposited in a similar way on each PL with water, oxygen plasma, and ozone by process cycles of 200, 143, and 250, respectively, followed by contact opening by wet etching of the Al_2O_3 using hot H_3PO_4. Then 100 nm thick Al was deposited by dc sputtering at room temperature. The electrode area of the capacitors was 9×10^{-4} cm^2. The stacks of the MIS capacitors were structured into Al/Al_2O_3/ZnO/ITO/glass. After fabricating the MIS capacitors, some devices were treated by post-thermal annealing (PA) at 200°C for 1 h in a N_2 ambient.

We also prepared some controlled devices using p-type Si substrates as semiconductors. The investigations on the *C-V* characteristics of the Al/Al_2O_3/p-Si can also provide us important information on the bulk properties of Al_2O_3 composed of PL and GI layers prepared with the same conditions for the Al/Al_2O_3/p-Si capacitors by completely separating the unknown factors related to the ZnO active layer. For these controlled devices, p-Si single crystal wafers with 1.5–4 Ω cm were employed. Si substrates were cleaned using a standard RCA cleaning method[35] and treated with a diluted HF solution to remove the native oxide just before the deposition of Al_2O_3.

For convenience, the prepared samples were notated with two capital characters, in which the first and second characters mean the deposition conditions of PL and GI layers, respectively. In other words, for the water–water (WW), water–plasma (WP), and water–ozone (WO) capacitors, PL was deposited using water and the deposition condition for the GI was varied to water, O_2 plasma, and ozone, respectively. Similarly, for the plasma–water (PW) and ozone–water (OW) capacitors, GI was deposited using water and the deposition condition for the PL was varied to O_2 plasma and ozone, respectively.

The *C-V* characteristics of the fabricated MIS capacitors were examined by using an impedance analyzer (HP 4194A). The measurement frequency was varied to 1 MHz, 100, 10, and 1 kHz. All measurements were carried out on the wafer with two-terminal probes without packaging in a conventional dark box at room temperature. The probe station used in the measurement only had a simple configuration without any special compensation appliances. We employed the measurement condition of the oscillation voltage level as 100 mV for comparison among all samples, although a low level signal of approximately 20 mV is typically set for *C-V* characterization. The data measured for some samples showed small fluctuations, and we had some difficulty in obtaining clear data sets at the small signal level of 20 mV. The current density–voltage (*J-V*) characteristics of the capacitors were also examined by using a semiconductor parameter analyzer (HP 4145B).

Results and Discussion

Figure 2a and b shows the *C-V* characteristics of the MIS capacitors (termed as WW) at the frequency of 1 MHz when both PL and GI layers were deposited using water on ZnO active layer and p-type Si substrate. The n-type nature of ZnO was clearly observed from the *C-V* curve, in which high capacitance was measured in the accumulation region at a positive bias voltage, and a low capacitance was measured in the depletion region at a negative bias voltage (Fig. 2a). Comparing with the MIS capacitor fabricated using p-Si, the curve was stretched out along the voltage axis. It means that the interface state density (D_{it}) of the ZnO capacitor is larger than that of the Si capacitor because these interface states should be charged during the *C-V* sweep. The D_{it} of the Al/Al_2O_3/p-Si capacitor shown in Fig. 2b was estimated to be approximately 3.6×10^{11}/eV cm^2 by the high frequency *C-V* technique.[36] As for the samples without postannealing, the negative shifts of the flatband voltage (V_{FB}) were observed. It implies that some charges with positive polarity exist within the GI. They are probably related to the low temperature process using water as an O_2 source during the ALD and eventually behave like fixed charges (Q_f). Considering that the quantity of the V_{FB} shift in the Si capacitor was smaller than that of the ZnO capacitor, the qualities of the PL and GI layers of Al_2O_3 grown by ALD may be dependent on the types of the lower layer. In other words, the atomic-layer-deposited ZnO might act as some source generating the fixed or mobile charges in the Al_2O_3 layers during the deposition process at 200°C, which is a completely different situation from the case using a conventional Si substrate. The V_{FB} could be recovered by postannealing at the temperature of 200°C for 1 h in an N_2 ambient, which suggests that the suitable post heat-treatment can improve the film quality and electrical characteristics of the capacitors. However, for the Al/Al_2O_3/ZnO capacitor, the slope during the transition from accumulation to depletion did not show any improvement even after the postannealing process. A good news was that there was no marked hysteresis for the ZnO capacitor in the up and down voltage sweep range of ±10 V. Hysteretic behaviors in the *C-V* curves are caused by the slow trapping of an injected charge carrier into the GI or migration of mobile ions in the GI. The nature of hysteresis can be speculated by its direction: For the n-type capacitors, counterclockwise or clockwise hysteresis

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indicates that its dominant origin is mobile ions or charge injection. Therefore, it can be concluded that the ZnO capacitor was almost free of mobile ions and induced charges when both the PL and GI layers of Al_2O_3 were prepared using water. This was also confirmed in the Si capacitor.

Here, we should discuss one important point related to this capacitor structure employing a 20 nm thick ZnO active layer. The measured normalized capacitances of the ZnO and Si capacitors correspond to the ratio of the minimum capacitance in the depletion region (C_{min}) to the maximum capacitance in the accumulation region C_{max}. The C_{min}/C_{max} ratio of the ZnO capacitor was approximately 0.73 at the voltage sweep of ± 10 V, which was much larger than that of the Si capacitor (approximately 0.31). Because the depletion capacitance (C_{dep}) of the MIS capacitors was composed of a serial connection of the GI capacitance and the depletion layer capacitance formed in the semiconductor, the depletion layer width (W_d) can be estimated from the C_{min}/C_{max} ratio,[22] assuming that the C_{min} is identical to the C_{dep}. The calculated W_d values of ZnO and Si capacitors were approximately 14.7 and 667 nm, respectively. Considering the carrier density of the employed p-type Si was approximately 2×10^{15} cm^{-3}, the value of W_d was quite reasonable.[36] However, it was found from the estimation that for the ZnO capacitor the maximum depletion width could not be obtained, and the W_d was limited to the thickness of the ZnO layer. This originated from the fact that the 20 nm thick ZnO layer was fully depleted with the evolution of voltage sweep in the *C-V* measurement. To solve this restriction in extracting useful parameters, such as the n-type carrier concentration of ZnO, and analyzing the capacitors using the conventional MIS theory, Song et al. prepared controlled devices by increasing the film thickness of ZnO to 300 nm.[22] Unfortunately, the polycrystalline ZnO layer being thicker showed rather different material behaviors compared to those of thinner ZnO films. Eventually, the evaluation of MIS capacitors with ZnO layers of less than 50 nm generally employed for the TFT applications is very difficult to perform with accurate quantitative studies. Therefore, the comparative studies using suitable controlled devices can be very useful to understand the related physics of the $Al/Al_2O_3/ZnO$ capacitors, which is one of the main objectives of this study. We confirmed from Fig. 2 that the ALD-grown PL and GI layers of Al_2O_3 using water as oxygen source were very appropriate to obtain quite good electrical properties of the MIS capacitor using ZnO as a semiconducting layer.

The saturation of the *C-V* curve at the accumulation region for the Si capacitor looks so different in the ZnO capacitor. The *C-V* curves for the ZnO capacitors did not show perfect saturation behaviors even when a significantly large voltage close to the breakdown field of the Al_2O_3 was applied to the capacitors. However, here, we have to remind that the ZnO layer is almost fully depleted at the depletion region. Eventually, the C_{min}/C_{max} ratio of the ZnO capacitor is much larger than that of the Si capacitor, which is pointing up at the unsaturating behavior of the *C-V* curves in Fig. 2a. We easily found that there was not such a big difference between ZnO and Si capacitors in their behaviors at the accumulation regions when the *C-V* curves were plotted on the same scale in *y*-axis. Therefore, we made a conclusion that the behavior observed at the accumulation region is not a critical issue in comparing the *C-V* characteristics and discussing the differences among the samples.

In these discussions, the normalized capacitance was employed, although actual values of measured capacitance also contain important information. Especially, the dielectric constant may be varied with the changes in ALD deposition conditions for the PL and GI layers. However, considering that the overall dielectric constant of the GI is determined by total contribution of the PL, GI, and a plausible interfacial layer between the PL and ZnO, it is very complicated to estimate the accurate values of dielectric constant and their variations for each combination of PL and GI with only the *C-V* measurement data. They should be investigated by varying the film thickness of Al_2O_3 layers prepared with various deposition conditions, which would be another theme for the atomic-layer-deposited Al_2O_3 thin films for future works. Therefore, the concept of normalized capacitance was suitable to easily understand and compare the *C-V* characteristics for the samples.

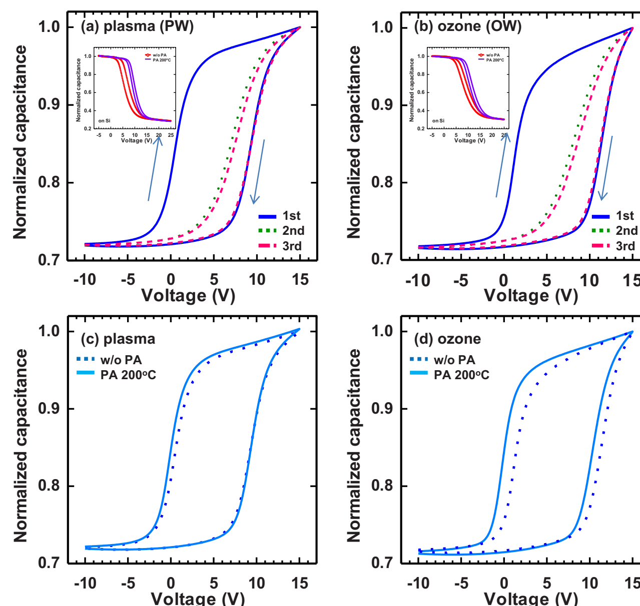

Figure 3. (Color online) Normalized *C-V* characteristics of MIS capacitors when the PL Al_2O_3 layer was prepared by (a) O_2 plasma (device termed as PW) or (b) ozone (device termed as OW). The GI layers for two capacitors were deposited by water. The measurements were repeated three times at the frequency of 1 MHz. The characteristics of the Si capacitors fabricated with the same conditions were also compared in the insets of Fig. 3a and b. The normalized *C-V* characteristics of the (c) PW and (d) OW capacitors were compared between before (dotted lines) and after (solid lines) the postannealing process at 200°C.

Next, the effects of the deposition conditions for PL on the electrical behaviors of the MIS capacitors were investigated with two controlled devices termed as PW and OW, in which the PL of Al_2O_3 in the PW and OW were prepared using in situ generated O_2 plasma and ozone as oxygen sources, respectively. The GI layers for the two controlled devices were deposited by water. Figure 3a and b shows the *C-V* characteristics of the PW and OW MIS capacitors, where the measurements were repeated three times at the frequency of 1 MHz. The first noticeable thing is that both the PW and OW capacitors showed large hystereses in the *C-V* curves. When the voltage was swept from -10 to 15 V and reversed to -10 V, the voltage hystereses of the PW and OW capacitors at the first sweep were measured to be approximately 8.7 and 9.8 V, respectively. The hysteresis width decreased with the evolution of successive measurements, especially at the second sweep. Because the directions of these hystereses were clockwise, the dominant effect of mobile ionic charges could be ruled out. From these results, we can suppose that the observed large hysteretic behaviors in the two capacitors are ascribed to the charge trapping/detrapping processes at or near the interface between the PL and ZnO layers. The possible scenario can be supposed as follows: At the first voltage sweep from -10 to 15 V, the negative charges (electrons) are continuously trapped into the interface trap sites and the resultant V_{FB} values of the capacitors are largely shifted to the positive direction. Once most of the trap sites were occupied, the hysteresis width is reduced at the next sweeps. This irreversibility of the hysteretic behavior is related to the fact that the emission time of the captured charges from the traps is substantially longer than the capture time. The charged traps behave as the fixed charges and cannot be discharged unless a sufficient voltage with opposite polarity is applied. Actually, the hysteresis widths were measured to be the same as initial values with the lapse

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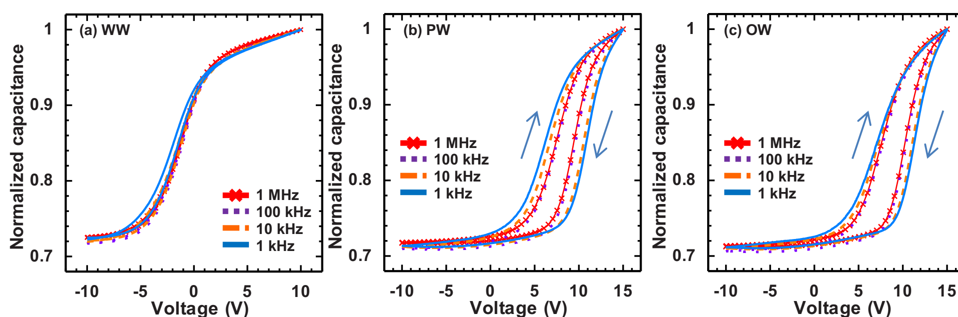

Figure 4. (Color online) Normalized *C-V* characteristics of the (a) WW, (b) PW, and (c) OW MIS capacitors when the measurement frequency was changed to 1 MHz, 100, 10, and 1 kHz.

of sufficient duration, as if the samples were virgins. The density of induced charges by hysteresis (Q_{hys}) can be estimated by $Q_{hys} = C_{ox}\Delta V_{hys}$, where C_{ox} is the capacitance per unit area of the total Al_2O_3 layers and ΔV_{hys} is the voltage width of hysteresis. The Q_{hys} values for the PW and OW capacitors were calculated to be 1.9×10^{-6} and 2.2×10^{-6} C/cm^2, respectively.

We suspect that the origin of traps at the interface between the PL and ZnO layers for the PW capacitor would be some kind of damages induced by plasma. The similar situation was observed in the Si capacitor using O_2 plasma-derived PL, as shown in the inset of Fig. 3a, in which the *C-V* curves were stretched out owing to the increase in D_{it} when compared to the capacitor using water-based PL, as shown in Fig. 2b. As can be seen in Fig. 3c, the heat-treatment at the temperature of 200°C could not drastically change the situation, unlike the case using the water-derived PL (Fig. 2a). Considering that in the Si capacitor using O_2 plasma-derived PL the slope of *C-V* curves and hysteresis width were improved after the postannealing at 200°C as shown in the inset of Fig. 3a, 200°C seemed to be insufficient to release the plasma-induced damages for the ZnO capacitor.

Al_2O_3 deposited by ALD using ozone incorporated less hydroxyl groups (OH) compared to that grown using water at a higher temperature than 300°C.[37] However, an incomplete reaction between the TMA and the ozone at a low growth temperature of 200°C, which was employed for the PL of Al_2O_3 in this study, can likely induce the formation of OH radicals bounded to Al_2O_3. Eventually, these OH radicals exist as kinds of dangling bonds at the interface and behave as interface states. The electrons that piled up near the conduction band at the accumulation region of the capacitor are easily trapped to OH, and the negatively charged OH^- values shift the V_{FB} to the positive direction. As for the Si capacitor using the O_3-derived PL, similar properties were also observed, as shown in the inset of Fig. 3b. The increase in deposition temperature can be a solution to reduce the unexpected formation of OH at the interface of the OW capacitor. Although the heat-treatment performed at 200°C made it better to some extent, as shown in Fig. 3d, the effect may not be sufficient. However, further increase in the annealing temperature higher than 200°C changes the ZnO to have a very conductive nature. Thus, more excessive temperature rise during the postannealing process can be a harsh condition to the TFT applications.

We investigated frequency dependent *C-V* characteristics for the ZnO capacitors with PLs prepared by water, O_2 plasma, and ozone, as shown in Fig. 4a-c, respectively. These measurements were performed at four different frequencies in the forward (−10 to 15 V) and reverse (15 to −10 V) directions after the termination of three successive sweeps in the same voltage range at 1 MHz. Although some studies have been reported for the In–Ga–Zn–O TFTs to estimate the trap densities,[38,39] the exact nature of the frequency dependency (FD) for the oxide-semiconductor-based MIS structures still has not been sufficiently understood. For the capacitor using water-derived PL, the FD in the full voltage range were negligible, even though the appearance of a weak voltage hysteresis in the depletion region was observed at a lower frequency of 1 kHz (Fig. 4a). However, for the PW and OW capacitors, the hysteresis widths increase as the frequency decrease. These kinds of FD most probably arise from a different emission time of the charges trapped in shallow or deep states during the precedent voltage sweeps. As mentioned above, a large number of interface trap states were generated when the PL was deposited on ZnO with O_2 plasma or ozone. The trapped electrons at the shallow states respond to the applied voltage even at high frequencies because the charge emission from these states has a relatively small time constant. Meanwhile the deep states having relatively long time constants are localized as fixed charges and only respond at sufficiently low frequencies. The fact that the PW and OW capacitors did not show the marked FD in the accumulation region suggests that the PL prepared by O_2 plasma or ozone did not induce considerable amounts of mobile charges in the total GI layers. If the induced mobile charges act as a dominant origin of hysteresis, the direction of hysteresis would be counterclockwise and the remarkable FD in the accumulation would be observed because the heavy mobile charges cannot respond to the higher frequencies. Thus, the water-derived PL of Al_2O_3 is most suitable for the ZnO-based TFT application compared with those by other preparation conditions of O_2 plasma and ozone.

This time, we investigated the effect of deposition condition for the GI layers on the electrical behaviors of ZnO capacitors with PL prepared by water, which was considered as the best condition for the PL. The *C-V* characteristics were examined for the MIS capacitors with GI layers deposited by O_2 plasma (the sample termed as WP) or ozone (the sample termed as WO) as an oxygen precursor, as shown in Fig. 5a and c, respectively. Similarly, the MIS capacitors fabricated using p-Si with the same conditions (WP and WO) were also prepared for comparison, as shown in Fig. 5b and d, respectively. The first feature of both the WP and WO capacitors was that there were no remarkable hystereses during voltage sweeps, which were completely different from the cases when the PL was prepared by O_2 plasma or ozone. Consequently, once the PL was prepared on ZnO by water, we can effectively eliminate undesirable trap sites at the interface irrespective of the deposition conditions for GI layers. For the WP and WO capacitors using ZnO, the *C-V* characteristics could be completely recovered in terms of V_{FB} by performing the postannealing process at 200°C for 1 h, which was identical to that observed in the WW capacitor (Fig. 2a). When the properties between the WP and WO capacitors using ZnO were compared, there were no marked differences except that the V_{FB} of the WP capacitor without postannealing showed more quantity of negative shift. The effect of the GI deposition condition can be emphasized when the p-Si was used as an active layer, considering that the interface between the Al_2O_3 and the Si is more sensitively behaved. While the voltage hysteresis and *C-V* slopes for the WP capacitors using p-Si were not fully restored even after the postannealing (Fig. 5b), the *C-V* behaviors of the WO capacitors showed excellent properties comparable to that of the WW capacitors using p-Si (Fig. 5d and 2b). It suggests that the GI layers deposited by O_2 plasma might cause more or less damage on the semiconducting layer. The preparation conditions for the PL played a very critical role in determining the electrical behaviors of the MIS systems of total structures of GI-Al_2O_3/PL–Al_2O_3/ZnO.

As for the positive role of water vapor, the wet O_2 annealing was

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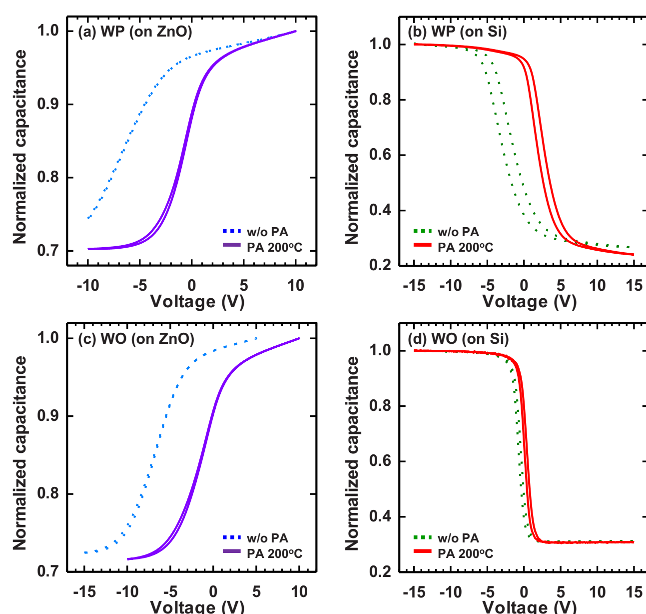

Figure 5. (Color online) Normalized *C-V* characteristics of MIS capacitors using (a) ZnO and (b) p-Si when the GI Al_2O_3 layer was prepared by O_2 plasma (devices termed as WP). Normalized *C-V* characteristics of MIS capacitors using (c) ZnO and (d) p-Si when the GI Al_2O_3 layer was prepared by ozone (devices termed as WO).The PLs for four capacitors were prepared by water vapor. All measurements were performed at the frequency of 1 MHz. The dotted and solid lines correspond to the behaviors before and after the postannealing process at 200°C.

very effective to suppress the formation of oxygen vacancy, and hence, the device performance was dramatically improved.[40] The methodology proposed in this work is rather different, in which water vapor can induce n-type carriers on the surface of ZnO during the deposition of PL, as discussed in Table I. The formation of an excellent interface between the GI and ZnO without any marked damage is also a very important role of the water-derived PL.

The exact estimation of interface trap densities for the MIS capacitors using an oxide semiconducting layer is very difficult and sometimes tricky. Generally, the high frequency *C-V* measurement or the Terman method[36] is the simplest way for estimating the D_{it} at the insulator/semiconductor interface. However, these methods cannot be applied well for the wide bandgap semiconductors, such as GaN, and may cause the underestimation of D_{it} at room

Table I. Comparisons of the extracted parameters of C_{min}/C_{max} and the depletion width (W_d) for the ZnO MIS capacitors fabricated by varying the deposition conditions of PL and GI layers of Al_2O_3. The first and second characters appeared in the samples' notation mean the deposition conditions of PL and GI layers, respectively, in which W, P, and O represent water, O_2 plasma, and ozone, respectively. All capacitors experienced the postannealing process at 200°C.

Sample	C_{min}/C_{max}	W_d (nm)
WW	0.725	14.7
WP	0.703	16.4
WO	0.710	15.8
PW	0.718	15.2
PP	0.680	18.3
PO	0.686	17.8
OW	0.712	15.6
OP	0.674	18.7
OO	0.695	17.0

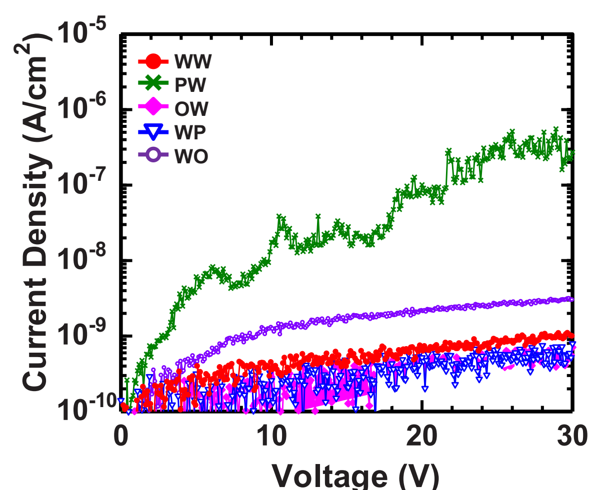

Figure 6. (Color online) Variation in current density as a function of applied voltage from 0 to 30 V for MIS capacitors using ZnO (WW, PW, OW, WP, and WO).

temperature[29] because of the awfully slow generation rate of minority carrier for the wide bandgap semiconductors. For example, in GaN, electrons initially captured in the deep-level states cannot be easily emitted to the conduction band at room temperature because the time constant of emission exponentially increases with the increase in bandgap energy.[41] Eventually, in the *C-V* characteristics of the MIS structures using wide bandgap semiconductors, the deep depletion feature without inversion is typically observed owing to the extremely slow generation rate of the minority carriers.[42,43] For these reasons, the room-temperature photoassisted *C-V* technique was also proposed[43] and exploited in the wide bandgap semiconductors[29,41] as another method to estimate the total number of D_{it} across the bandgap. Similar situations can be supposed for the oxide semiconductor with wide bandgap. However, it seems that the photoassisted technique is difficult to be applied for the MIS capacitors adopting ZnO in principle because the deep depletion behavior does not appear due to the full depletion of thin oxide-semiconducting layer with a few tens of nanometers.

In this study, the availability of the conductance method[44] in estimating the D_{it} for the MIS systems was also investigated. In this method, the equivalent parallel conductance (G_p) is measured as a function of frequency at a given gate bias, where the peak of G_p is generally observed because of the ac loss owing to the capture and emission of carriers by the interface states. The D_{it} can be extracted from the relationship between the value of G_p/ω and the time constants of the interface state. However, the obtained results (not shown here) include some problem in estimating the accurate D_{it} because they are easily affected by the total series resistance caused by the thin film of ZnO layer and ITO electrode. Eventually, we found that the calculated D_{it} values and their trends between the samples could not clearly reflect the observations described and discussed in Fig. 2-4. These results gave us an important sign that it would be very difficult to exactly evaluate the insulator/oxide–semiconductor interface and to quantitatively investigate the D_{it}. This issue is one of the most demanding works to understand the related physics for future works.

The *J-V* characteristics of each ZnO MIS capacitor were also examined, as shown in Fig. 6. From these measurements, we can estimate the leakage currents in the accumulation region of the MIS capacitors, which correspond to the gate leakage components during the TFT operations. As can be seen in figures, while the current density of the WW, OW, WP, and WO capacitors at the voltage of 30 V were as low as 10^{-9} A/cm^2, that of the PW showed much larger values by 2 orders of magnitude. Although the actual operating voltage region for the TFTs was limited to below 10 V, the leakage

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currents of the PW capacitor was much larger than those of other capacitors. These results indicate that the plasma-assisted deposition condition for the PL caused some damage on the interface or the PL of Al_2O_3 itself and increased the leakage components of the MIS capacitor. However, the leakage currents were effectively suppressed when the GI layer was deposited by the same condition using O_2 plasma on the PL prepared by water. For the ozone processes (OW and WO), there was not any marked increase in leakage current. Therefore, the oxygen-related dangling bonds, which were designated as the origin for the large hysteresis observed in the *C-V* curves for the OW capacitor, did not act as kinds of bad pills in the viewpoint of leakage currents. The proposed device (WW) using water for both PL and GI layers showed sufficiently good behaviors of leakage currents.

The reliability issue is also one of the most important factors in evaluating the MIS systems. Although the reliability-related measurements were not performed for the MIS capacitor systems in a detailed way, we carried out the evaluations on device stabilities for the fabricated ZnO TFTs with various GI/PL combinations (not shown here). As a result, it was confirmed that the WW device experienced no degradation from the initial behaviors even after the continuous gate bias stress of 1.7 MV/cm during 51,010 s. The detailed discussions on the bias stabilities of each sample and their comparisons will appear in our next publication.

Finally, it is interesting to compare some parameters of the ZnO MIS capacitors fabricated by varying the deposition conditions of the PL and GI layers of Al_2O_3, in which all capacitors experienced the postannealing process at 200°C for 1 h in an N_2 ambient. Table I summarizes the C_{min}/C_{max} ratio and the W_d for all capacitors, in which the first and second characters of the samples' symbol mean the deposition conditions for PL and GI layers, respectively. The W_d values were calculated using the simple equation of $W_d = (C_{min}/C_{max} - 1)t_{ox}(\epsilon_s/\epsilon_o x)$, where ϵ_s and ϵ_{ox} are the dielectric constants of Al_2O_3 (7.23) and ZnO (9.67),[45] t_{ox} is the total thickness of Al_2O_3, which was calculated from the accumulation capacitance in *C-V* characteristics. We could find a trend that the ratios of C_{min}/C_{max} were varied in an interesting order. When we changed the deposition conditions for the PL and GI layers from water to ozone and from ozone to plasma, the C_{min}/C_{max} values monotonically decreased. Consequently, while the ratio of C_{min}/C_{max} had the maximum of 0.725 for the WW, it had the minimum of 0.680 for the PP. The values of the C_{min}/C_{max} in *C-V* characteristics quantitatively reflect the carrier concentration of the semiconducting ZnO layer. When we use water vapor as an oxygen source for the deposition of Al_2O_3, it would be most probable that more n-type carriers can be induced on the surface of ZnO, compared when O_2 plasma is employed for the process. It should be carefully performed to deal with the absolute values of C_{min}/C_{max} because this is the situation where the ZnO layers are almost fully depleted, which can be also evidently found from the calculated values of W_d. Notwithstanding, these trends suggest that we can also control the electronic properties such as the carrier concentration of ZnO only varying the deposition conditions for the PL and GI layers of Al_2O_3. More detailed works concerning the actual device fabrication and related analysis are planned and will be carried out for future works.

Conclusion

Electrical characterization of MIS capacitors with $Al/Al_2O_3/ZnO$ structures was carried out by the *C-V* technique to investigate the effects of deposition conditions of ALD for the double-layered Al_2O_3 films. The ALD conditions for PL had a very critical impact on the interfacial properties for the MIS capacitors, although the main GI layer was deposited with the same oxygen precursor. When the GI layers were deposited by water, for the water-derived PL, good electrical behaviors such as no hysteresis and normal V_{FB} were observed especially when the capacitors experienced the postannealing process at 200°C. On the contrary, the Al_2O_3/ZnO interfaces were remarkably degraded for the O_2 plasma- or ozone-derived PL. The observed large hystereses and positive shifts of the V_{FB} indicated that a large quantity of the interface or bulk trap sites were generated at and near the Al_2O_3/ZnO interfaces and that they behaved as fixed or interface charges by capturing the electrons. The changes in oxygen sources for the PL and GI layers could control the electrical natures of ZnO surface, where the n-type carrier concentration of ZnO increased when the oxygen sources during ALD were changed in the order of O_2 plasma, ozone, and water. From these *C-V* analyses, we can conclude that the introduction of Al_2O_3 PL and its optimization in preparation condition can provide a useful insight for understanding the electrical behaviors of ALD-grown Al_2O_3/ZnO structures and realizing the high performance ZnO TFTs.

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