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Fully Transparent Non-volatile Memory Thin-Film Transistors Using an Organic Ferroelectric and Oxide Semiconductor Below 200 °C

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A fully transparent non-volatile memory thin-film transistor (T-MTFT) is demonstrated. The gate stack is composed of organic ferroelectric poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] and oxide semiconducting Al-Zn-Sn-O (AZTO) layers, in which thin Al_2O_3 is introduced between two layers. All the fabrication processes are performed below 200 °C on the glass substrate. The transmittance of the fabricated device was more than 90% at the wavelength of 550 nm. The memory window obtained in the T-MTFT was 7.5 V with a gate voltage sweep of −10 to 10 V, and it was still 1.8 V even with a lower voltage sweep of −6 to 6 V. The field-effect mobility, subthreshold swing, on/off ratio, and gate leakage currents were obtained to be 32.2 $cm^2 V^{-1} s^{-1}$, 0.45 V $decade^{-1}$, 10^8, and 10^{-13} A, respectively. All these characteristics correspond to the best performances among all types of non-volatile memory transistors reported so far, although the programming speed and retention time should be more improved.

1. Introduction

The new paradigm of 'transparent electronics' has attracted much interest as a novel technical solution in the field of the next-generation consumer electronics. A transparent display based on organic light emitting diodes (OLEDs) and an oxide semiconductor thin-film transistor (TFT) backplane is one of the most promising candidates.[1–4] The ultimate goal of this 'see-through' device is to realize an integrated system equipped with the ubiquitous functions of information storage, image display, and networking, which strongly demands an embeddable transparent non-volatile memory. Some types of non-volatile memories that feature transparency in the visible range have been reported.[5–9] The typical charge-trap devices using an oxide semiconductor such as In-Ga-Zn-O (IGZO) showed non-volatile memory behaviors, in which a thin charge-trap layer or nanoparticles were embedded within the gate stack. They, however, require a complicated fabrication process to prepare the charge-trap sites and strict operational conditions such as a high and long programming voltage to control the quantity of trapped charges. In order to provide a suitable memory device for the transparent integrated systems, the following three technical issues are the first considerations: 1) lower voltage operation, 2) lower temperature process, and 3) easier integration with driving circuit. These are closely related to the features of application systems in transparent electronics which especially requires a lower power and lower cost. If suitable devices satisfying such requirements are not available, we have no reason to insist on embedding the memory elements into the system, because it is better to employ an external-type conventional memory.

Based on these considerations, in this work, we propose a fully transparent non-volatile memory thin-film transistor (T-MTFT) with a hybrid-type gate stack composed of organic ferroelectric and oxide semiconducting layers. We can simply design the device structure and operational scheme for the memory transistors using the ferroelectric behavior of the gate insulator. A typical organic ferroelectric material of poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] has been employed to realize non-volatile memory transistors with organic semiconductors.[10–17] However, small on/off memory margins, poor ambient stability, and the low field effect mobility of organic transistors may be critical drawbacks for practical memory applications. Furthermore, it is very difficult to prepare low-resistive transparent conducting layers with organic semiconducting materials. With this in mind, the employment of a transparent oxide semiconductor as an active channel layer for the T-MTFT can be a good approach for realizing excellent transistor performance such as a higher mobility and a better uniformity. Although only a few studies on the memory transistors with this hybrid-type gate stack have been reported,[18–20] they were not fully transparent devices owing to the use of metal electrodes. This is the first successful demonstration of a completely transparent memory device based on the polymeric ferroelectrics.

In this work, we adopted the following strategies to obtain the transparent memory transistors with excellent performances with

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lower operational voltage at a process temperature below 200 °C: 1) Al-Zn-Sn-O (AZTO) was newly employed as a semiconducting channel layer to lower the overall process temperature to below 200 °C. The AZTO dosen't need an additional heat treatment at high temperature (~300 °C),[21] which is generally performed for ensuring good performances of the TFT. It is also desirable that elements such as Ga and In are not included in the AZTO. These features are very beneficial to realize low-cost and low-temperature transparent electronic devices on flexible substrates in the near future. 2) The first gate insulator of Al_2O_3 was prepared between the AZTO and P(VDF-TrFE) to guarantee the interfacial quality and protect the AZTO during the process. It is also very effective for maintaining the nature of the AZTO surface during the coating and etching processes of P(VDF-TrFE). The chemical solvent of P(VDF-TrFE) and O_2 plasma used for the etching might critically degrade the electrical properties of the AZTO. The fabricated memory device showed an excellent transmittance in the visible range and good electrical characteristics even at an operational voltage as low as 10 V. The proposed device structure is also very desirable to integrate with driving or accessing transistors for memory arrays, because the oxide TFTs using the same structure except for the main gate insulator can also be utilized for the driving devices.

2. Results and Discussion

Figures 1a and 1b show a schematic cross-sectional diagram and a photograph of the proposed T-MTFT, respectively. The gate stack structure was ITO (150 nm)/P(VDF-TrFE) (80 nm)/Al_2O_3 (6 nm)/AZTO (12 nm)/glass. The fabricated device was fully transparent and the logo of ETRI under the substrate was quite clear. Our T-MTFT exhibited a high transmittance of approximately 90% (averaged in different three points in the substrate) at a wavelength of 550 nm, as shown in Figure 1c. This was almost the same as that measured in a bare glass substrate.

Figure 2a shows the drain current–gate voltage (I_D–V_G) transfer curves and the gate leakage currents (I_G) for the fabricated T-MTFT, which were measured in a double sweep mode at two drain voltages (V_Ds) of 0.1 and 1.0 V. The gate width (W) and length (L) of the measured device were 20 and 10 μm, respectively. A counterclockwise direction of the transfer curves was clearly observed. These shifts in turn-on voltage of the TFT (V_{on}), which was defined as the voltage when the I_D was launched from the off-state, originated from the ferroelectric nature of P(VDF-TrFE). The memory window (quantity of shift in V_{on}) was obtained to be approximately 7.5 V with the V_G sweep from −10 to 10 V at a V_D of 1.0 V. In the viewpoint of the transistor, excellent electrical properties were also successfully confirmed. A field effect mobility (μ_{lin}) can be determined by applying the simplified equation below over the low drain voltage region ($V_D < 1.0$ V), which belongs to the linear regime in the I_D–V_G transfer characteristics.

$$\mu_{lin} = \frac{Lg_m}{WC_{ox}V_D} \quad (1)$$

C_{ox} and g_m correspond to the gate oxide capacitance per unit area and transconductance of the TFT, respectively. The obtained μ_{lin} was approximately 32.2 cm^2 V^{-1} s^{-1}, which is the best value among those of the previously reported memory transistors using P(VDF-TrFE). Other important parameters of subthreshold swing (SS), the ratio of on/off drain current, and the gate leakage current were obtained to be 0.45 V $decade^{-1}$, 1×10^8, and 10^{-13} A, respectively. These characteristics showed that our T-MTFT has excellent performances that have not been reported so far, and

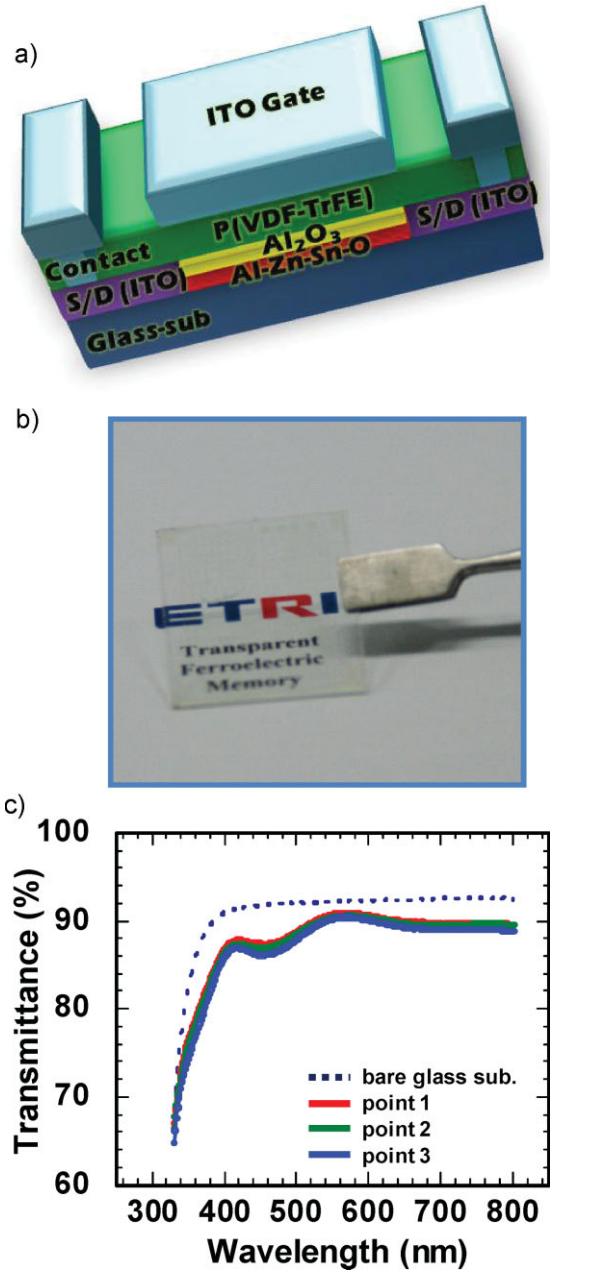

Figure 1. a) Schematic cross-sectional diagram and b) photograph of the proposed transparent non-volatile memory thin-film transistor. The size of the glass substrate was 2×2 cm^2. c) Transmittance of the T-MTFT fabricated on the glass substrate in the visible range. Three different points in the substrate were measured for accurate evaluation. Transmittance of bare glass was also plotted in dotted line.

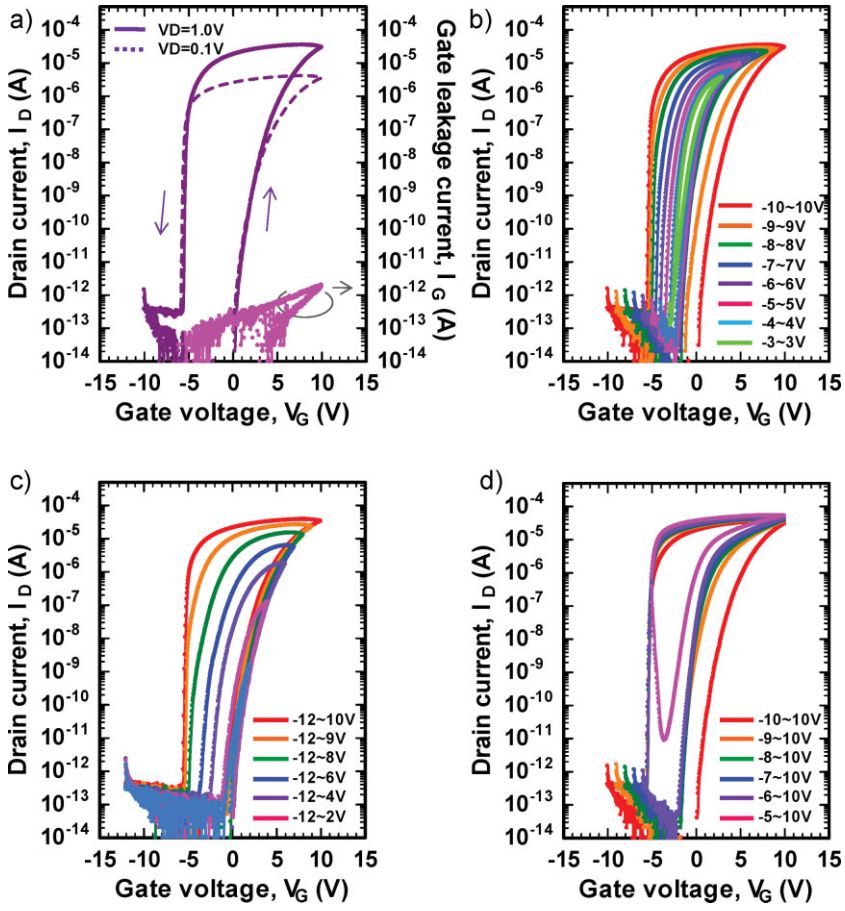

Figure 2. a) I_D–V_G transfer curves and gate leakage currents of the fabricated T-MTFT with the gate width of 20 μm and length of 10 μm. Indicated arrows describe the direction of transfer curves in a double sweep of V_G from −10 to 10 V at two V_D's of 0.1 and 1.0 V. b) Sets of transfer curves when the V_G sweep ranges symmetrically increased from −3 to 3 V to −10 to 10 V. The V_D at each measurement was 1.0 V. c) Transfer curve variations when only the positive side in the V_G sweep range increased from 2 to 10 V with maintaining the negative side as −12 V. d) Transfer curve variations when only the negative side in the V_G sweep range decreased from −10 to −5 V with maintaining the positive side to be 10 V. All the measurements were carried out in a dark box and at room temperature.

they are concluded to result from the suitable choice and combination of materials composing the gate stack. Figure 2b shows the variation in memory window at the various sweep range of V_G. The width of the memory window gradually increased from 0.6 to 7.5 V when the sweep range increased from −3 to 3 V to −10 to 10 V. Even when the V_G sweep was −6 to 6 V, the memory window was confirmed to be as wide as approximately 1.8 V. This suggests that the proposed T-MTFT can be operated with a sufficiently lower voltage. It is also noticeable that the memory window width increased in almost a symmetrical way toward both directions, which indicates that undesirable charge trapping at the interfaces of P(VDF-TrFE)/Al_2O_3 and Al_2O_3/AZTO were negligible during the ferroelectric-based memory operations. Figure 2c shows the variations of the transfer curves when the sweep range of V_G increased only to the positive side at a fixed −12 V in the negative side. In this series of measurements, the memory windows were observed to increase toward only the negative direction while maintaining the same V_{on}, which resulted from the fact that the off operations were ensured at each measurement by a sufficient negative voltage to program the off-state. Consequently, we can control and design the operation voltage and corresponding memory behaviors by using the operation schemes shown in Figure 2c. On the contrary, the different situations were expected when the sweep range of V_G increased only to the negative side at a fixed 10 V in the positive side. Although this series of measurements ensured the on operation, the off operation could not be carried out with an insufficient negative voltage for programming the off current, as shown in Figure 2d. We can estimate the programming voltages for the on and off operations by a load-line analysis,[20] in which the slopes of the calculated load-line have different values between positive and negative voltage regions. This is related to the fact that the fully depleted layer formed in the active channel is likely to be involved in the off programming operation. Because the employed thickness of the oxide semiconducting channel layer is so thin that the channel is fully depleted, it remains as an insulating layer at the off state in the negative V_G region. Therefore, a voltage must be applied with more than the given minimum amplitude in order to fully reverse the ferroelectric polarization set by the previous sweep. This is the reason why the I_D did not start from the off current level at the sweep into the forward direction and did not approach the initial value of the off state when the V_G was swept in the range of −5 to 10 V (Fig. 2d). The ferroelectric polarization set at the application of 10 V in V_G could not be fully reversed to the opposite direction with the application of only −5 V and the off operation could not be conducted. Furthermore, it is interesting to note that, for the off operation, a larger voltage is necessary than in the case of the on operation, as expected from the load-line analysis. Therefore, the employment of a thinner active layer would be desirable to reduce the off voltage level, because a steeper slope of the load-line can be expected. On the other hand, another situation can be considered when the V_G was swept in the range around or under the coercive field of the ferroelectric layer. At this condition, the polarization behaves on the minor loops, in which the P(VDF-TrFE) layer has some kind of partially switching polarization. Because, at this minor loop condition, only a small quantity of polarization remained and its interaction is unstable, thus a smaller voltage will be sufficient to switch the polarization to the opposite direction. The sweep of V_G to 5 V corresponds to this minor loop condition. Consequently, with only the reverse sweep of V_G to −5 V, we can confirm the complete off operation (Fig. 2b). Even though we can obtain a meaningful width in the memory window at the minor-loop

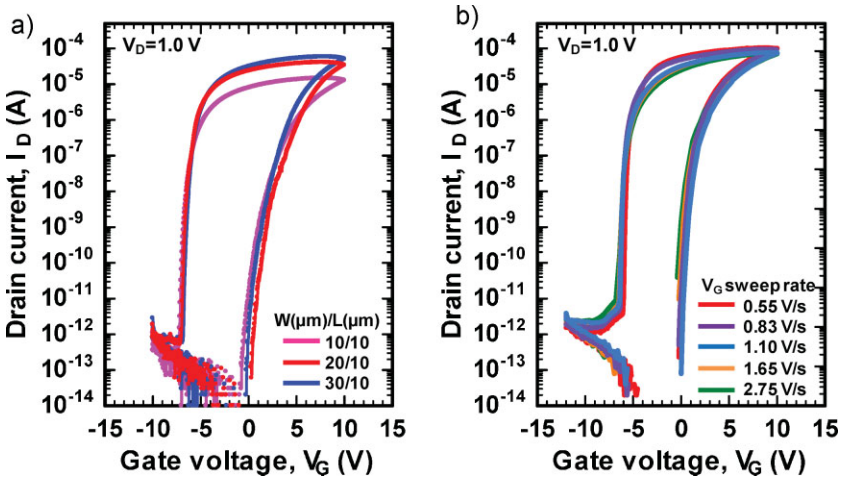

Figure 3. a) Sets of transfer curves of the fabricated T-MTFTs with various channel widths, in which W was changed to 10, 20, and 30 μm at a fixed L of 10 μm. The measurements were carried out in a dark box and at room temperature. b) Variations of transfer characteristics of T-MTFT ($W/L = 30/10$ μm) when the sweep rate of V_G was changed from 0.55 to 2.75 V s^{-1}. All curves were obtained at a V_D of 1.0 V.

conditions, it is more desirable to employ the fully saturated hysteresis curve to guarantee the memory retention behaviors of the T-MTFT.

Figure 3a shows sets of transfer curves when the channel width of T-MTFT is varied from 30 to 10 μm with a fixed L of 10 μm. The scaling in I_D was normally obtained with constant V_{on}s and memory windows of each device. We can confirm that the proposed device structure and fabrication procedures for our T-MTFT were sufficiently compatible for device scaling to the gate size of $10 \times 10\ \mu m^2$. Figure 3b shows the variation of transfer characteristics when the V_G was swept at various sweep rates from 0.55 to 2.75 V s^{-1}. There was no marked change in the memory window within the evaluated range of sweep rates. This result evidently indicates that the obtained memory window of our T-MTFT was dominantly a result of the ferroelectric field effect. If there exists a significant quantity of mobile charges drifting across the P(VDF-TrFE) gate insulator, the width of the apparent memory window would experience a large variation with the change of the V_G sweep rate. Another discussion point from this result is whether the change of sweep rate in V_G is related to the switching kinetics in the ferroelectric polarization or not. It is generally known that the switching time of polymeric ferroelectrics such as P(VDF-TrFE) is observed to be relatively slow and the polarization reversal is sensitively affected by the programming time. However, the applied time for one-cycle of a voltage sweep from −10 to 10 V is totally different from the cases of the programming operation using pulsed signals, which will be discussed in Figure 4. The sweep rate (around 0.3 V s^{-1}) generally employed for the measurements of direct current (dc) transfer characteristics is expected to have no marked impact on the kinetics of the polarization reversal. Therefore, even though the sweep rate was accelerated to be ten times faster (approximately 2.5 V s^{-1}), we don't have any problem in exploiting the ferroelectric nature.

In developing the integrated system embedded with the transparent memory, the investigation of the light effect on the memory and transistor behaviors is also important.[22,23] We have observed that the SS was somewhat degraded and V_{on} was shifted to the negative direction when the transfer characteristics were measured upon opening the dark box. However, the memory behaviors were confirmed to be not so degraded. More detailed investigations on the light effect will be performed in a systematic way in future work.

In order to examine the memory effect, drain current–drain voltage (I_D–V_D) output characteristics were measured for our T-MTFT, as shown in Figure 4a. First, V_G was swept in the range of 0 to 12 V or 0 to −12 V. The read-out voltage of −1.0 V was then applied to the gate terminal and the output curves were plotted. As shown in Figure 4a, the I_D changed from an off to on state by changing the previous V_G sweeps of from 0 to −12 to 0 to 12 V even at the same read-out V_G. In practical memory operations, it is also important to investigate the memory behaviors when the pulse signals with given duration are applied for programming actions, which is directly related to the memory switching speed and available on/off margin for corresponding operation speed. Figure 4b shows the initial programming current values in I_D and their variation with time evolution during the first 20 s when the width of the programming pulse signals were varied to 990, 500, and 200 ms. The pulse amplitudes for on and off were fixed at 10 and −10 V, respectively. The on/off memory margin was observed to markedly decrease with the decrease of programming pulse width. As shown in Figure 4c, which summarizes the obtained I_Ds at both memory states and corresponding on/off margins at each pulse width condition, the on/off current ratio drastically decreased from 1100 to 2.5 as the pulse width decreased from 990 to 200 ms. Therefore, it was found that a programming pulse width of more than 500 ms will be necessary to obtain a memory margin of higher than 10. This criterion is supposed to be quite slow compared with that reported in P(VDF-TrFE) capacitors.[24] Here, we believe there are two reasons for these results. The first is the strong dependency of the switching speed of the polarization reversal in P(VFD-TrFE) on the applied electric field (E).[25,26] This may be more remarkably observed for the metal–P(VDF-TrFE)–semiconductor structure owing to a higher resistance of the semiconducting layer and generation of a depletion layer in the semiconductor. Because the switching time exponentially decayed with $1/E$, a slight increase of programming voltage can reduce the pulse width to program both states, although we could not apply a voltage higher than 10 V owing to the circumstances of our measurement system. The second is the use of an ITO gate electrode in this work, in which the conventional metal electrode was replaced by the transparent ITO gate electrode to realize the fully transparent MTFT. A relatively high resistance of the gate electrode can delay the pulse propagation during the programming event. An imperfect interface between ITO and P(VDF-TrFE) might be an additional resistance component. This problem can be improved by optimizing the process conditions in future work. Although there remain some problems in programming with shorter pulse signals, the obtained results for our T-MTFT are quite encouraging.

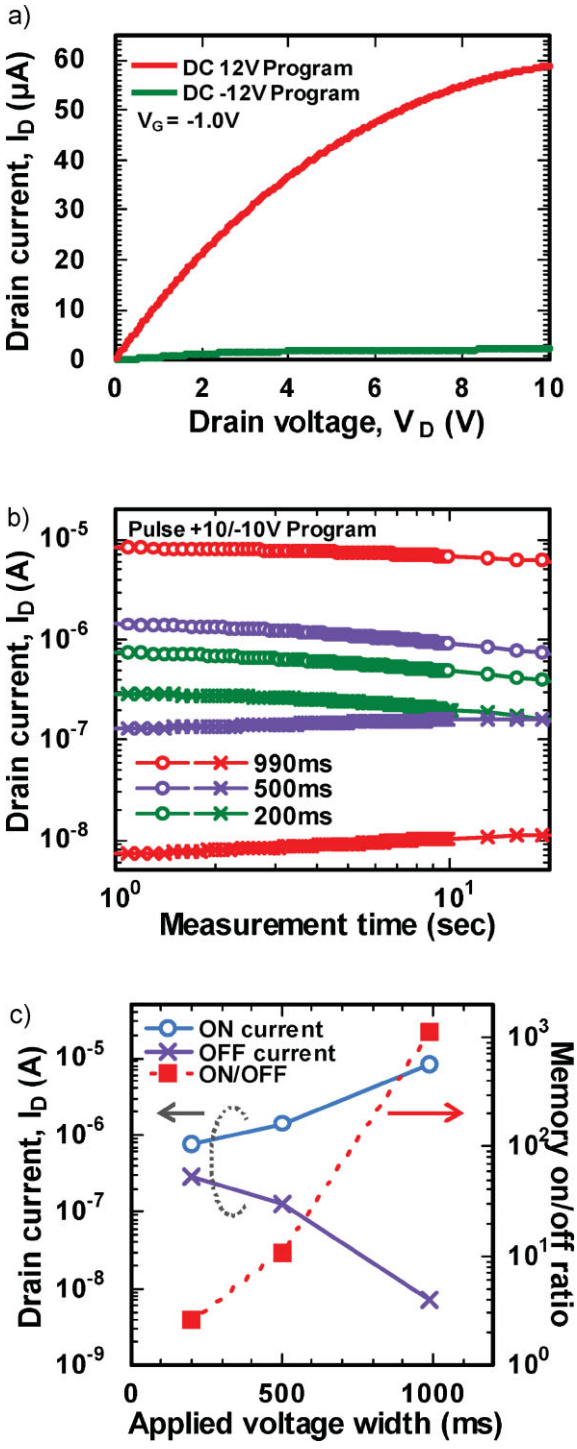

Figure 4. a) I_D–V_D output characteristics after the V_G sweeps of 0–12 V (red) and 0 to −12 V (green). For two measurements, the same V_G of −1.0 V was applied. b) Variations of the programmed I_Ds with time evolution for 20 s when the pulse width of programming signals were changed to 990, 500, and 200 ms. For the on or off programming, 10 or −10 V with various pulse widths were applied to the gate terminal, respectively, before the measurement of initial values and their changes of programmed drain currents. c) Summary of the initially obtained I_D values for each programming and corresponding on/off ratios when the programming pulse width was changed.

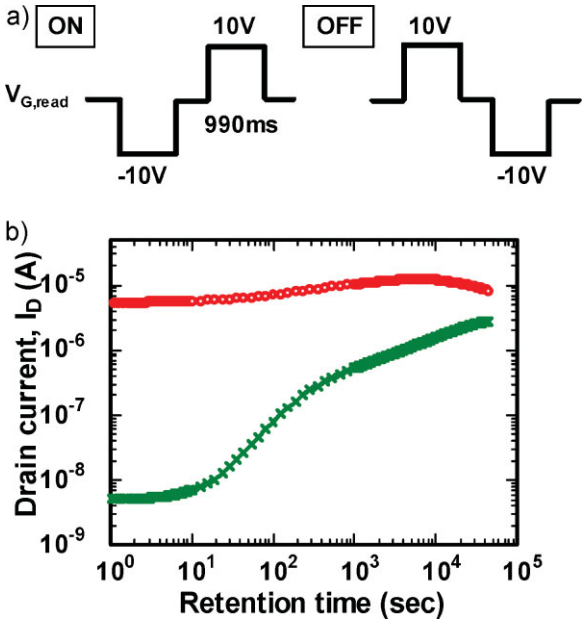

Figure 5. a) Programming pulse sequences for the evaluation of memory retention behaviors of T-MTFT. The first and second pulses of each sequence for on and off operations correspond to initialization and programming pulses, respectively. The pulse width was set to 990 ms. b) Variations in I_Ds programmed into both states with the lapse of memory retention time. During the measurements, the gate terminal was opened and a V_D of 1.0 V was applied.

The memory retention characteristics were investigated. The pulsing sequences are shown in Figure 5a. For programming the on state, the −10 V high and 990 ms wide initial pulse was first applied to the gate terminal to initialize the ferroelectric polarization in the P(VDF-TrFE) layer, then a 10 V high and 990 ms wide programming pulse was applied and I_D was measured at a given read-out V_G. For the case of the off state, the pulse amplitudes were reversely applied. Figure 5b shows the retention behaviors of programmed on and off currents, in which the read-out V_G was set to be an open condition. The initial on/off ratio was obtained to be higher than 10^3 and the ratio of more than 10 remained after the lapse of 1 h, although the off current markedly increased during the period. Because the regime of the memory window for this T-MTFT was formed in the negative voltage region, as shown in Figure 2a, the open condition of V_G might be severe for the off state retention. In general, the retention behaviors of programmed currents for this type of memory transistor are very sensitive to the read-out conditions of V_G. Although the obtained retention time should be more extended, considering the relatively low programming voltage of ±10 V, we can expect a great potential for the future development of our T-MTFT.

3. Conclusions

A fully T-MTFT with the hybrid-type gate stack composed of an ITO/P(VDF-TrFE)/Al_2O_3/AZTO structure has been fabricated. All the fabrication processes were performed below 200 °C on a glass

substrate. The fabricated device showed an excellent transmittance of more than 90% in the visible range (at a wavelength of 550 nm). To ensure good memory and transistor characteristics of our T-MTFT at a low process temperature, two important strategies were proposed, such as the use of AZTO as a semiconducting active channel and the use of a thin Al_2O_3 layer between P(VDF-TrFE) and AZTO. Consequently, the T-MTFT showed a memory window of 7.5 V even at a relatively low operation voltage range from −10 to 10 V, μ_{lin} of 32.2 cm^2 V^{-1} s^{-1}, SS of approximately 0.45 V $decade^{-1}$, an eight orders of magnitude on/off ratio, and a gate leakage current as low as 10^{-13} A. Although the programming speed and retention time should be more improved, it can be concluded that our transparent MTFT will provide novel functionalities and design schemes for the various system applications in future transparent electronics.

4. Experimental

Device Fabrication: The fabrication procedures of a top-gate T-MTFT are as follows. A 150 nm thick ITO glass was used as the transparent substrate. The ITO layer was patterned into the source/drain (S/D) electrodes using wet etchant. A 12 nm thick AZTO semiconductor layer was deposited by means of co-sputtering of an Al_2O_3−ZnO (Al_2O_3 2 wt %) and a SnO_2 target (manufactured by ANP Co.) with a radio frequency magnetron sputtering system. The deposition process was performed in an Ar/O_2 atmosphere at a chamber pressure of 0.2 Pa. A 6 nm thick Al_2O_3 layer was then deposited on the AZTO by an atomic layer deposition (ALD) method using an Al precursor of trimethylaluminium (TMA) and water vapor at 200 °C. After the Al_2O_3 and AZTO were patterned into the shape of the channel by using dilute hydrofluoric (HF) acid solution, a P(VDF-TrFE) layer was formed by means of spin-coating using a 2 wt % dilute solution of P(VDF-TrFE) (70/30 mol %) in *N*,*N*-dimethylformamide (DMF). A solution was spun-on the substrate at a spin rate of 2000 rpm for 10 s and then dried at 70 °C for 5 min on a hot plate. The film thickness of P(VDF-TrFE) was measured to be approximately 80 nm. The film was annealed at 140 °C for 1 h in an ambient air for the crystallization. For forming the holes for the S/D contacts, the given areas of P(VDF-TrFE) were removed by using O_2 plasma with a dry etching system using a helicon plasma source. In this process, the lithography included developing and stripping of photoresists coated on P(VDF-TrFE) layer and were so carefully designed as not to cause undesirable chemical damage to the P(VDF-TrFE) [27]. The transparent ITO gate electrode was deposited with a thickness of 150 nm by using the sputtering system (ULVAC) and annealed at 150 °C for 30 min in ambient air. In general cases, the plasma-induced sputtering process easily causes critical damage to organic films such as P(VDF-TrFE). In this work, the plausible physical damage was minimized by employing an off-axis geometry between the substrate and the target in the sputtering system, in which the substrate does not directly face the sputtering target. The wet etching process of the deposited ITO electrodes on P(VDF-TrFE) was also important owing to poor adhesion between the ITO and P(VDF-TrFE). The fact that the post annealing process for the ITO, which is generally performed to enhance the conductivity of the ITO electrode at around 250 °C, is not available above 150 °C and makes it more difficult to clearly pattern the ITO electrodes on P(VDF-TrFE). In this work, the concentration of hydrochloric acid (HCl)-based wet etchant was so controlled for the etching time to be about 100 s at 50 °C. Any additional heat treatments were not conducted after the device fabrication.

Electrical Characterization: All the electrical characteristics of the fabricated T-MTFT were basically evaluated in a dark box at room temperature using a semiconductor parameter analyzer (Agilent 4156C). The programming operations with pulse signals and retention behaviors were evaluated by using an arbitrary waveform generator (Biomation 2414A), a programmable power supply (Kepco), an electrometer (Keithley 6517A), and PC-interfaced measuring software.

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