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# Stability of a-InGaZnO thin film transistor under pulsed gate bias stress

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ABSTRACT

We investigated the stability of amorphous InGaZnO (a-IGZO) thin film transistor (TFT) under pulsed gate bias stress with light illumination, and compared that with DC bias stress. In the case of DC gate bias stress, a-IGZO TFT showed considerable degradation only when the negative gate voltage was applied under light illumination. For the pulsed gate bias stress, we constructed a voltage square wave with a bi-level of −20 V and 0 V and also made variations in the time duration of −20 V level in a cycle. Although the accumulated time duration of applying −20 V in the pulsed gate bias stress was the same with that of DC −20 V stress, the degradation was much reduced compared with DC bias stress. On the basis of the experimental results, we propose possible degradation mechanisms related with the role of subgap states.

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## 1. Introduction

Amorphous indium gallium zinc oxide (a-IGZO) thin film transistor (TFT) is a promising candidate for a switching element in display applications [1,2]. However, device stability under operation is an important issue for the commercialization of a-IGZO TFT. The electrical bias is one of the main factors which degrade the device performance as time passes, and the illuminant environment also affects the device stability directly or indirectly. There have been a lot of studies on the stabilities of a-IGZO TFTs [3-7]. Many articles commonly reported that well-fabricated a-IGZO TFTs showed stable characteristics under DC bias stress without light illumination, but they showed significant degradation under DC negative gate bias stress with light illumination [5,6]. These results showed that the light induced instability phenomenon arises via two kinds of main mechanisms which can be summarized as the hole trapping effect due to photo-generated hole carriers [7] and the change of the transition level of subgap defects such as oxygen vacancies [6]. However, these studies dealt with DC bias and illumination effects. The switching elements in display devices are subject to pulsed gate bias in order to change their switching state. Therefore it is necessary to investigate the stability of a-IGZO TFT under pulsed bias with light illumination.

In this work, we examined the stability of a-IGZO TFT under DC bias stress with light illumination for the first step, and then the pulsed gate bias stress was performed with light illumination. The degree of degradation depended seriously on the bias types, i.e. DC or pulse. Based on our experimental results, we propose possible mechanisms of light-induced dynamic instability of our a-IGZO TFTs. There have also been several reports related to instabilities under dynamic bias conditions [8-11]. In discussing our results and mechanisms, we will explain the differences in the experimental methodologies and the related mechanisms between our study and other studies.

## 2. Experiments

Fig. 1 shows the cross section view of our a-IGZO TFT fabricated in the top gate structure. We fabricated a-IGZO TFT on a glass substrate by using conventional photo-lithography. A 150 nm thick indium tin oxide (ITO) layer was deposited with r.f. magnetron sputtering and patterned for the source/drain (S/D) electrodes. A 20 nm thick a-IGZO active layer was deposited by using r.f. magnetron sputtering at room temperature. The active layer was patterned by using a wet etching process. A 180 nm thick alumina ($Al_2O_3$) layer was grown by using atomic layer deposition at 150 °C for the gate insulator. To achieve high transparency against top-light illumination, we utilized a transparent ITO layer for the gate electrode. A 150 nm thick ITO gate electrode was deposited by using r.f. magnetron sputtering and patterned with a wet-etching process. Finally the device was annealed at 200 °C in a vacuum chamber to optimize its electrical performance.

Stability tests were carried out in a shielding box to isolate external light. An Agilent 4155 °C semiconductor parameter analyzer with a pulse generating module and a probe positioning system were utilized for electrical measurements and stress tests. The wave length of light utilized for illumination during the stress tests was 430 nm which was achieved from the combination of a Xe lamp and a

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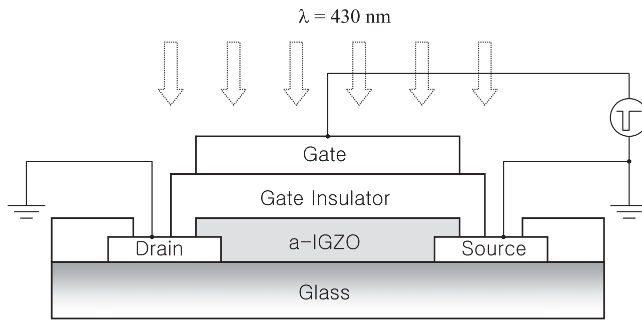


**Fig. 1.** Cross section view of a-IGZO TFT structure used in the study.

monochromator. The power density of the illumination was set to be 0.1 mW/cm$^2$.

## 3. Results and discussions

For the investigation of DC gate bias effect on the device stability, we applied +20 V gate bias and −20 V gate bias, respectively, for 10000 s with 430 nm wavelength light illumination. The S/D electrodes were connected to a ground (0 V) terminal. Fig. 2 (a) shows the evolution of changes in the transfer characteristics of a-IGZO TFT during DC + 20 V gate bias stress with light illumination. There are little changes in device characteristics before and after the stress. Fig. 2 (b) shows the evolution of changes in the transfer characteristics of a-IGZO TFT during DC −20 V gate bias stress with light illumination. In this figure, the significant changes in the transfer characteristics can be observed. The transfer curve was considerably shifted in the negative direction along the $V_{GS}$ axis. Furthermore, the linear slope of the subthreshold region was not maintained and the hump shape appeared in the subthreshold region.

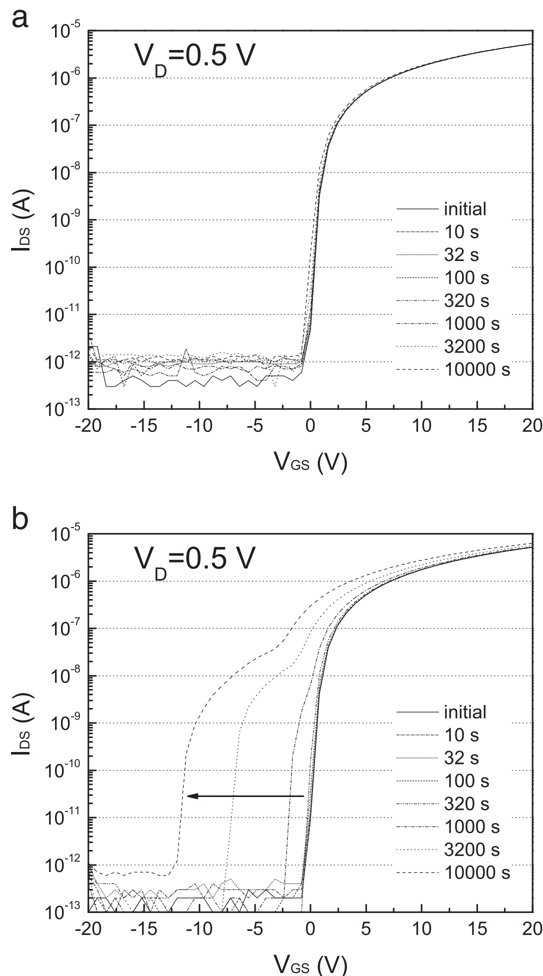


**Fig. 2.** Evolution of changes in the transfer characteristics of a-IGZO TFT during DC gate bias stress with light illumination (a) DC +20 V, (b) DC −20 V.

From the above results, it seems that our a-IGZO TFT suffered at least two different degradation mechanisms under DC −20 V gate bias stress with light illumination. The first mechanism can be regarded as hole trapping in the gate insulator or at the gate insulator/channel interface, which results in the negative shift of the transfer characteristics. The light illumination plays a pronounced role in hole trapping because it generates electron–hole pairs with the help of the subgap states. Because the bandgap of a-IGZO (3.1 eV) is larger than the photon energy of visible light, the direct transition of electrons from the valence band to the conduction band hardly occurs in the presence of illumination. However, if there exist the unfilled subgap states in the bandgap, electrons in the valence band can be excited into those subgap states and holes can be accumulated in the valence band. When holes are trapped in the gate insulator by the negative gate bias, the transfer curve can be shifted in the negative direction.

However, in the presence of illumination, the emission of electrons can occur not only from the valence band but also from the deep donor-like states such as oxygen vacancies [6]. The latter is not related with the hole generation but with theemergence of the positively ionized subgap states. Before the stress test, the transition level of the deep donor-like states are so deep that they always remain in the neutral state regardless of the Fermi level position when the transfer curve is measured. However, if they are changed to the charged state via illumination during the stress, they cannot return to their neutral state because the negative gate bias depletes most of electrons in the conduction band. Furthermore maintaining such a charged state will relocate the surrounding metal atoms slowly as to elevate the transition level of the donor-like states. Consequently, the transition levels elevated near the conduction band edge will trap and detrap electrons according to the Fermi level in measuring the transfer curve after the stress test. Therefore, the transfer curve reveals the hump shape in the subthreshold region after the stress test. This is the illustration of the second degradation mechanism of our a-IGZO TFT.

From the above results, it can be mentioned that the major condition for device degradation is the negative gate bias with light illumination. This is a serious condition for switching devices because the turn-off duration is much longer than the turn-on duration in periodic cycles of the gate pulse. Therefore, we investigated the stability of a-IGZO TFT under the pulsed gate bias stress with light illumination. We focused on the effect of the negative gate bias, so that we constructed a voltage square wave with a bi-level of −20 V and 0 V and also made variations in the time duration of −20 V ($t_{-20}$), fixing the time duration of 0 V ($t_0$) in one cycle. It should be noted that the accumulated time duration of applying −20 V in all thepulsed gate bias stress was kept to be the same with that of DC −20 V stress.

Fig. 3 (a) shows the evolution of changes in the transfer characteristics during the pulsed gate bias stress with light illumination. The time duration of −20 V and 0 V was 100 ms and 10 ms, respectively. In counting the accumulated stress time,only the time duration of − 20 V was counted but the time duration of 0 V was not counted. Interestingly, the degradation was much reduced compared with that under DC −20 V stress. The parallel shift of the transfer curve which is related with hole trapping cannot be observed, and only the slight evolution of the hump-like shape can be observed. When the time duration of −20 V gets longer, only the degree of the hump-like shape increases slightly as shown in Fig. 3 (b).

From the above results, it can be known that the periodic insertion of the short duration of 0 V effectively suppresses the degradation.

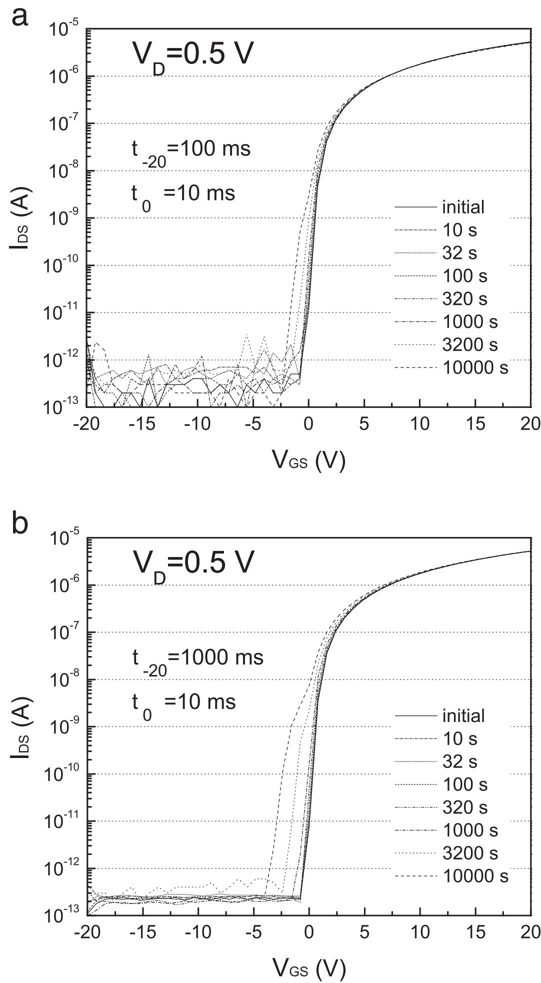


**Fig. 3.** Evolution of changes in the transfer characteristics of a-IGZO TFT during the pulsed gate bias stress with light illumination (a) $t_{-20}$= 100 ms/$t_0$= 10 ms, (b) $t_{-20}$= 1000 ms/$t_0$= 10 ms.

Son et al. reported similar experimental results [8], however, their waveform for the gate pulse was constructed with −20 V and + 10 V. Therefore they concluded that the degradation under the pulsed gate bias stress was reduced because the trapped holes during −20 V duration could be detrapped during +10 V duration. This explanation is suitable for their experiment, however in case of our experiment the positive bias was not utilized for constructing the waveform, so the detrapping mechanism is not a dominant factor in our experiment. Another report also utilized a similar waveform constructed with −15 V and +15 V [9]. Furthermore, the shift direction of the transfer curve in that report was in the positive direction, which seems to be related with poor gate dielectric material. Another two reports also dealt with charge trapping and detrapping under very low frequency waveforms of which the pulse period is longer than 1000 s [10,11]. Their waveforms are much different with ours. In our experiment, the reduced degradation seems to be related with the time duration effect rather than the bias polarity effect. Although the electron-hole pair generation starts to occur under the negative gate bias with light illumination, the negative gate bias should be continuously applied for a certain time duration for a sufficient density of holes to evolve. We call the time duration for hole accumulation as the transient time, which is essential for the emergence of hole trapping. In our waveform, the settled time duration of −20 V, such as 100 ms or 1000 ms, seems to be shorter than the transient time for hole accumulation. In addition, the periodic 0 V bias eliminates a small amount of accumulated holes periodically every pulse cycle.

The reason for the long transient time for hole accumulation is related to the time for the hole quasi-Fermi level to reach the steady state where it approaches near the valence band edge. In order to verify the existence of the transient time for hole accumulation, we investigated the variation of light-induced subthreshold current as time passes. The subthreshold current originates from the density of electrons determined by the electron quasi-Fermi level under light illumination. The transient behavior of the electron quasi-Fermi level is related to that of the hole quasi-Fermi level, so we can deduce indirectly the transient behavior of the hole quasi-Fermi level via investigating the transient subthreshold current. Fig. 4 shows the variation of light-induced subthreshold current at a fixed gate voltage as time passes. The level of the fixed gate voltages was 0 V, −0.8 V, −1.6 V and −2.4 V, respectively. The wavelength of light was 430 nm which was the same for the stress test. All the subthreshold currents in Fig. 4 are not constant but increase with time. This means that the steady state or the final position of the quasi-Fermi level was not obtained up to 20 s which was the time limit for the observation. The above result illustrates that the degradation under the negative gate bias with light illumination is not an immediate process but requires a somewhat long transient time. However, the slight evolution of the hump-like shape which is related to the positively ionized subgap states is possible during the pulsed gate bias stress. This is because electron emission from deep donor-like states is not related to the position of the Fermi level and the life time of those ionized subgap states is generally longer than that of holes. Therefore, some of the ionized subgap states seem to survive during the time duration of 0 V bias. Consequently, although the slight evolution of the hump-like shape occurs, the pulsed gate bias stress is not a serious condition for the device degradation compared with DC gate bias stress.

## 4. Conclusion

In this work, the instabilities of a-IGZO TFT under DC gate bias stress and the pulsed gate bias stress combined with light illumination have been examined. The transfer characteristics of our a-IGZO TFT were seriously degraded when DC negative gate bias stress was applied in the existence of light illumination. However, the pulsed gate bias stress with light illumination only slightly degraded the device. The periodic 0 V bias during the pulsed gate bias stress eliminates hole accumulation which is essential for the emergence of hole trapping. We have verified that the hole accumulation in a-IGZO under the negative gate bias with light illumination is not an immediate process, so that the pulsed gate bias stress is not a serious

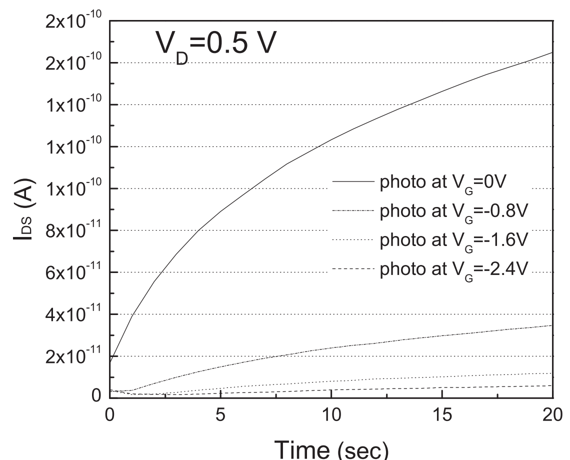


**Fig. 4.** Variations of light-induced subthreshold current at various fixed gate biases with time.

condition for the device degradation compared with DC gate bias stress.

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