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Flexible Nonvolatile Memory Thin-Film Transistor Using Ferroelectric Copolymer Gate Insulator and Oxide Semiconducting Channel

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The flexible nonvolatile memory thin-film transistor (F-MTFT) is demonstrated. The gate stack is composed of ferroelectric poly(vinylidene fluoride-trifluoroethylene) gate insulator and ZnO semiconducting channel. All the processes are performed below 150 °C on a poly(ethylene naphthalate) substrate. The ferroelectric field-effect-driven memory window and the on/off ratio of the fabricated F-MTFT were 7.8 V and 10^8, respectively. These behaviors did not show so marked degradations at bending situations with a curvature radius of 0.97 cm and after repetitive bendings of 20,000 cycles. The programmed on/off ratio was initially 6.6×10^5 and retained to be approximately 130 after a lapse of 15,000 s.
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Flexible electronic devices and systems realized on bendable and rollable substrates define important application fields of new paradigm for next-generation "consumer electronics."[1–6] In developing the highly-functional flexible electronic systems, an embeddable nonvolatile memory device is a strongly required as a core element for saving the power consumption[7] as well as for storing the information.

So far, various approaches using different operating origins and material combinations such as oxide-based[8] and polymer-based[9] resistive-type memory devices, have been tried to realize the nonvolatile memory functions on the flexible substrates. Among them, the ferroelectric-field-effect-based thin-film transistor (TFT) is one of the most promising candidates for the flexible memory devices.[10,11] The ferroelectric TFT can be operated in a very reproducible way with a definitely designable operation principle and simply be fabricated. The employment of polymeric ferroelectric thin film can offer an attractive solution to reduce the process temperature. A poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] is the most typical ferroelectric copolymer material. It shows superior properties of a relatively large remnant polarization, a short switching time, and a good thermal stability, compared with other organic ferroelectric materials.[12,13] The P(VDF-TrFE) thin film can simply be formed by a solution-based spin-coating method and be crystallized at a lower temperature around 140 °C, which is one of the benefits in realizing the memory device on the plastic substrate. Although most works on the fabrication and characterization for the nonvolatile memory transistors using the P(VDF-TrFE) have mainly been investigated for realizing all-organic memory transistors with organic semiconducting channel layers,[14,15] the weaknesses of a low field-effect mobility, an unsatisfactory ambient stability, and a difficult device integration with organic-based transistors seriously limit the scopes of application fields. A powerful alternative for enhancing and stabilizing the device performance is to utilize the oxide semiconductors such as ZnO or In-Ga-Zn oxide (IGZO). The oxide semiconductor-based TFTs present such beneficial features as high field-effect mobility, excellent uniformity, and robust device stability.[16,17] The combination of an organic ferroelectric gate insulator (GI) and an oxide semiconducting channel will be the best choice for the high performance nonvolatile memory transistors (MTFT). We previously demonstrated the feasibility of these MTFTs fabricated on the glass substrate.[18,19] In this letter, we propose an organic/inorganic hybrid-type flexible memory TFT (F-MTFT) by modifying some critical process steps in order to fabricate the MTFT with good performances even on the plastic substrate.

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Experimental

A top-gate F-MTFT was fabricated onto a 200-μm-thick poly(ethylene naphthalate) (PEN, Teijin DuPont) substrate, as schematically shown in Fig. 1a. Low coefficient of thermal expansion and strong chemical resistance are two important features of the PEN substrate. As the first step, 20-nm-thick Al_2O_3 was deposited by using an atomic-layer deposition (ALD) method on the bare PEN substrate as a barrier against out-gassing and a surface planarization layer. Multi-layered films of Ti/Au/Ti were then deposited by electron-beam (e-beam) evaporation and patterned into the source/drain (S/D) electrodes by lift-off process. Top and bottom layers of Ti are expected to work as a good ohmic contact with oxide channel layer and a good adhesive with the Al_2O_3-deposited substrate, respectively. This optimized S/D structure for the flexible substrate could replace the In-Sn-O (ITO) layer which had been used in our devices on the glass substrate. 10-nm-thick ZnO film was chosen as an oxide semiconducting channel for the F-MTFT. Although the oxide-channel TFT employing the ZnO show a relatively low field-effect mobility and moderate uniformity in device behaviors owing to its polycrystalline natures, the post-annealing process, which is generally demanded for obtaining stable TFT performances, can be carried out at a lower temperature compared with the TFTs using an IGZO channel. ZnO channel was prepared by plasma-enhanced ALD method at 150 °C using diethylzinc and O_2 plasma. Right after the ZnO deposition, 6-nm-thick Al_2O_3 interface controlling layer[18] was successively deposited by an ALD method at 150 °C using trimethylaluminium and water vapor. The channel areas were patterned by a wet etching of the Al_2O_3 and ZnO using a dilute hydrofluoric acid solution. Thermal treatment was then performed at 150 °C to enhance the ZnO channel properties. The employment of an Al_2O_3 barrier layer on the PEN, a multi-layered Ti/Au/Ti electrode, and a low-temperature compatible ZnO channel can be picked up as important features of the fabrication processes proposed for the F-MTFT.

Ferroelectric P(VDF-TrFE) GI was formed by spin-coating method using a 2.5 wt % diluted solution of P(VDF-TrFE) (70/30 mol %, VF2-TRFE, Solvay Solexis) in methyl ethyl ketone ($C_2H_5COCH_3$, CAS No. 78-93-3, Sigma Aldrich). The prepared film was crystallized at 140 °C for 1 h in an air ambient. The film thickness of P(VDF-TrFE) was measured to be approximately 150 nm. Via-holes were formed by removing the patterned areas of the P(VDF-TrFE), in which an O_2 plasma was applied in a vacuum dry etching chamber. Finally, Au film was deposited by e-beam evaporation and patterned as gate electrode and pads via lift-off process. Figures 1b and 1c show a microscopic top view of the fabricated F-MTFT and a typical photo image of the process-terminated bending substrate, respectively. The size of the processed PEN substrate was 2×2 cm^2.

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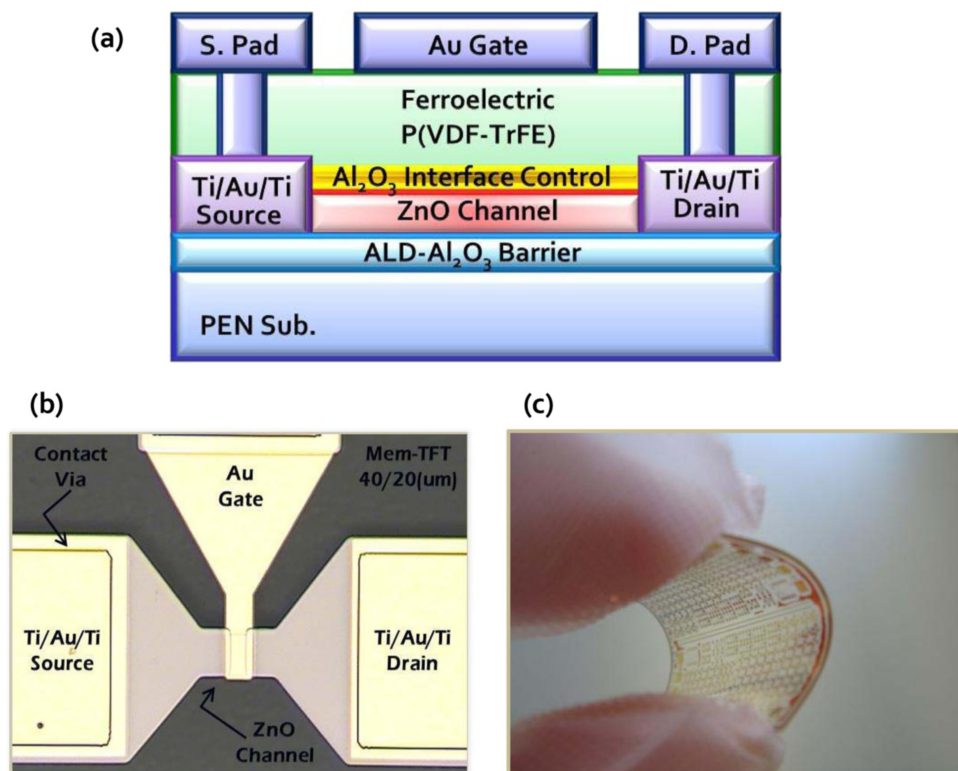

Figure 1. (Color online) (a) Schematic cross-sectional diagram of the proposed F-MTFT. (b) Microscopic top-view of the fabricated F-MTFT with the structure of Au/P(VDF-TrFE)/Al_2O_3/ZnO/Ti/Au/Ti/Al_2O_3/PEN. The channel width and length are 40 and 20 μm, respectively. (c) A typical photo image of the PEN substrate under a bending situation. The substrate size is 2×2 cm^2.

All the electrical characteristics including programming and retention behaviors of the fabricated F-MTFT were evaluated in a dark box at room temperature using a semiconductor parameter analyzer (Agilent B1500A) equipped with pulse generation units. The variations in their characteristics under bending situations and repeated bending cycles with a given curvature radius (R) were measured by setting the specified configurations.

Results and Discussions

Figure 2a shows the drain current-gate voltage (I_{DS}-V_{GS}) characteristics and the gate leakage current of the fabricated F-MTFT at a drain voltage (V_{DS}) of 5.0 V. The gate width (W) and length (L) of the evaluated F-MTFT were 40 and 20 μm, respectively. The transfer curve showed a counterclockwise hysteresis for a double sweep mode of forward and reverse directions of V_{GS}. The turn-on voltage (V_{on}) of the F-MTFT, which can be defined as the V_{GS} where the I_{DS} starts to flow from the off state, was shifted owing to the ferroelectric field-effect of the P(VDF-TrFE) GI. This voltage shift of V_{on} in the ferroelectric-based MTFT is termed the memory window (MW). The MW was observed to be approximately 7.8 V for a V_{GS} sweep range from -14 to 12 V. If the programmed I_{DS}'s are read at a V_{GS} of 0 V, the memory margin between the on and off states would be obtained to be more than 8-orders-of magnitude. Furthermore, our F-MTFT also exhibited good TFT performances such as a high field-effect mobility of approximately 33.3 cm^2 V^{-1} s^{-1} and a subthreshold swing (SS) of approximately 0.65 V/dec. The gate leakage currents could be suppressed to be lower than 10^{-11} A, even though the device was fabricated on the plastic substrate using a low-temperature processes below 150 °C. It was also confirmed that the transfer characteristics did not change between the first and the second sweeps of a V_{GS}. This is an important point in that the transfer curves of the MTFT employing the ferroelectric P(VDF-TrFE) GI are markedly fluctuated if the fabrication processes are not totally optimized. Although only two repeated measurements of the transfer curves cannot guarantee the program endurance in device performance, the undesirable variations in device characteristics during the repetitive operations could be easily examined even by performing only two successive sweeps for the F-MTFT. Therefore, it can be concluded that the proposed F-MTFT was well fabricated on the PEN substrate without any critical damage caused by fabrication processes. The variations in the MW at various sweep ranges of a V_{GS} were examined, as shown in Fig. 2b. The width of the MW gradually increased from 3.3 to 7.8 V when the V_{GS} sweep ranges were varied from -6 to 4 V to -14 to 12 V. The MW was obtained to be as wide as approximately 4.7 V even when the sweep range was -8 to 6 V. This indicates that our proposed F-MTFT can be operated and programmed with a sufficiently low voltage.

For the flexible memory applications, the variations in device behaviors against mechanical bending deformation need to be examined for the fabricated F-MTFT. Two concerns are related to the bending characteristics of our F-MTFT. The first issue is the mechanical strain effect on the ferroelectric behaviors of the P(VDF-TrFE), such as ferroelectric polarization and switching mechanism. We have confirmed that the mechanical strain applied to the P(VDF-TrFE) capacitor under the substrate bending situations do not make any critical influence on the ferroelectric properties such as remnant polarization, coercive field, and switching behaviors.[20] The second issue is the mechanical and/or electrical damage induced by bending strain to the ZnO channel layer. Because the inorganic oxide film has a brittle nature, mechanical failures of the TFT fabricated on the flexible substrate may be an important concern. There have been several reports on mechanical damages to amorphous-Si TFTs prepared on flexible substrates.[21,22] Similar mechanical damage to inorganic gate dielectric buffer layer as thick as 350 nm was reported for the case of IGZO TFT when it was fabricated on 90-μm-thick polyimide substrate.[23] The fabrication process, overall thermal budget, and device structure should be carefully designed. The main difference of our proposed F-MTFT is a hybrid combination of polymeric GI and inorganic oxide channel.

The bending characteristics were examined for the same F-MTFT as investigated in Fig. 2, in which two series of

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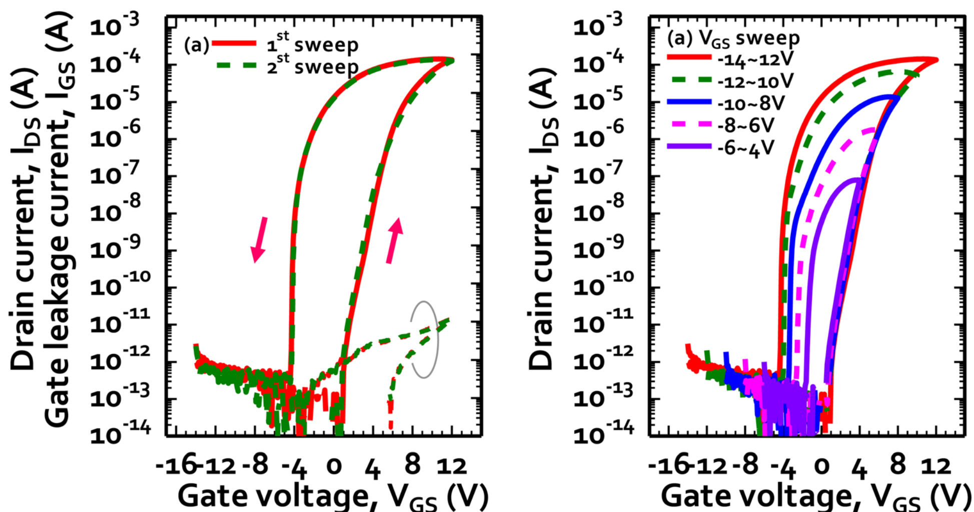

Figure 2. (Color online) (a) I_{DS}-V_{GS} characteristics and the gate leakage currents of the F-MTFT fabricated on the PEN substrate for a double sweep mode of forward and reverse directions of V_{GS}, in which the measurements of transfer characteristics were repeatedly performed. (b) Sets of I_{DS}-V_{GS} transfer curves when the V_{GS} sweep ranges were varied from −6 to 4 V to −10 to 12 V. The V_{DS} was set to be 5 V.

measurements were performed. The first test is related to the changes in device behaviors at the situations of substrate bending with a given R, which can be called "bending durability". The second test is related to the degradation in device performance after a given numbers of repetitive bending operations, which can be called"bending fatigue endurance". Figure 3a shows the bending durability by measuring I_{DS}-V_{GS} transfer characteristics and gate leakage currents when the substrate was bent with a R of 0.97 cm. The probing configuration for the bending durability test can be shown in Fig. 3b. The fabricated F-MTFT did not show so marked variations in its device behaviors of mobility, threshold voltage, and SS. The change in memory window at the bending situation was approximately 0.7 V at most. The off-state and gate leakage currents did not increase even at the bending situation.

It was also very encouraging that the overall device characteristics were not degraded after the bending fatigue endurance test until 20,000 cycles, as shown in Fig. 3c, even though a very small reduction in the MW of the F-MTFT was observed as the increase in the number of bending fatigue cycles. In this evaluation, bending fatigue cycles were intentionally loaded by using a specially-designed bending machine shown in Fig. 3d. The R was set to 2.35 cm. The obtained results indicate that the proposed F-MTFT fabricated on the PEN substrate may sufficiently be available under bending situations for any flexible devices. Subsequent microscope inspection

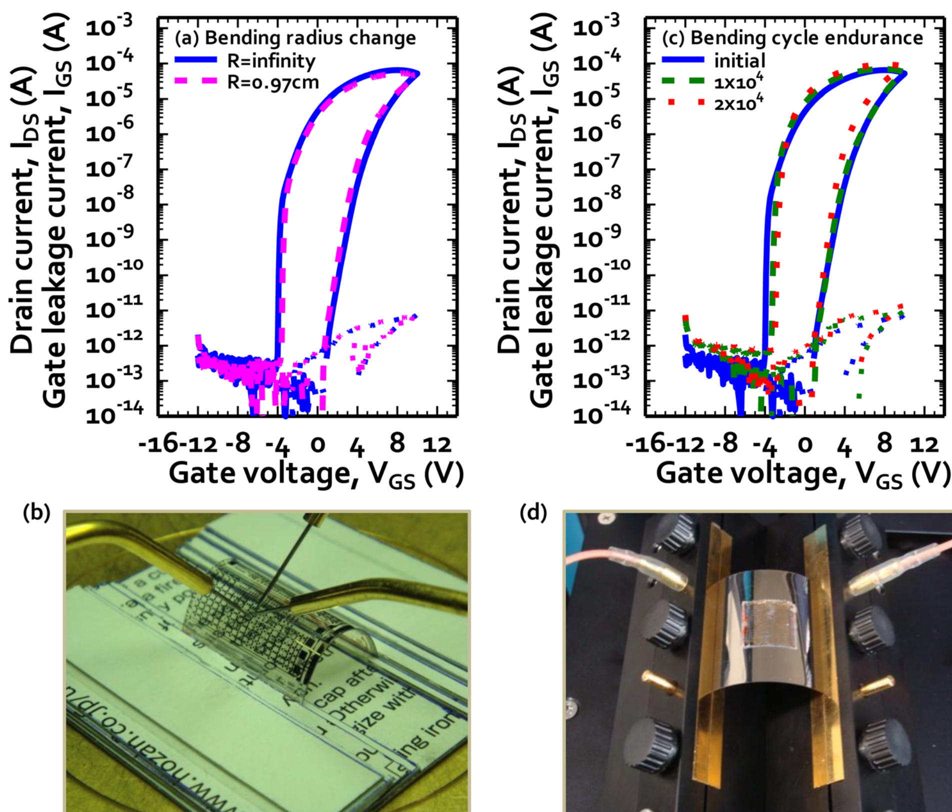

Figure 3. (Color online) Variations of transfer characteristics and memory behaviors of the fabricated F-MTFT (a) under a substrate bending situation with a R of 0.97 cm and (c) after 20,000 cycles of repetitive bending operations with a R of 2.35 cm. (b) A photo image of an electrical evaluation for the fabricated device when the PEN substrate was bent. (d) A typical photo image of the bending fatigue evaluation performed by a specially-designed bending machine.

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after the bending test revealed that there were no cracks, deformation, and delamination of the constituent layers for the F-MTFT over the full area of PEN substrate. The organic-inorganic hybrid-type gate stack can be an apparent benefit not only to enhance the device performances but also to relax the mechanical strain for flexible applications. Although the electrical cycling endurances of the F-MTFT were not evaluated owing to the inconvenience of measurement system, the properties can be inferred from the data obtained for the P(VDF-TrFE) capacitors, because the cycling endurance is mainly related to the fatigue behaviors of the P(VDF-TrFE). The stable polarization switching was verified during 1×10^5 cycles,[24] which is comparable to the programming endurance of conventional flash memory.

Finally, the programming and retention behaviors of the fabricated F-MTFT were evaluated. The programming pulsing sequences are shown in Fig. 4a. In order to program the on state, an initial pulse of −8 V high was first applied to the gate to initialize the ferroelectric polarization of the P(VDF-TrFE) GI, then a 6 V high program pulse was applied. Similarly, for the case of the off state, an initial pulse of 6 V high and a program pulse of −8 V high were sequentially applied. The duration of program pulse is defined as a program time (t_{prog}), in which the t_{prog} was varied to 1 s and 100 ms in order to estimate the relationship between the available memory margin and the t_{prog}. Both memory states were detected by measuring the I_{DS} at a read-out V_{GS} of 0 V. Figure 4b shows the variation of programmed drain currents for the on and off states with time. The initial on/off ratio was only 8.0×10^3 and the memory margin almost disappeared during the retention phase when the t_{prog} was reduced to 100 ms. On the other hand, when the t_{prog} was set to 1 s, the on/off ratio was initially obtained to be approximately 6.6×10^5 and it remained to be approximately 130 after a lapse of 15,000 s. It was sufficiently encouraging to confirm the on/off ratio of higher than 2-orders-of magnitude for the F-MTFT fabricated on the PEN substrate at lower temperature even after a lapse of 4 h. However, the programming and retention behaviors should be much more improved for practical flexible memory applications.

The typical retention times of the previously reported MTFT employing the polymeric ferroelectric GI and oxide channel are in the range of several hours even when they were fabricated on the glass substrate.[25–27] The main reasons for the retention degradation can be classified into several origins such as an intrinsic depolarization field,[28] a gate leakage component, an interface quality,[18] and/or an n-type nature of the P(VDF-TrFE).[29] Some approaches to improve the insulating property of P(VDF-TrFE) by blending PMMA[30] and to optimize the interface controlling layer[31] have been tried to enhance the retention performance. One more concern is that the obtained programming characteristics were sensitively dependent on the program time (program pulse width), which has a direct influence on the programming speed of the F-MTFT. The retention time and program speed are closely associated each other.[32] It may be an important trade-off for practical flexible memory applications that a long-time programming is definitely preferable to obtain a longer retention time. We have recently confirmed that the dual-gate configuration can be a very effective prescription to improve both requirements of the program speed and data retention time.[33]

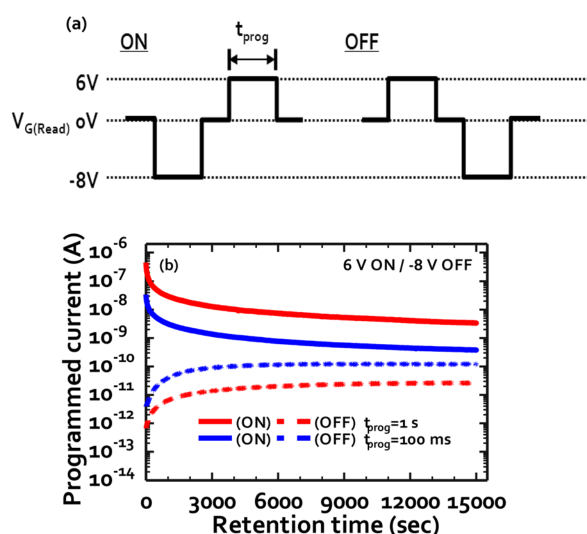

Figure 4. (Color online) (a) The pulsing sequences for programming the on and off states. (b) Data retention behaviors of the fabricated F-MTFT as the changes in programmed I_{DS} with a lapse of 15,000 s. The on and off states were programmed by applying the voltage pulses of 6 and −8 V, respectively. The t_{prog} was varied to 1 s and 100 ms.

Conclusions

In this work, we proposed and demonstrated the flexible nonvolatile MTFT employing the ferroelectric copolymer GI and oxide semiconductor active channel as a memory component for the flexible-type electronic devices. The device structure was designed to be Au/150 nm P(VDF-TrFE)/6 nm Al_2O_3/10 nm ZnO/Ti/Au/Ti/PEN. The memory characteristics of the fabricated F-MTFT were evaluated, in which a 7.8 V memory window and 8-orders-of magnitude on/off ratio were successfully obtained. These characteristics did not experience so marked degradations at the bending situation with a R of 0.97 cm and after the repetitive bending of 20,000 cycles. We can conclude from the obtained results that our proposed hybrid-type F-MTFT can be a suitable candidate for an embeddable memory device to realize the low-cost flexible electronic applications.

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