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Solution-Processed Zinc Indium Oxide Transparent Nonvolatile Memory Thin-Film Transistors with Polymeric Ferroelectric Gate Insulator

Sung-Min Yoon,[a,b,z] Shin-Hyuk Yang,[b] Soon-Won Jung,[b] Chun-Won Byun,[b] Sang-Hee Ko Park,[b] Chi-Sun Hwang,[b] and Hiroshi Ishiwara[a,*]

[a]*Tokyo Institute of Technology, Yokohama 226-8502, Japan*
[b]*Convergence Components and Material Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea*

A solution-process-based nonvolatile memory thin-film transistor (MTFT) was demonstrated to realize simple and low cost memory devices for future large-area electronics. The semiconducting active channel of zinc indium oxide (ZIO) and a gate insulator of poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] were prepared by a spin-coating method using corresponding precursor solutions. The obtained ZIO film was amorphous and showed an excellent transmittance (~90%) in the visible range. The MTFT showed a turn-on voltage shift originating from the ferroelectric nature of P(VDF-TrFE), a field-effect mobility of 3.3 $cm^2\ V^{-1}\ s^{-1}$, and a subthreshold swing of 0.86 V/dec with an on/off current ratio of 8.4×10^6.
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The thin-film transistor (TFT) with nonvolatile memory function can be one of the key devices to realize highly functionalized, large-area electronic systems such as an active matrix display panel[1,2] and various sensor applications.[3,4] These memory thin-film transistors (MTFTs) have features of mechanical flexibility and transparency in the visible range. For these fields, the employment of a solution-based process is very desirable because it provides us many advantages such as a simpler process, lower cost, and higher throughput compared to the conventional vacuum-deposition-based methods. The MTFT composed of a ferroelectric gate insulator (GI) and an oxide semiconducting channel is a good approach. Because a relatively high crystallization temperature required for the sol–gel-driven oxide ferroelectric films such as $Pb(Zr,Ti)O_3$ may restrict the scope of process window and applications,[5-7] the use of a ferroelectric copolymer is more acceptable.

A typical ferroelectric copolymer of poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] can be formed by means of a simple spin-coating method and crystallized at a lower temperature of around 140°C.[8,9] Although the P(VDF-TrFE) has been employed with various organic semiconductor to fabricate such MTFTs,[10-12] the change of the active channel into the oxide semiconductor can be a good choice in obtaining higher mobility and better stability in device behaviors. Various oxide-based TFTs have been fabricated by a solution-based process using ZnO,[13,14] zinc tin oxide,[15,16] indium gallium zinc oxide,[17,18] indium zinc oxide (IZO),[19,20] and aluminum indium oxide.[21] News that a prototype active matrix organic light emitting diode display panel using solution-processed IZO TFT was demonstrated is also very encouraging.[22] However, the combination of spin-coated P(VDF-TrFE) ferroelectric GI with the solution-processed oxide semiconducting channel has seldom been attempted for the promising candidate of embeddable nonvolatile memory device for large-area electronics, although there have been only a few articles on the MTFTs using sputtered or atomic-layer deposited ZnO active layers.[23,24]

In this article, we present the MTFTs fabricated using the solution-processed, amorphous Zn-rich phase of zinc indium oxide (ZIO) active channel and P(VDF-TrFE) GI. Good transistor behaviors and nonvolatile memory operations of the ZIO MTFT were demonstrated.

ZIO precursor solution was prepared by diluting and blending the commercial metallorganic solutions of ZnO (SYM-ZN20, 2 M) and In_2O_3 (SYM-IN02, 0.2 M), which were synthesized by Kojundo Chemical Laboratory. Co. *n*-Butyl acetate [$CH_3COO(CH_2)_3CH_3$, CAS-no. 123-86-4] was employed as the solvent for the dilution process. The final solution concentration of 0.2 M was chosen by considering the viscosity and wetting events on the glass substrates. Dilution and blending were performed at 60°C for more than 1 h with stirring. The molar ratio of the ZIO solution was adjusted to be 5:1 (Zn:In). The resulting solution was filtered through a 0.45 μm syringe filter (cellulose) and then deposited on the substrates by a spin-coating method at 2500 rpm for 20 s. The crystallinity of the prepared film was investigated by using X-ray diffraction (XRD, Rigaku RU-200BH) with Cu Kα radiation (40 kV/60 mA) at a scan rate of 2°/min. The optical transmission spectrum was measured by a UV spectrophotometer (Shimadzu UV-1800).

We fabricated a bottom-gate ZIO TFT with a conventional Al_2O_3 GI and a top-gate MTFT with P(VDF-TrFE) ferroelectric GI for comparison. An indium tin oxide (ITO)-coated glass substrate was employed for the fabrication of both TFTs, on which 150 nm thick ITO was patterned into the gate and source/drain (S/D) electrodes for the bottom- and top-gate TFTs, respectively. For the bottom-gate TFT, 80 nm thick Al_2O_3 GI was deposited at 200°C by the atomic layer deposition method using trimethylaluminum and water vapor as Al and O_2 sources, correspondingly. Via-holes for the contact with the ITO gate were formed by wet etching of the Al_2O_3 layer. The ZIO thin film was formed by using the previously prepared precursor solution on the Al_2O_3 GI layer. The thickness of the film could be controlled by the repetitive coating process, and the resultant film thickness was approximately 40 nm after twice coating. After the gate patterning of the ZIO channel region using a diluted hydrochloric acid-based etchant, the annealing process was carried out at 400°C for 1 h in an oxygen ambient Finally, the Al film was deposited by a thermal evaporation method and patterned via a lift-off process for the S/D electrodes and gate pads. Figure 1a and b shows a cross-sectional schematic diagram and a photograph of the fabricated bottom-gate solution-processed ZIO TFT, respectively.

For the MTFT, the ZIO thin film was deposited on the S/D patterned substrate by using the same process that was used for the bottom-gate TFT fabrication. After the channel patterning and thermal annealing processes (at 400°C for 1 h in an O_2 ambient) of the ZIO layer, a P(VDF-TrFE) film was deposited by a spin-coating method using a 3 wt % diluted solution of P(VDF-TrFE) (70/30 mol %, VF2-TRFE, Solvay Solexis) in methyl ethyl ketone. The prepared film was crystallized by performing the annealing process at 140°C for 1 h. The resultant film thickness was approximately 150 nm. The given areas of P(VDF-TrFE) were removed to form the S/D contacts by the etching process using O_2 plasma. Similarly, the gate electrode and S/D pads were finally formed by the deposition and patterning of Al film. Figure 1c and d shows a cross-sectional schematic diagram and a photograph of the solution-processed ZIO-

* Electrochemical Society Active Member.
[z] E-mail: sungmin@etri.re.kr

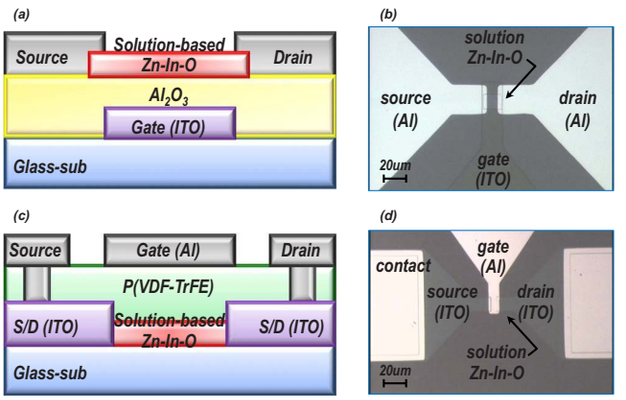

Figure 1. (Color online) [(a) and (c)] Schematic cross-sectional diagrams and [(b) and (d)] photographs of the bottom-gate ZIO TFT using Al_2O_3 GI and the top-gate ZIO TFT using P(VDF-TrFE) GI, respectively. The gate widths and lengths of both TFTs were 20 and 10 μm, respectively.

based ferroelectric MTFT, respectively. The electrical characteristics of both TFTs were evaluated using a semiconductor parameter analyzer (HP4156C) in a dark box at room temperature.

Figure 2a shows the optical transmission spectra of the ZIO films prepared at different temperatures on the glass substrate. The solution-processed ZIO films exhibited a high transmittance of more than 90% in the visible range (400–700 nm), which was almost the same as that of the bare glass substrate. The transmittance of the ZIO film annealed at 400°C was observed to be better than that of the film dried at 250°C. This improvement of transmittance may originate from the complete removal of organic residue and the slight increase in crystallinity when the film was thermally treated at 400°C. The transparency of the film can also be confirmed from the top view of the optical image of the ZIO film, as shown in the inset of Fig. 2a.

The crystalline phases of the ZIO films were investigated by XRD patterns, as shown in Fig. 2b, in which the film thickness was increased to approximately 100 nm to clearly confirm the changes in crystallinity for films prepared at different annealing temperatures. The XRD patterns did not show any distinct peaks, such as ZnO(100) at $2\theta = 31.7°$, ZnO(002) $2\theta = 34.4°$, ZnO(101) $2\theta = 36.2°$ (JCPDS file no. 36-1451), $In_2O_3(222)$ $2\theta = 30.6°$, and $In_2O_3(400)$ $2\theta = 35.5°$ (JCPDS file no. 06-0416) even for the 400°C annealed film. This indicates that the solution-processed ZIO films are essentially amorphous. It is likely that the addition of 17 mol % In into ZnO suppressed the progress of crystallization of ZnO, considering that pure ZnO is easily crystallized at a relatively low annealing temperature.

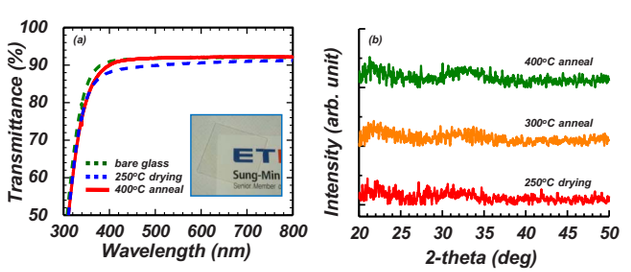

Figure 2. (Color online) (a) Optical transmittance spectra of the solution-processed ZIO film prepared at different temperatures of 250 and 400°C. Transmittance of the bare glass is also plotted. The inset shows a top view of optical image of the ZIO film. The substrate size was 2 × 2 cm. (b) XRD patterns for the ZIO film treated at various temperatures of 250, 300, and 400°C.

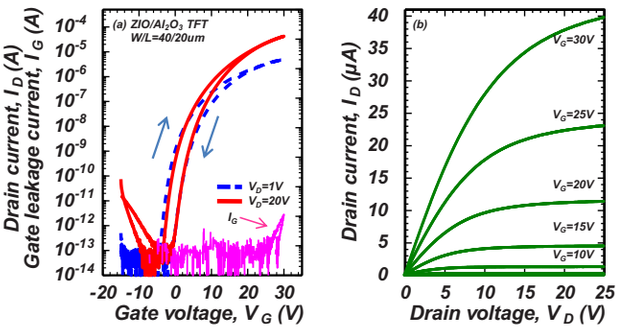

Figure 3. (Color online) (a) I_d-V_g transfer characteristics and (b) I_d-V_d output characteristics of the fabricated bottom-gate solution-processed ZIO TFT (W/L = 40/20 μm). The gate leakage current is also plotted in (a).

Figure 3a shows the drain current (I_d)–gate voltage (V_g) transfer curves for the fabricated bottom-gate ZIO TFT. Transfer curves were measured in the double sweep mode at two drain voltages (V_d's) of 1.0 and 20.0 V for the TFTs with the gate width (W) and length (L) of 40 and 20 μm, respectively. The off current was defined to be as low as 10^{-13} A and the on/off ratio in I_d amounted to more than 10^8 at the V_d of 20 V. The gate leakage current was also sufficiently low (10^{-11} A) even at the V_g of 30 V. The field-effect mobility at the saturation regime and the subthreshold swing (SS) were estimated to be approximately 1.3 cm^2 V^{-1} s^{-1} and 0.92 V/dec, respectively. These values are comparable to those reported for other TFTs using solution-processed oxide active channels. The hysteresis observed in the transfer curves between forward and reverse directions in V_g sweep was ascribed to the degradation of interface between the ZIO channel and Al_2O_3 GI layers, which might result from the relatively high process temperature of 400°C for the ZIO film deposited on the GI layer. The clockwise direction of hysteresis typically indicated that charge trapping/detrapping process occurred at or near the interface between the ZIO active and GI layers. Figure 3b shows the drain current (I_d)–drain voltage (V_d) output characteristics when the V_g was varied from −15 to 30 V. The TFT exhibited good ohmic behaviors in the linear region without current crowding. Excellent gate modulation and hard saturation behaviors were also confirmed for the saturation region, which is very desirable for the most practical applications.

Based on these basic investigations on the ZIO film prepared by the solution process, we characterized the transistor and memory behaviors of the fabricated top-gate ZIO MTFT with the W and L of 40 and 20 μm, respectively. Figure 4a shows the sets of I_d-V_g transfer curves with the variation in V_g sweep ranges. A counterclockwise

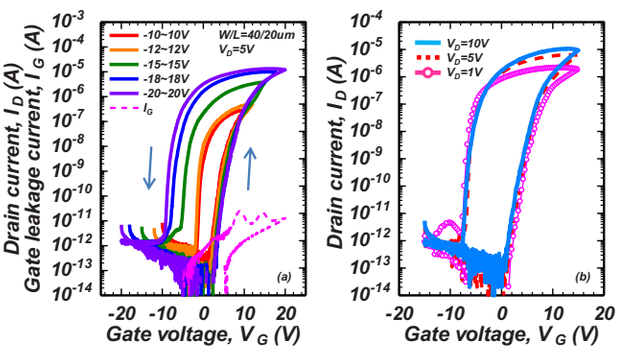

Figure 4. (Color online) Sets of I_d-V_g transfer curves of the fabricated top-gate ZIO ferroelectric MTFT (W/L = 40/20 μm) (a) at the V_d of 5 V when the V_g sweep ranges increased from −10 to 10 V to −20 to 20 V, and (b) when the V_d was varied to 1, 5, and 10 V.

direction hysteresis in the transfer characteristics was clearly observed for all curves. These shifts in the turn-on voltage of the MTFT (V_{on}), which was defined as the voltage when the I_d jumped up from the off state, resulted from the ferroelectric remnant polarization of the P(VDF-TrFE) GI layer. The memory window (voltage width of V_{on} shift) was observed to increase from 4.6 to 14.2 V when the V_g sweep ranges increased from −10 to 10 V to −20 to 20 V. It was also very desirable that the obtained memory window was located with centering around 0 V in V_g. Therefore, we do not need any additional bias condition for the read-out operation to maximize the memory margin. The gate leakage current was confirmed to be lower than 10^{-11} A. The field-effect mobility, SS, and the on/off ratio in I_d were typically obtained to be 3.3 cm^2 V^{-1} s^{-1}, 0.86 V/dec, and 8.4×10^6, respectively. It was also confirmed that the I_d's were accurately amplified with the increase in V_d without critical changes in memory window and V_{on} in the transfer characteristics, as shown in Fig. 4b. If the obtained hysteretic behaviors dominantly originate from the undesirable ion-drift or mobile charges, the width of the memory window and the V_{on} inevitably experience a series of fluctuation during the continuously performed I_d-V_g evaluations.

The retention and endurance characteristics are also very important for these nonvolatile memory devices. We evaluated the programming and retention behaviors of the fabricated MTFT (not shown here). The programming operations were confirmed to be normally conducted when the programming voltage pulses of more than 15 V were applied to the device. The memory on/off ratio was initially obtained to be approximately 5×10^5 when the voltage pulses with ±20 V and 990 ms were applied for the programming of on and off states, and it still remained to be more than 500 even after 10 h. The endurance against the repetitive rewriting operations could be expected to be more than 10^7 cycles. These characteristics evidently indicated that our MTFT has excellent performance, of which the gate stack was composed of solution-based ferroelectric copolymer GI and oxide semiconducting channel layers.

In summary, we reported the fabrication of nonvolatile MTFT using a solution-process-based organic–inorganic hybrid-type gate structure composed of ZIO active channel and P(VDF-TrFE) GI layers. The ZIO film prepared by a precursor solution was highly transparent (~90%) in the visible range and was observed to be amorphous at annealing temperatures up to 400°C. The feasibility of the prepared ZIO film as a channel material for a TFT was well confirmed by the fabrication of the conventional bottom-gate TFT with the structure of Al (S/D)/40 nm ZIO/80 nm Al_2O_3/ITO (gate), in which the field-effect mobility of 1.3 cm^2 V^{-1} s^{-1}, SS of 0.92 V/dec, on/off ratio of more than 10^8, and good saturation behaviors in I_d were obtained. The MTFT fabricated with the gate structure of Al/150 nm P(VDF-TrFE)/40 nm ZIO showed a ferroelectric field-effect-driven memory window in its transfer characteristic. The memory window at V_g sweep of ±15 V, field-effect mobility, SS, and on/off ratio were obtained to be 9.6 V, 3.3 cm^2 V^{-1} s^{-1}, 0.86 V/dec, and 8.4×10^6, respectively. This work successfully demonstrated a simple and low cost solution process to fabricate high performance embeddable nonvolatile memory devices for various large-area electronic systems.

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