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Effect of ZnO channel thickness on the device behaviour of nonvolatile memory thin film transistors with double-layered gate insulators of Al_2O_3 and ferroelectric polymer

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Abstract
Poly(vinylidene fluoride trifluoroethylene) and ZnO were employed for nonvolatile memory thin film transistors as ferroelectric gate insulator and oxide semiconducting channel layers, respectively. It was proposed that the thickness of the ZnO layer be carefully controlled for realizing the lower programming voltage, because the serially connected capacitor by the formation of a fully depleted ZnO channel had a critical effect on the *off* programming voltage. The fabricated memory transistor with Al/P(VDF–TrFE) (80 nm)/Al_2O_3 (4 nm)/ZnO (5 nm) exhibits encouraging behaviour such as a memory window of 3.8 V at the gate voltage of −10 to 12 V, and 10^7 *on*/*off* ratio, and a gate leakage current of 10^{-11} A.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The features of low-cost and low-temperature process below 200 °C for ferroelectric polymer-based nonvolatile (NV) memories can be expected to give us a new chance to realize embedded memories for the new field of flexible electronics. Among them, polyvinylidene fluoride (PDVF) and copolymer with trifluoroethylene [P(VDF–TrFE)] have been applied for the ferroelectric capacitor and field-effect transistor applications, which are most well-known polymer ferroelectric materials with the best performances [1, 2]. In most previous approaches to thin-film-transistor (TFT)-type memory devices using P(VDF–TrFE), organic semiconductors such as pentacene and poly(3-hexylthiophene) have been mainly picked as active channels owing to their mechanical flexibility and solution-process compatibility [2–7]. However, the handicaps of small *on*/*off* ratio, poor ambient stability and low field-effect mobility for the organic TFTs restrict the practical memory application within narrow limits. Another promising candidate as a semiconducting channel for P(VDF–TrFE)-based memory TFTs (MemTFTs) is oxide semiconductors such as ZnO. The better stability in device behaviour and higher mobility of oxide TFTs can be beneficial features for NV-MemTFTs. Furthermore, its transparency in the visible range and compatibility with low-temperature process are very appropriate for future ubiquitous information systems with transparent and flexible features. Because the oxide semiconducting channels are patterned only in small gate areas on the substrate, there is no problem in fabricating the device on plastic substrates. The studies on MemTFTs using oxide semiconductors have been focused on charge-trap devices, in which a thin charge-trap layer or nano-particles were embedded within the gate stack [8–11]. However, these devices require complicated

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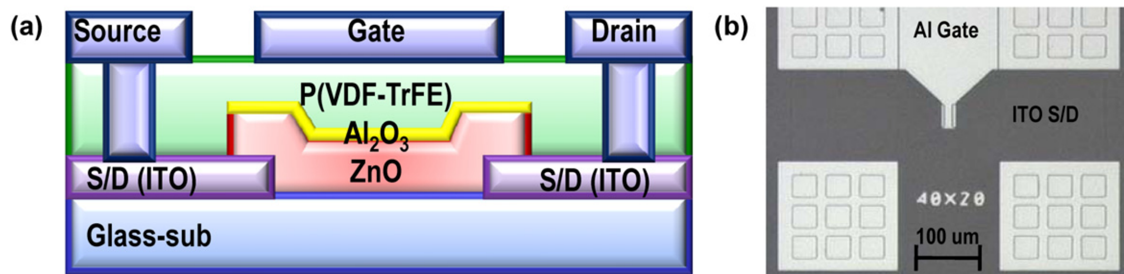

Figure 1. (*a*) Cross-sectional schematic diagram and (*b*) photograph of the fabricated NV-MemTFTs with Al/P(VDF–TrFE)/Al_2O_3/ZnO/glass structure. (Color online.)

fabrication procedures and strict operational conditions in controlling the quantity of trapped charges. In contrast, the device structure and operation scheme for the MemTFTs exploiting the ferroelectric nature of the gate insulator are very simple and clear. Nevertheless, only a few studies on MemTFTs composed of polymeric ferroelectrics and oxide semiconductors have been reported [12, 13]. For realizing this hybrid-type NV-MemTFT with good performances such as lower operating voltage and longer memory retention, it is critical to optimize the structure of the gate stack. In this paper, we have investigated the effect of thickness variation in semiconducting channels on the memory device behaviour and proposed the optimized gate stack structures for MemTFTs using ferroelectric polymer insulator and oxide semiconductor. This is the first attempt to exploit the active channel thickness for improving the memory behaviour, although there have been some reports suggesting that MemTFTs using the oxide semiconducting channel operate in accumulation/depletion mode [14, 15]. The importance of controlling the channel thickness for memory transistors using oxide semiconductors has been overlooked so far, while the reduction of the equivalent oxide thickness of the gate insulator has mainly been carried out for lowering the operation voltage of the TFT [16–18].

2. Experimental details

We selected ZnO as an oxide semiconducting channel for the MemTFTs. Two main schemes were applied for the fabrication of NV-MemTFTs in this work. The first scheme is to employ a thin Al_2O_3 layer between the ZnO and P(VDF–TrFE) layers, which protects ZnO during the fabrication procedures [19] and suppresses the leakage currents through the gate stack. The second one is to decrease the film thickness of the ZnO channel to around 5 nm. The control of active channel thickness is very important in the proposed MemTFTs, because the TFT operates between the accumulation and full depletion regions in transistor actions. The details will be discussed in the following with the obtained results. The fabrication procedures are as follows. 150 nm thick indium tin oxide (ITO) was patterned into the source/drain (S/D) electrodes. ZnO was deposited by plasma-enhanced atomic-layer deposition (PEALD) at 200 °C with diethylzinc (DEZ) and O_2 plasma (at radio-frequency power of 130 W) as the Zn and O_2 sources, respectively. The thickness of the prepared ZnO film was varied to approximately 5 and 20 nm. A 4 nm thick Al_2O_3 layer was initially deposited on ZnO with the ALD methods using water vapour at 200 °C. Trimethylaluminium (TMA) was used as the Al precursor. After ZnO and Al_2O_3 were patterned into the shape of the channel, a P(VDF–TrFE) thin film was deposited by the spin-coating method using a 3 wt% diluted solution of P(VDF–TrFE) (70/30 mol%) in dimethylformamide (DMF). The film was annealed at 140 °C for 1 h in ambient air for its crystallization. The film thickness was measured to be approximately 80 nm. To form the via holes for the S/D contacts, the given areas of P(VDF–TrFE) were removed by the plasma etching process using O_2 plasma, in which the lithography processes including developing and stripping of photo-resists on the P(VDF–TrFE) film were so carefully designed as not to cause any undesirable damage to the P(VDF–TrFE) film. Finally, the Al film was deposited as the gate electrode and S/D pads using thermal evaporation and was patterned by wet etchant. Figures 1(*a*) and (*b*) show a cross-sectional schematic diagram and a photograph of the fabricated MemTFT with Al/P(VDF–TrFE)/Al_2O_3/ZnO gate stack, respectively. The electrical behaviour of the MemTFT was evaluated using a semiconductor parameter analyzer (B1500A, Agilent) at room temperature.

3. Results and discussion

In advance, the basic ferroelectric properties of the 80 nm-thick P(VDF–TrFE) film prepared on the Pt substrate were confirmed, as shown in figure 2. The top electrode was Au of diameter 200 μm. The remanent polarization and coercive field were typically measured to be approximately 9.5 $\mu C\,cm^{-2}$ and 800 $kV\,cm^{-1}$, respectively, at the frequency of 1 kHz. This result suggests that the prepared P(VDF–TrFE) thin film showed good ferroelectric characteristics even when the thickness was chosen to be below 100 nm. Figures 3(*a*) and (*b*) show the drain current (I_D)–gate voltage (V_G) transfer curves and the gate leakage currents (I_G) for the fabricated MemTFTs with the ZnO thicknesses of 5 nm (Dev-1) and 20 nm (Dev-2), respectively, which were measured in a double sweep mode at two drain voltages (V_Ds) of 0.1 V and 1.1 V for the MemTFTs with the gate width and length of 40 μm and 20 μm, correspondingly. The counterclockwise direction of the transfer curves in both devices clearly indicated that the shifts of turn-on voltage of the TFT (V_{on}), which was defined as the voltage when the I_D was launched from the *off*-state current of the TFT, resulted from the ferroelectric nature of

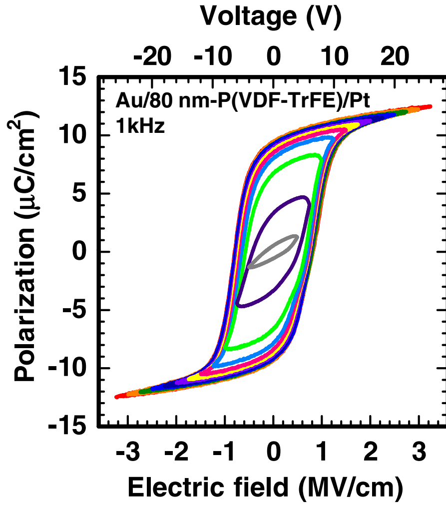

Figure 2. Polarization versus electric field (P–E) characteristics for the Au/80 nm-P(VDF–TrFE)/Pt capacitor. The top electrode size was 200 μm in diameter. The measurement frequency was 1 kHz. (Color online.)

P(VDF–TrFE). The widths of the memory window (MW) of Dev-1 and Dev-2, which are determined to be the quantity in shift of V_{on}, were confirmed to be approximately 3.8 V and 2.7 V with the V_G sweep from −10 V to 12 V (at $V_D = 0.1$ V), respectively. Good electrical characteristics were also observed in the viewpoints of the transistor. A sufficiently low I_G as low as 10^{-11} A, steep subthreshold swing (SS) of approximately 400 mV/dec, and 7-orders-of-magnitude I_{on}/I_{off} ratio (at $V_D = 1.1$ V) are excellent characteristics for the NV-MemTFTs using polymeric ferroelectrics, that have not been reported so far. The slight increase in I_D observed at the reverse sweep in V_G might be related to the fact that I_G was also experiencing counterclockwise hysteresis owing to the remanent polarization of the ferroelectric gate insulator. It can be said that these results were successfully obtained thanks to the contribution of the inserted 4 nm thick Al_2O_3 layer, although we did not fabricate the MemTFT without the Al_2O_3 layer. We have to note that the ZnO film is easily degraded by the chemical processes such as conventional lithography for the active patterning and spin-coating of P(VDF–TrFE) solution. Therefore it was very difficult to obtain stable transistor actions without the introduction of Al_2O_3.

The difference in MW between the two devices can be explained by the variation of active channel thickness. The programming voltages for the *on* ($V_{W,on}$) and *off* ($V_{W,off}$) operations of the MemTFTs are determined as the summation of the applied voltages to P(VDF–TrFE) (V_F), Al_2O_3 (V_{ox}) and the depletion layer (V_{dep}) of the ZnO channel, because they are required to completely program the data states of *on* and *off*. $V_{W,on}$ and $V_{W,off}$ are generally decided to be larger than the operating voltages of ordinary TFTs. It relates to the fact that the use of saturated ferroelectric hysteresis loop is absolutely desirable to guarantee the stable memory operations of the MemTFTs. The minor loops having partial ferroelectric polarization generally show a very weak immunity against the depolarization field during the data retention period [20]. Eventually, from the viewpoint of reducing the operation voltage for the MemTFTs, we have to reduce $V_{W,on}$ and $V_{W,off}$.

We performed load-line analysis to estimate the programming voltages, as shown in figure 4, at which the ferroelectric polarization in the P(VDF–TrFE) film is assumed to be fully saturated. For the proposed MemTFTs, the gate stack is composed of serially connected ferroelectric [P(VDF–TrFE)] and insulator (Al_2O_3) capacitors. The total induced charge density (Q) can be expressed by $Q = Q_F = Q_O = C_O(V_w - V_F)$, where Q_F and Q_O are the corresponding induced charge densities across the ferroelectric [P(VDF–TrFE)] and Al_2O_3 capacitors. Therefore, a load line formed by the Al_2O_3 capacitor is described in the V_F axis by the straight line plotted in the second and fourth quadrants in figure 4(a). This explanation can be applied only for the voltage range of the positive side (accumulation side of the ZnO channel). We have to note that the employed thickness of ZnO is so small that the channel can be fully depleted. As a result, it remains an insulating layer at the *off* state, because the inversion carriers are very difficult to form for ZnO unlike the case of Si. For this case, C_O is given by the geometric average of C_{ox} (for the Al_2O_3 capacitor) and C_{dep} (for the depletion capacitor of ZnO). For this reason, the slope of the resultant load line has different values between the positive and negative sides in the voltage axis. Because the operating points at each programming event are determined by the interceptions of ferroelectric Q-V_F hysteresis and the load line, as schematically shown in figure 4(a), the MemTFT employing the oxide semiconductor as an active channel has a feature that different voltage levels are required to completely program both *on* and *off* states. Therefore, we cannot minimize the programming voltage for the *off* state only with the reduction of Al_2O_3 thickness. $V_{W,on}$ and $V_{W,off}$ of the MemTFTs can be estimated by the following equations:

$$V_{W,on} = \frac{P_s \cdot d_{ox}}{\epsilon_0 \cdot \epsilon_{ox}} + V_{F,sat}, \tag{1}$$

$$V_{W,off} = \frac{P_s}{C_{ox}}\left(1 + \frac{\epsilon_{ox} \cdot d_s}{\epsilon_s \cdot d_{ox}}\right) + V_{F,sat}, \quad \text{where } C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{ox}}{d_{ox}}, \tag{2}$$

where P_s and $V_{F,sat}$ are saturated polarization charge per unit area of the ferroelectric P(VDF–TrFE) film and the corresponding applied voltage across the P(VDF–TrFE) capacitor. ϵ_{ox}, ϵ_s, d_{ox}, d_s are dielectric constants and the film thicknesses of Al_2O_3 and ZnO layers, respectively. Because the depletion width (d_{dep}) of the ZnO layer is related to the applied voltage and the carrier concentration of the ZnO channel (N_D), we can estimate the critical voltage value (V_{FD}) at which the ZnO layer is fully depleted as shown in the following equation derived from the delta-depletion analysis [21]:

$$d_{dep} = \frac{\epsilon_s}{\epsilon_{ox}} d_{ox}\sqrt{1 + \frac{V_G}{V_\delta}} - 1, \qquad \text{where } V_\delta = \frac{q}{2}\frac{\epsilon_s \cdot d_{ox}{}^2}{\epsilon_0 \cdot \epsilon_{ox}{}^2} \cdot N_D. \tag{3}$$

In equation (3), the applied voltage when d_{dep} becomes identical to d_s corresponds to the V_{FD}. If N_D and d_s are 1×10^{18} cm^{-3} and 10 nm, respectively, V_{FD} is calculated to be only

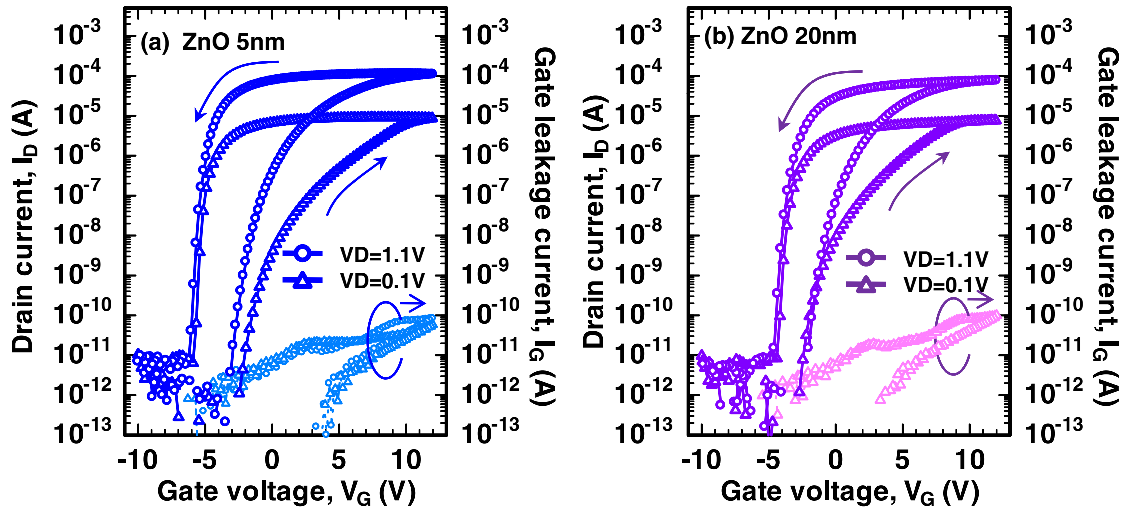

Figure 3. Sets of I_D–V_G transfer curves and gate leakage currents for the fabricated MemTFTs with the ZnO channel thicknesses of (*a*) 5 (Dev-1) and (*b*) 20 nm (Dev-2). The measurements were carried out in a double sweep mode at two V_Ds of 0.1 and 1.1 V. The hysteresis in transfer curves showed counterclockwise directions for both devices. (Color online.)

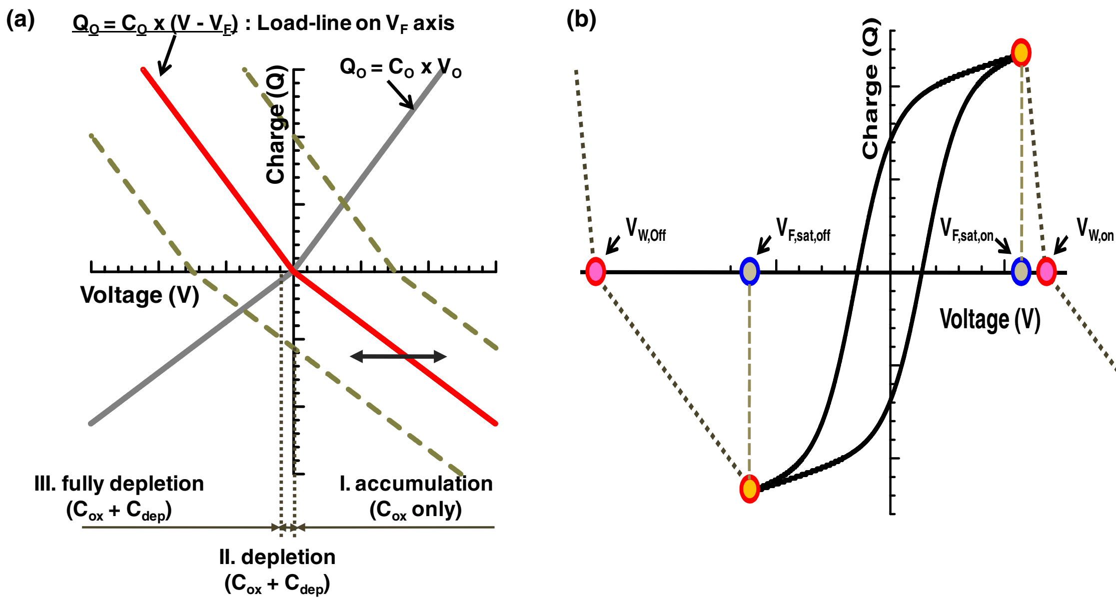

Figure 4. (*a*) Load line in Q–V plane for the determination of operating points at each programming event for the proposed MemTFT. The straight line plotted in the first and third quadrants shows the variation of total induced charge density as a function of applied voltage. Because Q_O can be expressed by $C_O \times (V - V_F)$, the load line is determined to be the straight line plotted in the second and fourth quadrants on the V_F axis and moves with the change in total applied voltage as described by the dotted lines. C_{OX} and C_{dep} correspond to the capacitance values induced in Al_2O_3 and the depletion layer of ZnO, respectively. (*b*) The programming voltages ($V_{W,on}$ and $V_{W,off}$) of the proposed MemTFT are determined by the interceptions of ferroelectric Q–V_F hysteresis and the load-line described in (*a*), in which it is assumed that $V_{F,sat,on}$ and $V_{F,sat,off}$ are applied to the ferroelectric capacitor at *on* and *off* operations, respectively. Because these plots were schematically drawn, they did not accurately reflect the quantitative information. (Color online.)

about −0.2 V. In other words, the MemTFT always operates in the fully depletion mode at the *off*-programmed state. As shown in equation (2), the increase in d_s linearly increases $V_{W,off}$. Consequently, the reduction in the film thickness of both layers of Al_2O_3 and ZnO is necessary for realizing lower voltage programming in the proposed MemTFT. The relatively small MW for Dev-2 originated from the fact that the *off* operation was not sufficiently carried out.

We can evidently confirm these effects from the programming voltage dependence on the variations of MW and V_{on} of the MemTFTs, as shown in figure 5. In these measurements, while V_G for *off* on the negative side was fixed at −10 V, V_G for *on* on the positive side was varied from 10 to 5 V. There are two differences between the two devices. The first one is that the MW of Dev-2 did not increase from V_G of 6 V any more, even though the ferroelectric polarization was not yet saturated in that voltage range. The second one is that V_{on} of the TFT was shifted in the negative direction with the evolution of repetitive measurements at various V_G sweeps, as clearly shown in the insets of figure 5. For the case

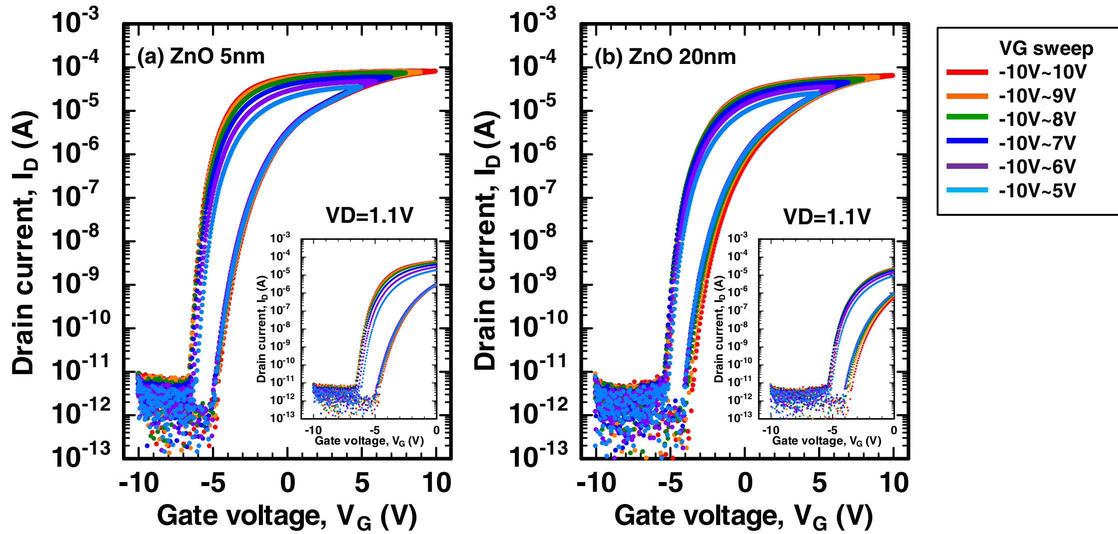

Figure 5. Variations of transfer curves of the fabricated MemTFTs with the ZnO channel thicknesses of (*a*) 5 (Dev-1) and (*b*) 20 nm (Dev-2) when the sweep range in V_G was changed, in which V_G for the *off* operation was fixed at −10 V and V_G for the *on* operation was varied from 10 to 5 V. Their behaviour is also shown in a magnified way in the insets of each figure. (Color online.)

of Dev-1, V_{on} showed no change at every sweep, which is a very desirable feature for the design of operation scheme of this MemTFTs. Considering that V_{on} of Dev-2 was initially defined to be larger than that of Dev-1, this effect could be evidently confirmed. These results are related to the fact that V_G of −10 V was not sufficient for the complete *off* operation for Dev-2, as expected in equation (2). Therefore, the oxide channel thickness for the MemTFTs should be so optimized as to realize both characteristics of low voltage operation and stable transistor behaviour.

Another stability issue related to the memory device is data retention. For the case of Dev-1, the *on*/*off* ratio for the programmed drain currents between the two memory states was initially obtained to be more than 300 when the programming voltage pulses with ±18 V and 500 ms were applied. It was also observed to be still higher than 20 after a lapse of 10^3 s and remained at 3.4 even after 10^4 s. We expected that the MemTFT employing thinner ZnO could show better retention behaviour thanks to the decrease in the depolarization field during the retention period. However, it was difficult to directly compare the retention behaviour of the MemTFTs with different ZnO thicknesses, because V_{on}s for the two TFTs have some variations. Actually, we found that the retention time for the programmed data was very sensitively dependent on the programming conditions such as pulse amplitude and duration of voltage signals as well as the gate bias conditions during the retention period. More detailed discussions on the programming characteristics and retention behaviour of the proposed MemTFT will be presented in the next publication.

In realizing this MemTFT for practical application, the control of V_{on} is also important. It is desirable that the TFT be operated in an enhancement mode and the MW be formed above 0 V in the V_G axis. Otherwise, it is very difficult to design the driving circuits for the memory array owing to the unwanted drain currents from unselected MemTFTs even at a V_G of 0 V. Post-annealing process is one of the promising methods to control V_{on} of the MemTFT, which has been normally observed

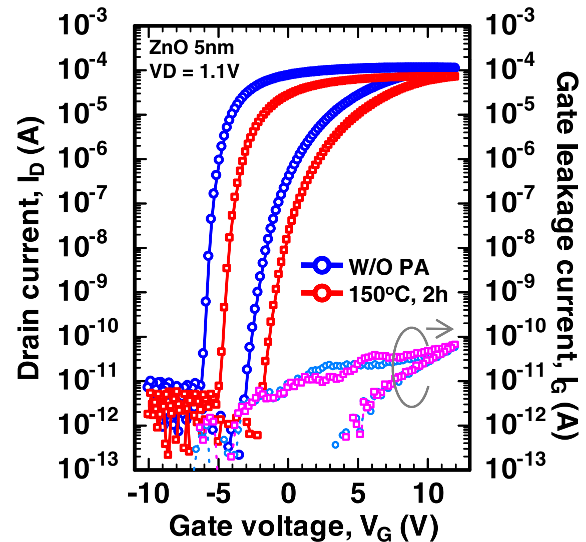

Figure 6. Comparison in I_D–V_G characteristics for the fabricated MemTFTs with the 5 nm thick ZnO channel before and after the post-heat treatment at 150 °C for 2 h in ambient N_2. (Color online.)

for the oxide TFTs [22]. V_{on} of Dev-1 was changed from −3.1 to −1.7 V when the device was annealed at 150 °C for 2 h without any marked decrease in MW and increase in I_G, as shown in figure 6. Although the annealing process at 200 °C would be more effective, there exists a limitation in temperature owing to the lower melting temperature (∼160 °C) of P(VDF–TrFE). Therefore, the obtained results imply that an additional methodology including the device structure and fabrication process should be developed. The modification of the semiconducting nature of ZnO and/or replacement by other compositions of oxide semiconductors can be possible solutions to improve this problem. From this viewpoint, the thicknesses of the inserted insulator and channel layers should be optimized for a sufficient MW as well as a suitable V_{on}. Improving the quality of P(VDF–TrFE) can be another solution

for optimizing the MW and V_{on}. A ferroelectric copolymer spin-coated and annealed in a glove box in an Ar atmosphere can improve the quality of the active channel, because the density of water molecules incorporated in the polymer thin film can be reduced [23].

4. Conclusions

In summary, we fabricated NV-MemTFTs using ZnO and P(VDF–TrFE) as a semiconducting channel and a ferroelectric gate insulator, respectively. Two important strategies were adopted for guaranteeing the good memory and transistor characteristics of the proposed NV-MemTFTs. A thin Al_2O_3 layer was confirmed to play a good role in protecting the ZnO channel and suppressing the leakage component for the relatively thin P(VDF–TrFE) layer. Furthermore, the reduction in ZnO channel thickness was very effective in decreasing $V_{W,off}$. Consequently, the MemTFTs with the gate structure of Al/80 nm P(VDF–TrFE)/4 nm Al_2O_3/5 nm ZnO showed a MW of 3.8 V at lower operation voltages ranging from −10 to 12 V, SS of about 400 mV/dec, 7-orders-of-magnitude I_{on}/I_{off} ratio and I_G as low as 10^{-11} A. Although some technical issues such as the control of V_{on} remained, it can be concluded from the encouraging results obtained that the proposed NV-MemTFT is a very promising memory component for the future flexible and transparent electronic systems.

Acknowledgments

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