Plasma-Enhanced Atomic Layer Deposition Processed SiO_2 Gate Insulating Layer for High Mobility Top-Gate Structured Oxide Thin-Film Transistors

Jong Beom Ko, Hye In Yeom, and Sang-Hee Ko Park

***Abstract*— SiO_2 processed by plasma-enhanced atomic layer deposition (PEALD) was applied as a gate insulator (GI) to the top gate high mobility InZnO (IZO) thin-film transistor (TFT). In as-fabricated devices, while IZO TFTs with GI processed by PEALD shows high ON/OFF ratio characteristics, the devices with GI deposited by plasma-enhanced chemical vapor deposition showed the conductive characteristics. From the secondary ion mass spectroscopy analysis, it is inferred that PEALD processed SiO_2 generates fewer free electron donating elements in the active layer. The IZO TFT with PEALD processed GI exhibits a high-field effect mobility of 32.9 $cm^2/V \cdot s$, V_{ON} of −0.3 V, and ΔV_{ON} of 0.56 V under positive bias temperature stress (1 MV/cm, 60 °C, 3600 s) after being subject to thermal annealing at 350 °C.**

***Index Terms*— InZnO TFT, PEALD, SiO_2, gate insulator, high mobility, hydrogen, OH.**

I. Introduction

THIN-FILM transistors (TFTs) with oxide semiconductors have drawn much attention due to their stellar performances, easy fabrication and scalability [1], [2]. For the implementation of ultra-high resolution display, TFTs with mobility of higher than 30 $cm^2/V \cdot s$ [3] and high stability are essential as well as reduction of resistance-capacitance (RC) delay, which can be realized in top gate (TG) self-aligned (SA) structure [4]. There are several concerns, though, in processing high mobility TG oxide TFTs such as metallization, threshold-voltage (V_{th}) control for short channels [5], gate insulator (GI) deposition process [6], film quality, and passivation. Among these, the GI process is most critical in controlling V_{th} and securing high stability.

The conventional plasma-enhanced chemical vapor deposition (PECVD) process should be performed at high temperature to get a high quality GI of SiO_2. High temperature processing for SiO_2 deposition on the active layer during the oxide TFT fabrication, however, induces degradation of the channel layer resulting in negative V_{th} shift of the TFT possibly due to the hydrogen (H) incorporation into the active layer [6] or generation of free carrier source on the surface of the active layer. This phenomenon becomes more serious as the mobility of the TFT increases. Meanwhile, low temperature processed SiO_2 films contain more H and in such cases, high temperature post annealing gives rise to serious negative V_{th} shift due to H diffusion into the active layer [7]. Obtaining a high quality GI without any degradation of the oxide TFT therefore is very difficult in the TG oxide TFTs with high mobility and good stability.

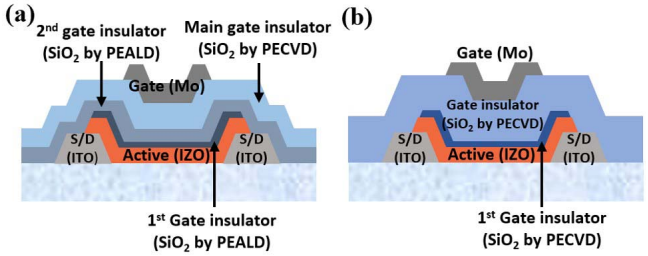

Fig. 1. Schematic diagram of top gate staggered IZO TFTs (a) with SiO_2 gate insulators deposited firstly by PEALD and then by PECVD at 300 °C and (b) with SiO_2 gate insulator deposited only by PECVD at 300 °C.

Here we investigated feasibility of SiO_2 processed by plasma-enhanced atomic layer deposition (PEALD) on the GI of TG high mobility InZnO (IZO) TFT to model the SA TFT by comparing the result from these TFTs with that from PECVD processed SiO_2 GI film. Top-gate staggered oxide TFTs have the same issues as SA TFTs as far as the deposition sequence of the active layer and GI is concerned. The results show the promise that PEALD SiO_2 could be a good GI layer for high mobility SA oxide TFTs.

II. Experiments

Two different TG staggered type IZO TFTs were fabricated with a GI of SiO_2 deposited by (a) PEALD and (b) PECVD at 300 °C. For the PEALD SiO_2, the bis-diethylamino silane (BDEAS, $H_2Si[N(C_2H_5)_2]_2$) and oxygen plasma are used as reactants. Fig. 1 shows the schematic diagram of fabricated TFTs. The main purpose of adopting a 1st GI in both TFTs is to protect the interface between the active layer and the 1st GI from the chemical exposures [8]. The use of a 2nd GI is to surround the active layer with SiO_2

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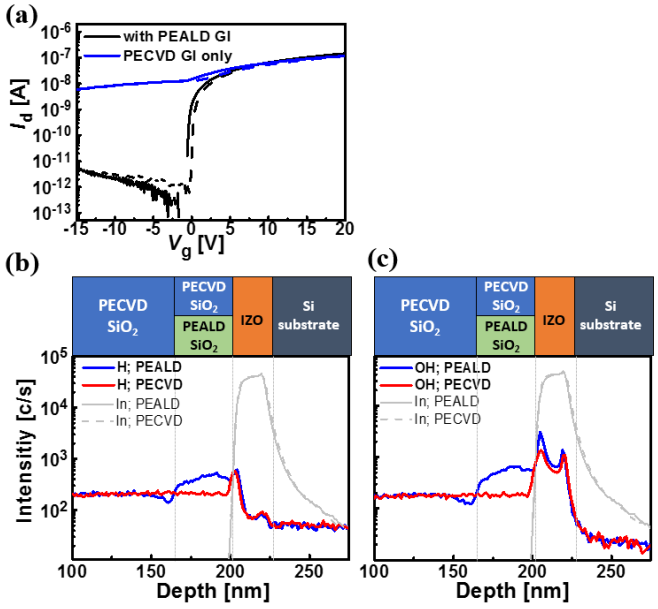

Fig. 2. (a) Transfer characteristics of as-fabricated PEALD and PECVD processed oxide TFTs. SIMS results of (b) H and (c) OH elements in as-fabricated PEALD and PECVD processed samples.

by means of PEALD so as not to expose the sides of the active layer to the main GI of SiO_2 by PECVD. 150 nm of ITO and 30 nm of IZO were sputtered for the source/drain and active layer, respectively. The thickness of first and second GI of SiO_2 deposited by PEALD (CS-KIT-1404, CN1) in (a) are 10 nm and 30 nm, respectively. The thickness of first GI of SiO_2 deposited by PECVD in (b) is 10 nm. The main GI in (a) and (b) are both deposited by PECVD and their thickness are 170 and 200 nm, respectively. The total capacitance of the GI for (a) and (b) devices are 19.8 and 19.6 nF/cm^{-2}, respectively. Finally, 150 nm of sputtered molybdenum is used for gate electrode. The devices were annealed under vacuum at 350 °C for 2 hours. The transfer and output characteristics were measured at 0.1V of drain voltage and the measured width and length of the channel were 20 μm and 160 μm, respectively. The mobility in the linear region was extracted by plotting graphs with following equation:

$$\mu = (L/W)(1/C_i V_{ds})(\Delta I_{ds}/\Delta V_g) \quad (1)$$

where W and L are channel width and length, respectively. C_i is a capacitance of insulator and V_{ds} is 0.1V. The mobility was extracted at 20V of V_g. To analyze the degree of incorporation of H and OH in real fabrication environment of the device, IZO, PEALD/PECVD (film a) and PECVD (film b) processed SiO_2 were deposited under the same stack sequences of fabricated devices and analyzed by secondary ion mass spectroscopy (SIMS).

III. Results and Discussions

Fig. 2(a) shows the transfer characteristics of two types of as-fabricated TG IZO TFTs. While TFTs with the first GI of SiO_2 deposited by PECVD did not show any on/off characteristics, that with PEALD processed SiO_2 has V_{on} and hysteresis of -0.72 V and 0.72 V, respectively, with an on/off ratio of 10^6. Mostly as-fabricated TG oxide TFTs show hysteresis owing to the plasma damage on the interface caused during the GI deposition.

The origin of increased carrier in the channel layer of virgin oxide TFT may be H incorporation, oxygen vacancy (V_o) formation, In rich phase generation in the active layer during the high power plasma process on top of the active, or light illumination from plasma exposure during the fabrication. To clarify the origin, we carried out SIMS analysis of H and OH of the films in as-fabricated multilayers which were prepared exactly the same as in the TFTs as shown in Fig. 2. Contrary to our conjecture, PECVD SiO_2/IZO films have less H than in PEALD SiO_2/IZO films at the GI but almost similar amounts of H in the active layer in spite of totally different characteristics of V_{on} of each TFT.

The detected H by SIMS can exist as various bonding states such as –OH, −H, and In-H. All the bonding states of H, however, do not always donate free electrons. It has been reported that most of the electrons from H which exist as M-OH states are compensated by excess O in the active layer resulting in relatively low free electron density [9]. According to the SIMS results in Fig. 2(b) and 2(c), PEALD SiO_2/IZO contains more increased OH in the channel layer than that of PECVD SiO_2/IZO despite similar H contents in the active layer. During the SIMS measurement, the OH molecules can be broken by primary ions with high energy and then detached into O and H. The H generated by this process can also be detected. Although the detected H profiles in both active layers are similar, those for OH in each IZO layer are different [10]. Therefore, we suspect that more oxygen could be supplied into the IZO active layer during the first GI process of PEALD and the compensation of electrons by excess O in the channel layer is dominant in PEALD processed samples.

Although high mobility SA TFTs with PECVD deposited SiO_2 GI had been reported, they showed good on/off ratio just with separated N_2O plasma treatment before the deposition of SiO_2. Furthermore, N_2O plasma treatment needs an annealing temperature higher than 350 °C to get high stability under positive bias temperature stress. To date, a detailed process has not been reported. To exclusively compare performance of TFTs in both cases of (a) and (b), we did not perform N_2O plasma treatment.

Two oxide TFTs were thermally annealed at 350 °C under vacuum and showed improved performances as shown in Fig. 3(a) and (b). In terms of the leakage current, both TFTs show reduced leakage current after annealing. This can partially be attributed to the recovery of shallow donors of ionized V_o, which are generated by light illumination during the plasma process of PEALD, PECVD and sputtering, to the original deep state of V_o [11]. There is a main difference in V_{on} of each TFT. TFTs with PEALD processed GI (a) show negligible V_{on} change of 0.4 V with removal of hysteresis. On the other hand, TFTs with PECVD only processed GI (b) show large positive V_{on} shift to give -5.8 V but still a large negative shifted value. The TFT with PEALD processed GI shows a field effect mobility of 32.9 cm^2/V·s and V_{on} of -0.3 V. The inset in Fig 3(a) shows the output characteristics. For the output characteristic, the I_{ds} was measured as a func-

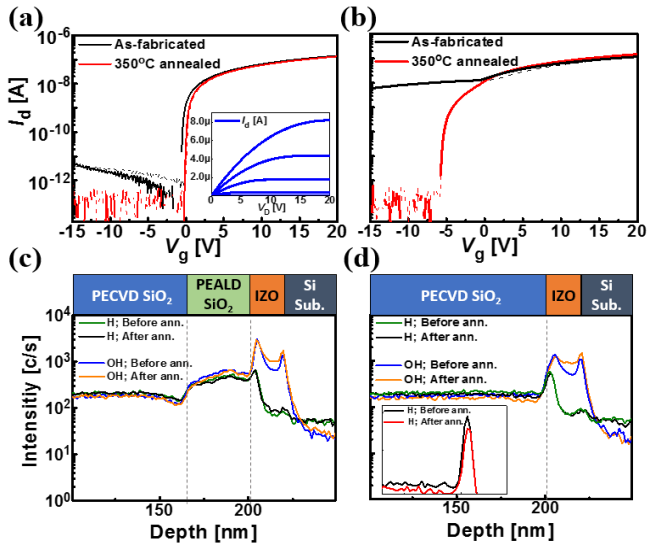

Fig. 3. Transfer curve of as-fabricated (black line) and annealed at 350°C in vacuum for 2h (red line) devices with (a) PEALD processed GI and (b) PECVD only processed GI. Inset in figure 3 (a) indicates the output characteristics. SIMS result of H and OH amount in (c) PEALD processed sample and (d) PECVD processed sample before and after thermal annealing. Inset in figure 3 (d) indicates the expansion graph of H amount in channel region.

tion of drain voltage with various V_g (0, 5, 10, 15 and 20 V) and it shows no contact issues.

To investigate the origin of the different behavior of TFTs after annealing, we compared SIMS analysis results before and after thermal annealing as shown in Fig. 3(c) and (d). H and OH peak intensities of the main GI SiO_2 deposited by PECVD in both film stacks (film a, and b) do not show large difference before and after annealing. Meanwhile, the intensities in H and OH of the first GI SiO_2 films deposited by PEALD and PECVD are slightly different after annealing. Although the intensities of H and OH in PEALD SiO_2 are much higher compared to those in PECVD SiO_2, they would not be mobile even after higher temperature annealing than the deposition temperature, yielding similar intensity before and after annealing. The thermal annealing at 350 °C seems to bring about a slight diffusion of H in the GI into the interface between the active layer and the GI, and active layer which seems to contribute to the reduction of hysteresis and S.S value of TFT by passivating defects in the interface and active layer as demonstrated in previous result [12]. H in the PECVD SiO_2 film, however, is more mobile and easily diffuses out or into the adjacent film under annealing temperature higher than the deposition temperature as shown in Fig. 3(d).

High temperature annealing under vacuum condition may cause outgassing of H from the channel layer and GI [13]. The reduction in the H amount after annealing at 350 °C in the IZO channel region of the stacked films with PECVD SiO_2 as first GI resulted in TFT with high on/off characteristic. When compared with TFTs processed by PEALD, however, it still shows negative shifted V_{on} of -5.8 V in spite of a relatively lower H intensity than that with PEALD SiO_2 GI. This makes us suspect the possibility of V_o formation or other cation disorder such as an indium rich phase during the PECVD process. Furthermore, IZO TFTs with PECVD processed first GI seem

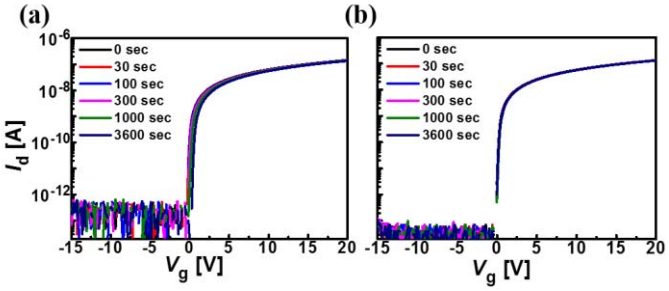

Fig. 4. Transfer curve during (a) PBTS and (b) NBTS stress as function of stress time. The stressed temperature was 60 °C and stressed gate bias were 20V and −20V, respectively.

to have more H which was not compensated by supply of oxygen source, existing in an electrically active state.

Fig. 4 shows the bias stability of IZO TFT with PEALD SiO_2 GI under gate bias stress conditions. The ΔV_{on} under the positive bias stress of 20 V (1 MV/cm) and negative bias stress of −20 V (−1 MV/cm) at 60 °C for 3600 seconds were +0.56 V and almost 0 V, respectively. Taking into account that high mobility oxide TFT would have more V_o related defects than lower mobility TFT resulting in more negative V_{th} shift under NBTS, our high mobility TG IZO TFT exhibits excellent NBTS performance. This suggest that the PEALD SiO_2 process during the fabrication of TG oxide TFT provides a good front channel interface which does not induce severe trapping of any charged states.

IV. Conclusion

High quality SiO_2 layer processed by means of PEALD was successfully applied to the high mobility TG IZO TFT as the GI. The IZO TFT shows high mobility of 32.9 $cm^2/V{\cdot}s$, V_{on} of −0.3 V, and S.S of 0.11 V/dec. with good bias stress stability after 350 °C thermal annealing. It is suggested that the TG oxide TFT with PEALD SiO_2 GI could exhibit high performance even after high temperature annealing thanks to immobile H in SiO_2 and sufficient oxygen supply to the active layer during the deposition process without generating any significant interface defects. Although PEALD needs longer time than PECVD, SiO_2 film by PEALD will be adopted just for interface formation as thin as 30 nm in real SA TFTs. The results confirmed the feasibility of applying PEALD process to the GI of high mobility SA TG structured oxide TFT.

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