Optimizing De-trap Pulses in Gate-injection Type Ferroelectric NAND Cells to Minimize Read After Write Delay Issue

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***Abstract*— The ferroelectric (FE) NAND flash, featuring metal-interlayer-FE-interlayer-silicon (MIFIS) gate stacks, leverages both charge trapping and polarization ($\triangle P$) switching to achieve a broad memory window (MW) and low operation voltage. These remarkable advancements establish it as a viable contender for future NAND flash technologies. However, the read-after-write-delay (RAWD) problem during program/erase (PGM/ERS), caused by channel-injected interface trapped charges (Q_{it}) between the FE layer and the channel interlayer (Ch.IL), leading to short-term V_{th} variations, remains unexplored in MIFIS FE-NAND cells. This letter presents the first analysis of RAWD in FE-NAND cells, including the experimental optimization of a de-trap pulse that effectively eliminates Q_{it} whereas preserving both gate-injected interface trapped charges (Q_{it}') and $\triangle P$. Consequently, the FE-NAND cell exhibits a narrow MW of 3.45 V at a delay time (t_{Delay}) of 1 μs between PGM/ERS and read operations, expending to 7.40 V at a t_{Delay} of 1 s. This variation is attributed to the generation of Q_{it} and the subsequent de-trap process, affecting channel conductivity. To thoroughly address the RAWD, various pulse widths and amplitudes are experimentally explored immediately post-PGM/ERS to optimize the de-trap pulse for selective Q_{it} removal. Upon applying the optimized de-trap pulse, the stable wide MW (7.40 V) is consistently maintained regardless of t_{Delay}. This work is meaningful as it brings attention to previously unexplored issues in next-generation ferroelectric (FE) NAND cells and suggests practical operational solutions.**

***Index Terms*— Ferroelectric NAND flash, MIFIS FeFET, Read after write delay, RAWD, De-trap pulse.**

I. Introduction

GATE-INJECTION type FE-NAND cells employing MIFIS gate structures have been extensively researched as a promising extension of traditional 3D-NAND flash technologies [1]-[6]. Fig. 1(a)-(b) demonstrate how the synergistic effects of gate-injected Q_{it}' and switched $\triangle P$ enable lower operation voltages and larger MW. However, since the MIFIS gate stack is derived from the conventional metal-FE-IL-silicon (MFIS) stack, it is still not free from the issues related to channel-injected Q_{it} [7]-[12].

During PGM/ERS operations, the Q_{it} injected from the channel between the FE layer and Ch.IL has an opposite polarity to the gate-injected Q_{it}', as well as $\triangle P$ [13]-[15]. This leads to various obstacles. Q_{it} can be categorized into two types: stable and unstable [16]. The stable Q_{it} remains trapped for more than 100 s due to its strong coupling with around 90 % of $\triangle P$ [17]. In contrast, the unstable Q_{it}, which is not linked with $\triangle P$, quickly de-traps and vanishes in less than 1 ms [18]. The properties of stable and unstable Q_{it} lead to the narrow MW and RAWD issue, respectively [19]. Fig. 1(c) shows the gradual release of unstable Q_{it} after PGM/ERS. This process affects the stability of MW and V_{th} regarding t_{Delay} between PGM/ERS and read operations [20]. Previous studies have mostly focused on improving the performance of gate-injection type FE-NAND cells, while generally neglecting the analysis of reliability or the development of solutions for RAWD [21].

This study aims to provide experimental clarification on the RAWD in FE-NAND cells, marking the first illustration of such elucidation. As shown in Fig 1(d), we have designed a de-trap pulse that specifically eliminates channel-injected Q_{it} whereas leaving gate-injected Q_{it}' and $\triangle P$ unaffected. We observed substantial variations in the MW characteristics as a function of t_{Delay}. Specifically, the MW was measured to be 3.45 V at a t_{Delay} of 1 μs and 7.40 V at 1 s. Afterwards, we investigated the effects of de-trap pulses under various conditions. Ultimately, when applying the optimal de-trap pulse, we achieved broad MW consistently, independent of t_{Delay}. However, de-trap pulses with insufficient amplitudes were unable to fully resolve the RAWD, while pulses with overly high amplitudes caused disturbance for Q_{it}' and $\triangle P$. Our research findings provide essential insights for advancing research on FE-NAND for future 3D-NAND flash technology.

II. Experimental Details and Results

The MIFIS gate stack FE-NAND cell process is as follows. A field oxide of 500 nm thick SiO_2 was grown on a P-type low-doped prime wafer. Subsequently, after defining the active region, a replacement gate was formed on the channel using photoresist. The source and drain were then formed through an

This work was supported by the TIP (RS-2023-00231985, RS-2023-00235655) and MSIT (No. RS-2023-00260527).

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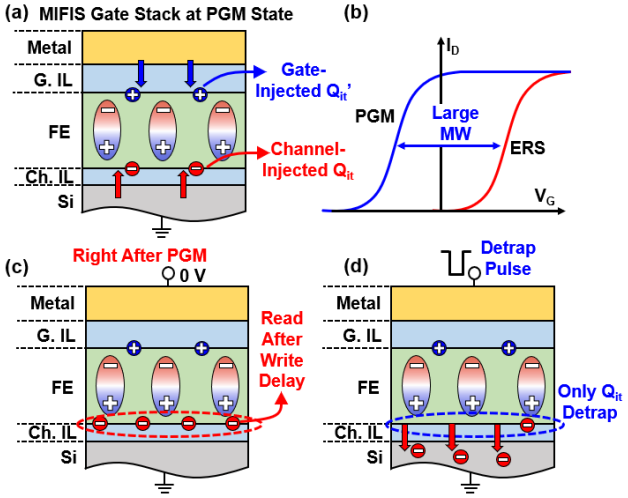

Fig. 1(a) Schematic of $\triangle P$, Q_{it}, and Q_{it}' during PGM. (b) MW expansion induced by $\triangle P$ and Q_{it}'. (c) RAWD caused by channel-injected Q_{it}. (d) Introduction of a detrap pulse to resolve RAWD.

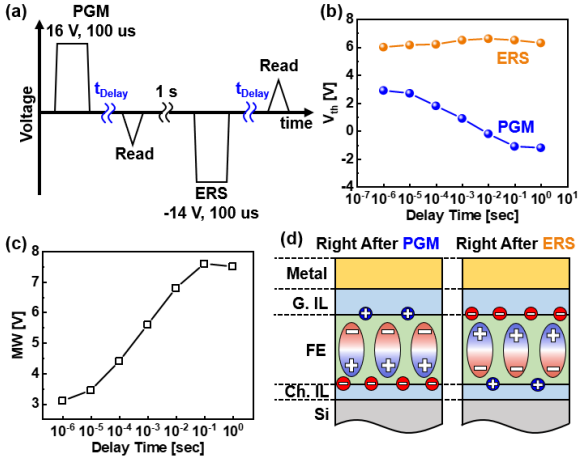

Fig. 2(a) Pulse scheme for assessing RAWD. (b) Measured V_{th} in ERS/PGM states with t_{Delay} and (c) MW. (d) Schematics for RAWD caused by Q_{it} in PGM and ERS states.

ion implantation process. After removing the replacement gate, an activation process was conducted using a rapid thermal annealing system at 1000 ℃ for 30 s. The SC-1 wet cleaning was performed to form 1.5 nm thick Ch.IL, followed by an additional RTA process (1000 ℃, 30 s). Next, an 18 nm $Hf_{0.5}Zr_{0.5}O_2$ FE layer and gate IL were formed using plasma-enhanced atomic layer deposition (PEALD). The gate IL is composed of SiO_2/SiN/SiO_2, each 2 nm-thick. Subsequently, a sputtering process was used to form the TiN electrode. Finally, an RTA process at 600 ℃ for 10 s was conducted for crystallization of FE material. For pulse I-V measurements, a pulse generator (81104-A) and a current analyzer (CX3324-A) were utilized.

III. Result and Discussion

In order to quantify the RAWD in FE-NAND cells, we employed the pulse technique depicted in Fig 2(a). The t_{Delay} was adjusted between a range of 1 μs to 1 s. In order to determine the effective MW properties, the magnitudes of the PGM and ERS pulses were adjusted to 16 V and -14 V respectively, with a duration of 100 μs. In addition, the read pulse's rising and falling times were adjusted to 100 μs in order to conduct pulse I-V measurements [15]. Fig 2(b)-(c) illustrate the V_{th} and MW with t_{Delay}. Significantly, whereas V_{th} instability is noticeable when t_{Delay} varies during PGM operations, it is insignificant during ERS operations. According to Fig 2(d), during PGM operations, the number of channel-injected electrons far exceeds that of channel-injected holes during ERS operations [22]. Specifically, during PGM, some of the channel-injected electrons are coupled with about 90 % of the $\triangle P$ to become stable Q_{it}, while the remaining electrons form unstable Q_{it}, leading to RAWD. Conversely, during ERS operations, the lesser quantity of channel-injected holes mostly compensates with $\triangle P$, resulting in stable Q_{it} behavior.

To completely resolve RAWD, it is crucial to design a de-trap pulse that can selectively remove unstable Q_{it} during PGM operations. Fig. 3(a) illustrates the pulse scheme utilized to optimize the de-trap pulse. After setting a t_{Delay} of 1 μs following the PGM/ERS operations, we applied the de-trap pulse and then conducted a read operation to assess the effect of the de-trap pulse on RAWD. Fig. 3(b) presents a contour map of the MW that includes the effects of the de-trap pulse. It should be noted that the de-trap pulse does not affect the erase states and influences only the program states (not shown here). This is because the de-trap pulse has a much smaller amplitude and width compared to the erase pulse. We observed that RAWD still occur when the amplitude and width of the de-trap pulse are relatively low (RAWD regions). In addition, the white dotted line indicates the optimal de-trap pulse conditions where an MW of 7.4 V is observed. Conversely, when the amplitude and width of the de-trap pulse are relatively high, a disturbance phenomenon is observed, resulting in an MW exceeding 7.4 V (disturb regions).

Fig. 4(a) illustrates the pulse scheme used to precisely evaluate the effects of the de-trap pulse. Following PGM/ERS operations, a de-trap pulse was applied after a 1 μs delay, and MW characteristics were observed after additional delays of 1 μs and 1 s, respectively. As seen in Fig 4(b), it is noteworthy that RAWD problems continue to exist both with and without the de-trap pulse, as illustrated in Fig 3(b). Nevertheless, while utilizing de-trap pulses (ii) and (iii), a stable MW of 7.4 V was consistently observed at both t_{Delay} intervals of 1 μs and 1 s, signifying the absence of any RAWD issues. Conversely, in the case of de-trap pulse (iv), while an MW of 7.4 V was observed

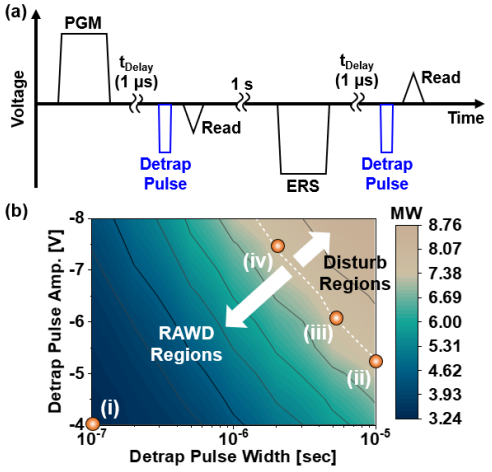

Fig. 3. Optimization of the de-trap pulse: (a) Pulse scheme for exploring the optimal de-trap pulse. (b) Contour map of the measured MW characteristics including the effects of the de-trap pulse.

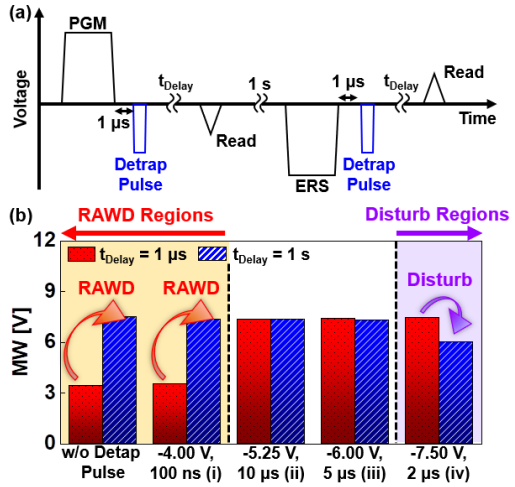

Fig. 4. Verification for effect of de-trap pulse: (a) Pulse scheme for exploring the optimal de-trap pulse and verifying its effects. (b) MW variations as a function of t_{Delay} with various de-trap pulses.

at a t_{Delay} of 1 µs, a reduced MW of 6.0 V appeared at a t_{Delay} of 1 s. This suggests that using a de-trap pulse with relatively high amplitude can induce the disturbing Q_{it}' or $\triangle P$ [3]. Detailed analysis is described in Fig. 5.

Fig. 5(a)-(b) show the schematics for scenarios when a disturb-inducing de-trap pulse with excessively high amplitude is applied to the gate electrode and after t_{Delay} of 1 s, respectively. When the the de-trap pulse (iv) is biased, disturbances occur in Q_{it}' or $\triangle P$. Concurrently, unstable Q_{it}, in other words, some electrons between the Ch.IL and FE layer are de-trapped, and channel-injected holes are generated. Although channel-injected holes during ERS operations couple with $\triangle$P to form stable Q_{it}, those generated by the de-trap pulse become unstable Q_{it} due to their opposite polarity to $\triangle P$ [23]. In more detail, as illustrated in the Fig. 5(a)-(b), the channel-injected holes generated during the biasing de-trap pulse do not couple with $\triangle P$ and are de-trapped within 1 ms. Therefore, as shown in Fig. 4 (b), immediately after applying the de-trap pulse with a t_{Delay} of 1 µs, the MW characteristic is overestimated due to channel-injected holes. However, as these holes are de-trapped within a t_{Delay} of 1 s, a smaller MW is observed due to disturbances in Q_{it}' or $\triangle P$ caused by the de-trap pulse. On the other hand, Fig. 5(c)-(d) display the schematics of the gate stack during applying de-trap pulses (i) and (ii)/(iii), respectively. De-trap pulse (i) lacks sufficient amplitude and width to effectively remove Q_{it}. In contrast, de-trap pulses (ii) and (iii) are optimized to selectively remove Q_{it} without disturbing Q_{it}' or $\triangle P$.

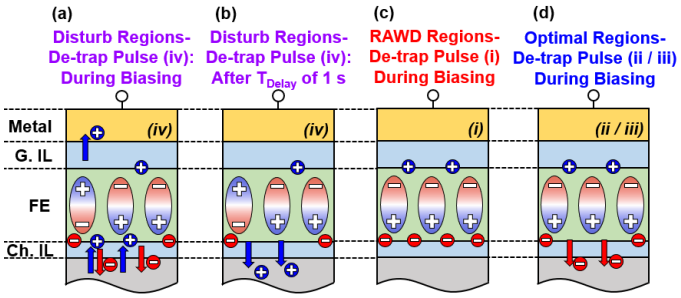

Fig. 5(a) Schematic when biasing a de-trap pulse under disturb regions conditions and (b) after a t_{Delay} of 1 s. (c) Schematic under RAWD regions and (d) optimal regions conditions.

IV. Conclusion

Our research offers a comprehensive examination of RAWD in FE NAND cells, especially focusing on the experimental refinement of a de-trap pulse that effectively removes Q_{it}, whereas maintaining gate-injected Q_{it}' and $\triangle P$. The FE NAND cell exhibited a narrow MW of 3.45 V at a t_{Delay} of 1 µs post-PGM/ERS operations, which widens to 7.4 V at a t_{Delay} of 1 s. Our analysis suggests that these changes mostly originated from the formation of channel-injected Q_{it} and the influence of its de-trapping process. Immediately following the PGM/ERS process, a thorough investigation was carried out to analyze different pulse widths and amplitudes. This was done to optimize the de-trap pulse and ensure efficient elimination of channel-injected Q_{it}. By implementing the meticulously designed de-trap pulse, a stable and amplified MW (7.4 V) was consistently obtained regardless of t_{Delay}. This study is important because it tackles crucial obstacles in the advancement of next-generation ferroelectric (FE) NAND cells and suggests efficient operational approaches.

REFERENCES

[1] J.-G. Lee *et al.*, "Memory Window Expansion for Ferroelectric FET based Multilevel NVM: Hybrid Solution with Combination of Polarization and Injected Charges," in *2022 IEEE International Memory Workshop (IMW)*, 2022: IEEE, pp. 1-4, doi: 10.1109/IMW52921.2022.9779292

[2] S. Yoon *et al.*, "QLC programmable 3D ferroelectric NAND Flash memory by memory window expansion using cell stack engineering," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023: IEEE, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185294

[3] S. Lim *et al*., "Comprehensive Design Guidelines of Gate Stack for QLC and Highly Reliable Ferroelectric VNAND," in *2023 International Electron Devices Meeting (IEDM)*, 2023: IEEE, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413820

[4] D. Das *et al.*, "Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications," in *2023 International Electron Devices Meeting (IEDM)*, 2023: IEEE, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413697

[5] M. Hellenbrand, and J. MacManus-Driscroll, "Multi-level resistive switching in hafnium-oxide-based devices for neuromorphic computing," *Nano Convergence*, vol. 10, no. 1, p. 44, 2023, doi: 10.1186/s40580-023-00392-4

[6] Z. Zhang, W. Kim, M. J. Ko, and Y. Li, "Perovskite single-crystal thin films: preparation, surface engineering, and application," *Nano Convergence*, vol. 10, no. 1, p. 23, 2023, doi: 10.1186/s40580-023-00373-7

[7] K. Ni *et al.*, "Critical role of interlayer in Hf 0.5 Zr 0.5 O 2 ferroelectric FET nonvolatile memory performance," *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2461-2469, 2018, doi: 10.1109/TED.2018.2829122

[8] S. Lee *et al*., "Design Guidelines of Hafnia Ferroelectrics and Gate-Stack for Multilevel-Cell FeFET," *IEEE Transactions on Electron Devices*, 2024, doi: 10.1109/TED.2024.3355873

[9] J. Lee *et al.*, "Role of oxygen vacancies in ferroelectric or resistive switching hafnium oxide," *Nano Convergence*, vol. 10, no. 1, p. 55, 2023, doi: 10.1186/s40580-023-00403-4

[10] N. Tasneem *et al.*, "Efficiency of ferroelectric field-effect transistors: An experimental study," *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 1568-1574, 2022, doi: 10.1109/TED.2022.3141988

[11] N. Tasneem *et al.*, "The impacts of ferroelectric and interfacial layer thicknesses on ferroelectric FET design," *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1156-1159, 2021, doi: 10.1109/LED.2021.3088388

[12] S.-H. Kuk, S.-M. Han, B.-H. Kim, S.-H. Baek, J.-H. Han, and S.-h. Kim, "Comprehensive understanding of the HZO-based n/pFeFET operation and device performance enhancement strategy," in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021: IEEE, pp. 33.6. 1-33.6. 4, doi: 10.1109/IEDM19574.2021.9720642

[13] M. Hoffmann *et al.*, "Fast read-after-write and depolarization fields in high endurance n-type ferroelectric FETs," *IEEE Electron Device Letters*, vol. 43, no. 5, pp. 717-720, 2022, doi: 10.1109/LED.2022.3163354

[14] Z. Wang *et al.*, "Standby bias improvement of read after write delay in ferroelectric field effect transistors," in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021: IEEE, pp. 19.3. 1-19.3. 4, doi: 10.1109/IEDM19574.2021.9720502

[15] N. Tasneem, Z. Wang, H. Chen, S. Yu, W. Chern, and A. Khan, "Immediate read-after-write capability in p-type ferroelectric field-effect transistors and its evolution with fatigue cycling," *IEEE Transactions on Device and Materials Reliability*, vol. 23, no. 1, pp. 142-146, 2023, doi: 10.1109/TDMR.2023.3240319

[16] K. Suzuki *et al*., "High-Endurance FeFET with Metal-Doped Interfacial Layer for Controlled Charge Trapping and Stabilized Polarization," in *2023 International Electron Devices Meeting (IEDM)*, 2023: IEEE, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413699

[17] R. Ichihara *et al.*, "Re-examination of vth window and reliability in HfO2 FeFET based on the direct extraction of spontaneous polarization and trap charge during memory operation," in *2020 IEEE Symposium on VLSI Technology*, 2020: IEEE, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265055

[18] C.-Y. Liao *et al.*, "Mechanisms of instability retention for ferroelectric field effect transistors with HfZrO2 gate stack scaling down," *Applied Physics Letters*, vol. 121, no. 25, 2022, doi: 10.1063/5.0111592

[19] Y. Higashi *et al*., "Impact of Charge Trapping and Depolarization on Data Retention Using Simultaneous P–V and I–V in HfO_2-Based Ferroelectric FET," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4391-4396, 2021, doi: 10.1109/TED.2021.3096510

[20] P. Cai *et al.*, "Deep Understanding of Reliability in Hf-based FeFET during Bipolar Pulse Cycling: Trap Profiling for Read-After-Write Delay and Memory Window Degradation," in *2022 International Electron Devices Meeting (IEDM)*, 2022: IEEE, pp. 32.2. 1-32.2. 4, doi: 10.1109/IEDM45625.2022.10019441

[21] E. J. Shin, G. Lee, S. Kim, J. H. Chu, and B. J. Cho, "Dual-Mechanism Memory Combining Charge Trapping and Polarization Switching for Wide Memory Window Flash Cell," *IEEE Electron Device Letters*, 2023, doi: 10.1109/LED.2023.3282366

[22] S.-H. Kuk, S.-M. Han, B. H. Kim, S.-H. Baek, J.-H. Han, and S.-H. Kim, "An investigation of HZO-based n/p-FeFET operation mechanism and improved device performance by the electron detrapping mode," *IEEE Transactions on Electron Devices*, vol. 69, no. 4, pp. 2080-2087, 2022, doi: 10.1109/TED.2022.3154687

[23] S.-H. Kuk, J.-H. Han, B. H. Kim, J. Kim, and S.-H. Kim, "Proposal of P-Channel FE NAND with High Drain Current and Feasible Disturbance for Next Generation 3D NAND," in *2023 IEEE International Memory Workshop (IMW)*, 2023: IEEE, pp. 1-4, doi: 10.1109/IMW56887.2023.10145967