High-Performance Al–Sn–Zn–In–O Thin-Film Transistors: Impact of Passivation Layer on Device Stability

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***Abstract*—We fabricated high-performance thin-film transistors (TFTs) with an amorphous-Al–Sn–Zn–In–O (a-AT-ZIO) channel deposited by cosputtering using a dual Al–Zn–O and In–Sn–O target. The fabricated AT-ZIO TFTs, which feature a bottom-gate and bottom-contact configuration, exhibited a high field-effect mobility of 31.9 $cm^2/V \cdot s$, an excellent subthreshold gate swing of 0.07 V/decade, and a high $I_{on/off}$ ratio of $> 10^9$, even below the process temperature of 250 °C. In addition, we demonstrated that the temperature and bias-induced stability of the bottom-gate TFT structure can significantly be improved by adopting a suitable passivation layer of atomic-layer-deposition-derived Al_2O_3 thin film.**

***Index Terms*—Amorphous semiconductor, multicomponent oxide semiconductor, passivation, sputtering, stability, thin-film transistors (TFTs).**

I. Introduction

IN RECENT years, ZnO-based oxide thin-film transistors (TFTs) have received much attention as a possible alternative to amorphous-Si or/and polycrystalline-Si TFTs in applications such as active-matrix liquid crystal displays (AMLCDs), organic light-emitting diodes (OLEDs), and flexible electronics. Major progress in oxide TFTs has been driven by improvements in field-effect mobility (μ_{FE}) or by demonstrations of AMOLED or AMLCD prototypes via device integration. In particular, the development of high-mobility ZnO-based channel materials has been proven invaluable; thus, there have been many reports of high-performance TFTs with oxide semiconductor channels such as ZnO [1], [2], InZnO [3], [4], ZnSnO [5], [6], and InGaZnO [7]–[10]. However, with a viewpoint of low-voltage driving, improvements in subthreshold gate swing (SS) and μ_{FE} are still needed to meet the requirements of integrated peripheral circuits on glass substrate. Furthermore, little is known regarding the mechanism of bias-induced threshold-voltage (V_{th}) instability in oxide TFTs, which is one of the crucial problems to be resolved before the implementation of oxide TFTs into commercial products.

In this letter, we present an Al–Sn–Zn–In–O (AT-ZIO) TFT with a high μ_{FE} value of 32.4 $cm^2/V \cdot s$ and an excellent SS value of 0.07 V/decade. Moreover, we show that direct-current-or/and temperature-induced device stability can significantly be improved by adopting an Al_2O_3 thin film as a passivation layer on the oxide channel.

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II. Experimental Introduction

A 185-nm-thick Al_2O_3 film as a gate dielectric layer was deposited by atomic layer deposition (ALD) at a substrate temperature of 150 °C on a patterned ITO (150-nm-thick)/glass substrate with a surface area of 100×100 mm^2. The ITO source/drain electrode was deposited using a conventional sputtering method and was patterned using photolithography and wet etching. An a-AT-ZIO film with a thickness of 25 nm was grown by cosputtering an Al_2O_3–ZnO (Al_2O_3, 2 wt%) target and an ITO target, followed by photolithography and wet etching (device A). Thus, the fabricated TFTs have a bottom-gate and bottom-contact configuration. For comparison, ALD-derived Al_2O_3 (40-nm-thick) films were deposited as a passivation (or protective) layer on the AT-ZIO/Al_2O_3/ITO/glass substrate after active channel patterning (device B). The fabrication procedure of the AT-ZIO transistor was previously reported in detail [11]. The maximum temperature process during device fabrication was due to thermal annealing at 250 °C. Electrical measurements were performed at room temperature in air using an Agilent B1500A precision semiconductor parameter analyzer.

III. Results and Discussion

Fig. 1(a) and (b) shows the transfer characteristics of the unpassivated (device A) and passivated (device B) AT-ZIO TFTs with $W/L = 40$ μm/20 μm, respectively. The value of μ_{FE} was calculated from the maximum transconductance ($\mu_{FE} = Lg_m/WC_iV_{DS}$, where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively). The

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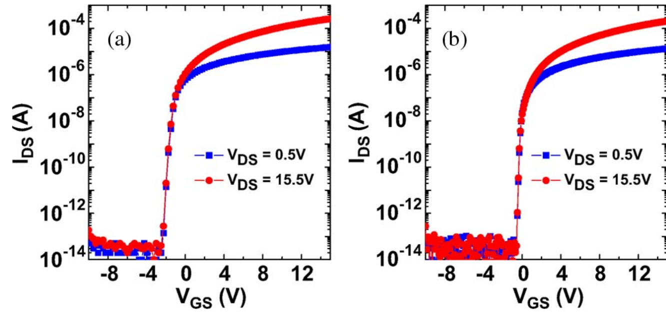

Fig. 1. Transfer characteristics of AT-ZIO TFTs with a bottom-gate and bottom-contact structure $(W/L = 40/20\ \mu\text{m})$. (a) Unpassivated device (device A). (b) Passivated device (device B).

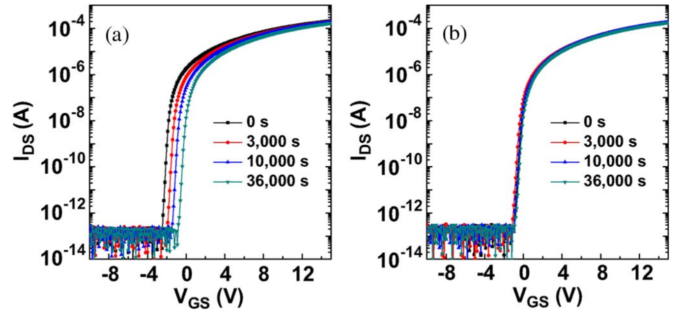

Fig. 3. Evolution of transfer curves as a function of applied stress time for (a) device A and (b) device B.

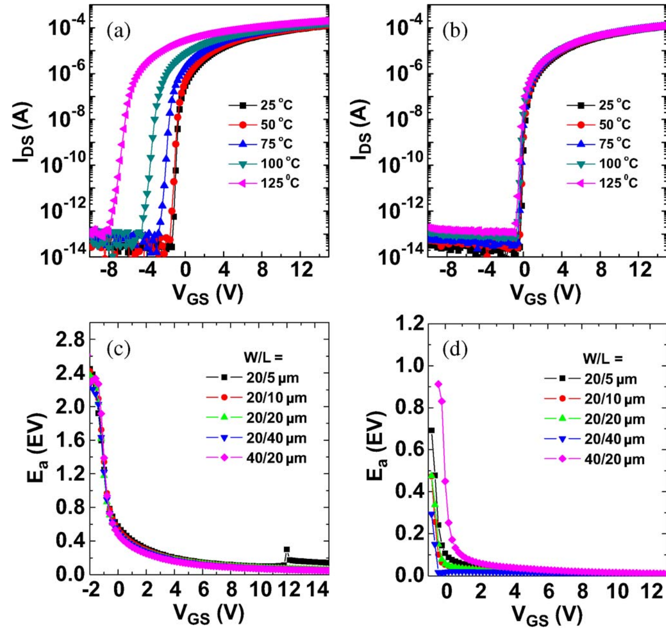

Fig. 2. Evolution of transfer curves as a function of measurement temperature. (a) Device A. (b) Device B. Variations of activation energy (E_A) of the I_{DS}-versus-V_{GS} curves for (c) device A and (d) device B.

threshold voltage (V_{th}) was determined by adjusting the gate voltage, which induces a drain current of $L/W \times 10$ nA at a V_{DS} of 15.5 V. In addition, SS $[= dV_{\text{GS}}/d\log I_{\text{DS}}$ (V/decade)$]$ was extracted from the linear portion of the $\log(I_{\text{DS}})$-versus-V_{GS} plot. Device A exhibited a μ_{FE} of 32.4 $\text{cm}^2/\text{V}\cdot\text{s}$, an SS value of 0.13 V/decade, a V_{th} of -1.5 V, and an $I_{\text{on/off}}$ ratio of 2×10^9. On the other hand, a significantly improved performance was observed for device B. The values of SS and V_{th} were enhanced to 0.07 V/decade and -0.2 V, respectively, while similar values of μ_{FE} (31.9 $\text{cm}^2/\text{V}\cdot\text{s}$) and $I_{\text{on/off}}$ ratio (2×10^9) were observed. Thus, it is tentatively believed that the role of the passivation layer is to annihilate the ambient molecule-related deep states on the bare channel layer, which would result in the reduced channel bulk trap density of device B.

Fig. 2(a) and (b) shows the evolution of the transfer curves of devices A and B, respectively. As the measurement temperature increased from 25 °C to 125 °C, the value of V_{th} shifted negatively for both devices. However, while a very large negative V_{th} shift of 5.46 V was observed for device A after heating up to 125 °C, device B showed a much smaller V_{th} shift of 0.46 V. We believe that the inferior temperature instability of device A came from the interaction between the bare channel and the ambient atmosphere (e.g., oxygen or water) [12]. Presumably, the dynamically adsorbed oxygen concentration on the bare AT-ZIO channel could decrease at a higher temperature, leading to the additional negative V_{th} shift compared to that of device B.

The increase in subthreshold current with increasing measurement temperature in AT-ZIO TFTs, as shown in Fig. 2(a) and (b), can be explained by the thermally activated Arrhenius model that has been applied to amorphous- and polycrystalline-Si TFTs [13]–[16]. In this model, the conductance activation energy (E_A) can be calculated as a function of V_{GS} in the forbidden band gap from the fitting of the temperature-dependent log (I_{DS})-versus-$1/T$ curve, where $E_A = E_C - E_F$ assuming Boltzmann statistics. Fig. 2(c) and (d) shows E_A $(= E_C - E_F)$ as a function of voltage V_{GS} for devices A and B, respectively. It can be shown that the rate of change (0.41 ± 0.05 eV/V) of E_A with respect to V_{GS} for device A is much smaller than that (0.91 ± 0.16 eV/V) for device B, indicating that the gate-voltage efficiency for device B is superior to that for device A. Here, the value of $(|\Delta E_A/\Delta V_{\text{GS}}|)$ denotes the average slope between two points with maximum activation energy $(E_{A,\max})$ and 0.2 eV (arbitrarily chosen), as shown in Fig. 2(c) and (d). This means that device B has a reduced total trap density, including the density of states of the bulk channel layer and the interfacial trap density of the back channel, leading to a faster moving E_F level with respect to V_{GS}. This interpretation is corroborated by the fact that the SS value for device B (0.07 V/decade) was smaller than that for device A (0.15 V/decade). Furthermore, the temperature-induced V_{th} instability can be improved by reducing the total trap density. Interestingly, the value of $E_{a,\max}$ for device A (2.2–2.6 eV) was larger than the value of $E_{a,\max}$ for device B (0.5–0.9 eV). The origin is not obvious at this time. The higher $E_{A,\max}$ for device A may be attributed to the contribution of thermal desorption of oxygen molecules on the bare channel.

Finally, we investigated the effect of the passivation material on the bias stability of the resulting AT-ZIO TFTs. The device was stressed under the following conditions: V_{GS} was set to 20 V at room temperature, and the stress duration was 36 000 s. Fig. 3(a) and (b) shows the evolution of the transfer curve as a function of the applied stress time for devices A and B,

respectively. For both devices, a parallel V_{th} shift to a higher voltage with increasing stress time occurred without significant change in the value of μ_{FE}, SS, and $I_{\mathrm{on/off}}$ ratio. Although V_{th} for device A shifted by approximately 1.8 V from -1.5 to 0.3 V, the positive V_{th} shift in device B was much smaller (~0.2 V) after a stress duration of 36 000 s. The superior V_{th} stability for device B is also explained by prevention of the ambient effect, which is in good agreement with the results reported for InGaZnO TFTs [12]. It should be noted that these results, including temperature and gate-bias stability, cannot be accounted for by charge trapping or the injection model, which has frequently been attributed to the origin of V_{th} instability in oxide TFTs [17]–[19].

IV. Conclusion

High-performance AT-ZIO TFTs with bottom-gate and bottom-contact configuration were fabricated below the process temperature of 250 °C and exhibited a high μ_{FE} value of 31.9 $\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$, an excellent SS value of 0.07 V/decade, and a high $I_{\mathrm{on/off}}$ ratio of 2×10^9. Furthermore, we concluded that the temperature and bias-induced stability of the bottom gate TFT structure can significantly be improved by adopting a suitable passivation layer of ALD-derived Al_2O_3 thin film. This suggests that the origin of the observed V_{th} shift in the oxide TFT cannot be attributed to charge trapping only at the channel layer/gate dielectric layer or to the charge injection into the underlying gate dielectric layer.

References

[1] E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, “Fully transparent ZnO thin-film transistor produced at room temperature,” *Adv. Mater.*, vol. 17, no. 5, pp. 590–594, Mar. 2005.

[2] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. K. Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee, and H. Y. Chu, “Light effects on the bias stability of transparent ZnO thin film transistors,” *ETRI J.*, vol. 31, no. 1, pp. 62–64, Feb. 2009.

[3] Y.-L. Wang, F. Ren, W. Lim, D. P. Norton, S. J. Pearton, I. I. Kravchenko, and J. M. Zavada, “Room temperature deposited indium zinc oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 90, no. 23, p. 232 103, Jun. 2007.

[4] B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine, “High-mobility amorphous In2O3-10 wt% ZnO thin film transistors,” *Appl. Phys. Lett.*, vol. 89, no. 6, p. 062103, Aug. 2006.

[5] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, “High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer,” *Appl. Phys. Lett.*, vol. 86, no. 1, p. 013503, Jan. 2005.

[6] W. B. Jackson, R. L. Hoffman, and G. S. Herman, “High-performance flexible zinc tin oxide field-effect transistors,” *Appl. Phys. Lett.*, vol. 87, no. 19, p. 193 503, Nov. 2005.

[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[8] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, “High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering,” *Appl. Phys. Lett.*, vol. 89, no. 11, p. 112 123, Sep. 2006.

[9] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K. Jeong, Y. G. Mo, and H. D. Kim, “High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper,” *Appl. Phys. Lett.*, vol. 90, no. 21, p. 212 114, May 2007.

[10] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo, and H. D. Kim, “High performance thin film transistors with cosputtered amorphous indium gallium zinc oxide channel,” *Appl. Phys. Lett.*, vol. 91, no. 11, p. 113 505, Sep. 2007.

[11] D.-H. Cho, S. Yang, C. Byun, J. Shin, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, S. M. Chung, W.-S. Cheong, S. M. Yoon, and H.-Y. Chu, “Transparent Al–Zn–Sn–O thin film transistors prepared at low temperature,” *Appl. Phys. Lett.*, vol. 93, no. 14, p. 142 111, Oct. 2008.

[12] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, “Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistor,” *Appl. Phys. Lett.*, vol. 93, no. 12, p. 123 508, Sep. 2008.

[13] H. C. Slade, M. S. Shur, S. C. Deane, and M. Hack, “Below threshold conduction in a-Si:H thin film transistors with and without a silicon nitride passivating layer,” *Appl. Phys. Lett.*, vol. 69, no. 17, pp. 2560–2562, Oct. 1996.

[14] L. Pichon, A. Mercha, R. Carin, O. Bonnaud, T. Mohammed-Brahim, Y. Helen, and R. Rogel, “Analysis of the activation energy of the subthreshold current in laser- and solid-phase-crystallized polycrystalline silicon thin-film transistors,” *Appl. Phys. Lett.*, vol. 77, no. 4, pp. 576–578, Jul. 2000.

[15] H. C. Slade and M. S. Shur, “Analysis of bias stress on unpassivated hydrogenated amorphous silicon thin-film transistor,” *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1548–1553, Jul. 1998.

[16] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, “SPICE models for amorphous silicon and polysilicon thin film transistors,” *J. Electrochem. Soc.*, vol. 144, no. 8, pp. 2833–2839, Aug. 1997.

[17] R. B. M. Cross and M. M. De Souza, “Investigating the stability of zinc oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 89, no. 26, p. 263 513, Dec. 2006.

[18] P. Gorrn, P. Holzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, “Stability of transparent zinc tin oxide transistors under bias stress,” *Appl. Phys. Lett.*, vol. 90, no. 6, p. 063502, Feb. 2007.

[19] Y. Vygranenko, K. Wang, and A. Nathan, “Stable indium oxide thin-film transistors with fast threshold voltage recovery,” *Appl. Phys. Lett.*, vol. 91, no. 26, p. 263 508, Dec. 2007.