Oxide Semiconductor-Based Organic/Inorganic Hybrid Dual-Gate Nonvolatile Memory Thin-Film Transistor

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***Abstract*—An organic/inorganic hybrid dual-gate (DG) nonvolatile memory thin-film transistor (M-TFT) was proposed as a device with high potential for implementing large-area electronics on flexible and/or transparent substrates. The active channel and bottom and top gate insulators (GIs) of the M-TFT were composed of In–Ga–Zn–O, Al_2O_3, and poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)], respectively. It was confirmed that the fabricated DG M-TFT showed excellent device characteristics, in which the obtained field-effect mobility, subthreshold swing, and *on/off* ratio were approximately 32.1 $cm^2\ V^{-1}s^{-1}$, 0.13 V/dec, and 10^8, respectively. It was also successfully demonstrated that the DG configuration for the proposed M-TFT could effectively work for improving the device controllability by individually controlling the bias conditions of the top gate and bottom gate (BG). The turn-on voltage could be dynamically modulated and controlled when an appropriate fixed negative voltage was applied to the BG. The required duration of the programming pulse to obtain a memory margin of more than 10 could be reduced to 100 μs. These results correspond to the first demonstration of a hybrid-type DG M-TFT using a ferroelectric copolymer GI/oxide semiconducting active channel structure and demonstrate the feasibility of a promising memory device embeddable in a large-area electronic system.**

***Index Terms*—Dual gate (DG), ferroelectric P(VDF-TrFE), In–Ga–Zn–O (IGZO), nonvolatile memory, oxide semiconductor, thin-film transistor (TFT).**

I. Introduction

A NONVOLATILE memory device is one of the most important elements for realizing future highly functional large-area electronic systems [1], [2]. Various types of devices have been proposed and demonstrated to have features such as transparency to visible light [3]–[5] and mechanical flexibility [6]–[8]. Among them, thin-film transistors (TFTs) employing a ferroelectric copolymer gate insulator (GI) are potential candidates because of their clear operation principle, simple process, and low-temperature compatibility [9]–[11]. However, in order to actually utilize this memory TFT (M-TFT) for specific applications, suitable strategies to cope with the present technical problems should be provided. Device performances could be drastically improved by replacing the conventional organic channel layer with an oxide semiconducting channel [12]–[14].

The remaining two critical drawbacks of these kinds of M-TFTs are their depletion-mode operation (negative turn-on voltage) and slow programming speed. When we employed the oxide semiconductor as an active channel for a TFT, the turn-on voltage ($V_{\rm on}$) was typically found to be below 0 V of the gate voltage (V_G). On the other hand, it is desirable to operate the M-TFT in enhancement mode (positive $V_{\rm on}$), because it would be very difficult to design peripheral driving circuitry for the memory array because of the unwanted current components from the unselected cell even at a V_G of 0 V. Although a postannealing process might be a good method to shift the $V_{\rm on}$ of the oxide TFT to the positive direction, the annealing temperature is severely limited to below the melting point of the employed polymeric ferroelectric GI [15]. The appropriate control of $V_{\rm on}$ is also required to ensure both low power operation and stable memory retention behavior. The programming speed of the proposed M-TFT must also be enhanced to a practical level. In many studies, the programming events for a ferroelectric-driven M-TFT have been examined by applying voltage pulses longer than 1 s [14], [16]–[18] or by sweeping the dc voltages [19]. Although some publications have reported relatively short switching times for poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)]-based M-TFTs in a range of 50 μs to 40 ms [9], [10], [20], even these values are considerably longer than those obtained for P(VDF-TrFE) capacitors sandwiched by top and bottom electrodes [21]–[23]. These long switching times for the M-TFT can be explained by combining the following two factors: 1) the formation of a fully depletion layer in the semiconducting channel [24] and 2) the RC time constant generated by the product of the channel resistance R and gate capacitance C [20], [25]. We must also note that the switching time for the polarization reversal of P(VDF-TrFE) thin film is very sensitively dependent on the amplitude of the electric field across the film [22]–[24], [26], [27]. For the case of an

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ultrathin P(VDF-TrFE) capacitor, the fastest observed switching time of 25 ns at a higher electric field of 8.4 MV/cm was reported by Nakajima *et al.* [28]. This strong dependence of the programming speed of M-TFTs on the programming electric field was apparently observed, irrespective of the active channel types of organic or oxide semiconductor thin films. Because the switching time is known to exponentially decay with $1/E$ [24], where E is the electric field applied across the ferroelectric film, a slight reduction in the amplitude of the programming voltage may markedly impede the switching events. Finally, it is very difficult to simultaneously optimize both important issues of lower voltage and higher speed operations for the M-TFT with a conventional single-gate device structure.

In this paper, we propose a dual-gate (DG) configuration for this M-TFT as a suitable solution to the aforementioned issues. For oxide-based TFTs, DG approaches have been tried to improve the device performances, including current drivability and subthreshold swing (SS), with the goal of low-power and high-performance device applications [29]–[32]. Control of the threshold voltage [33], [34] and improvement in device stability [35] for a TFT were also demonstrated for a DG TFT using an oxide channel such as ZnO or In-Ga-Zn-O (IGZO). Similarly, because we can simultaneously or individually bias the top gate (TG) and bottom gate (BG) of a DG M-TFT, control of the BG bias can be expected to remarkably influence the surface potential and/or field distribution of the oxide active channel. We fabricated a DG M-TFT and verified improved performances in both V_{on} controllability and programming speed. This is the first demonstration of the employment of a DG configuration for the proposed M-TFT exploiting the ferroelectric field effect.

II. Device Structure and Fabrication

The proposed DG M-TFT was designed as schematically shown in Fig. 1(a). A 10-nm-thick layer of In–Ga–Zn–O (IGZO), which is a typical amorphous oxide semiconductor [36], was chosen as an active channel layer. The bottom GI (BGI) and top GI (TGI) were composed of Al_2O_3 (70 nm) and P(VDF-TrFE) (120 nm), which have been mainly employed as a typical ferroelectric copolymer, respectively. Although, in this structure, for convenience, Al and indium-tin oxide (ITO) were used as the TG and BG electrodes, respectively, the use of ITO is also available for the TG electrodes for a fully transparent DG-structured memory device. The detailed fabrication procedures and process conditions are shown in Fig. 2. For the first step, the BG electrode of ITO was formed using a 150-nm-thick ITO-coated glass substrate. The BGI of Al_2O_3 was deposited by an atomic layer deposition (ALD) method using an Al precursor of trimethylaluminum and water vapor at 200 °C and patterned to obtain an electrical contact with the BG pad. After the source/drain (S/D) electrodes were formed on the BGI layer, the common active channel of oxide semiconductor, IGZO, and the protection layer (PL) of Al_2O_3 were successively prepared using the radio-frequency magnetron sputtering and ALD methods, respectively. The introduction of this thin PL of 9-nm-thick Al_2O_3 between the IGZO and P(VDF-TrFE) was one of the important features of the proposed DG M-TFT. The PL was confirmed to play an effective role in protecting the oxide active

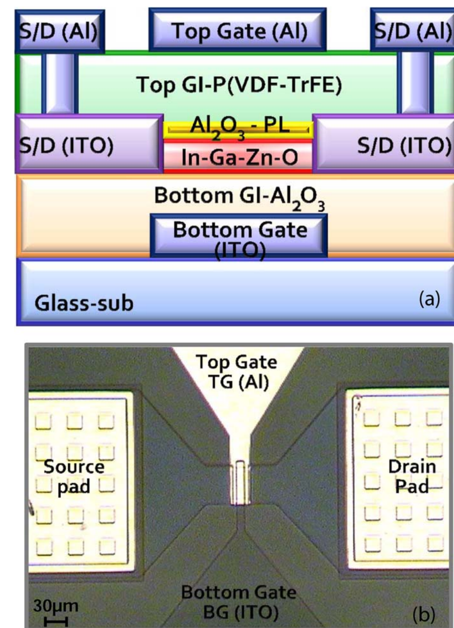

Fig. 1. (a) Cross-sectional schematic diagram and (b) microscopic image of the proposed and fabricated M-TFT with DG configuration. The gate width W and length L of the TFT shown in (b) were 40 and 20 μm, respectively.

channel during the follow-up lithography process and enhancing the device performances of the TFT [37]. It can also be available for maintaining the surface nature of the IGZO during the spin-coating and plasma-etching processes for the P(VDF-TrFE) layer. The PL and active layers were simultaneously patterned into the channel region by wet chemical etching using a dilute hydrofluoric acid solution. Here, a thermal annealing process was specially designed to be performed at 250 °C for 2 h in an air ambient, which was very important for guaranteeing sound transistor behaviors from the oxide TFT. This process is generally planned for the last step of the conventional device fabrication. However, because the melting temperature of P(VDF-TrFE) is known to be approximately 155 °C [38], we could not perform the final thermal annealing after defining the TGI layer. The TGI of P(VDF-TrFE) was formed by a spin-coating method using a 3.5 wt% dilute solution of P(VDF-TrFE) powder source (Solvay Solexis, Solef) in dimethylformamide, in which a co-polymerization ratio of 70/30 mol% was chosen for the VDF and TrFE. The prepared P(VDF-TrFE) film was crystallized at 140 °C for 1 h in an air ambient. Then, the given areas of the TGI layer were removed in order to form via holes for S/D contacts by using O_2 plasma with a dry etching system. Finally, the TG electrode of Al was deposited using the thermal evaporation method on the photoresist layer previously patterned for the lift-off process. The employment of the lift-off process for the patterning of the TG electrode and pads is related to the fact that the acid-based wet etchant may permeate through the P(VDF-TrFE) layer and damage the IGZO channel area. This phenomenon was sometimes observed for M-TFTs using a P(VDF-TrFE) GI and eventually acts as a bad influence on the TFT stability. A microscopic photo image of the fabricated DG M-TFT is shown in Fig. 1(b). Using the proposed fabrication procedures designed for the DG M-TFT,

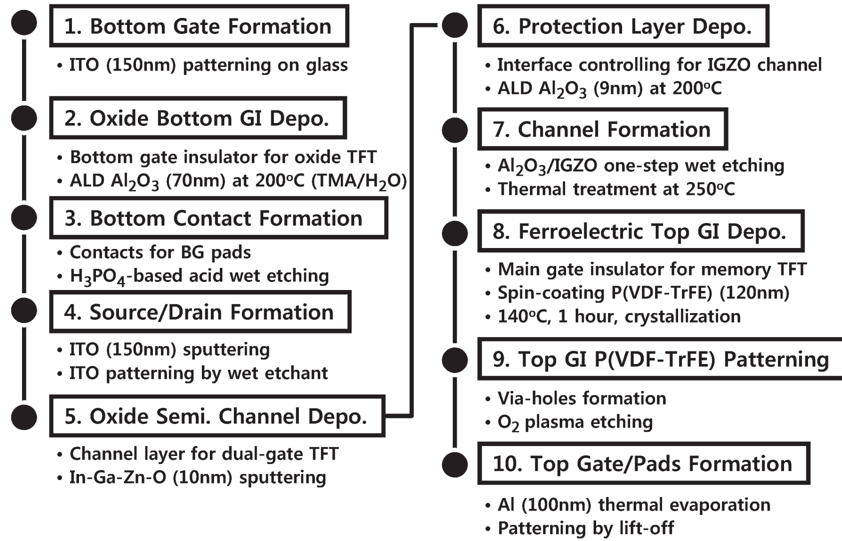

Fig. 2. Flowchart of the full fabrication procedures for the proposed DG M-TFT, in which the process steps were designed to use six photomasks. All processes were performed below 250 °C.

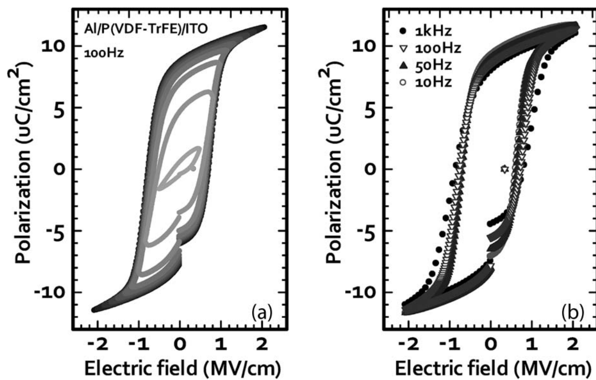

Fig. 3. (a) Polarization-electric field (P–E) characteristics of the Al/120-nm-thick P (VDF-TrFE)/ITO capacitors at a signal frequency of 100 Hz. The electric field was varied from 0.5 to 2.1 MV/cm. (b) Signal frequency dependence on the P–E hysteresis curve. The capacitor size was 50×50 μm^2.

we could also integrate the memory device with peripheral driving circuitry composed of oxide TFTs.

III. Results and Discussions

First, the basic ferroelectric properties of the Al/P(VDF-TrFE)/ITO capacitors fabricated on the same substrate were electrically examined. Fig. 3(a) shows the polarization-electric field (P–E) characteristics of a 50×50 μm^2 ferroelectric capacitor at a signal frequency of 100 Hz. The applied electric field was varied from 0.5 to 2.1 MV/cm. The remnant polarization (P_r) and coercive field (E_c) were estimated to be approximately 8.6 μC/cm^2 and 740 kV/cm, respectively. The polarization saturation with an increase in the electric field was observed to be sufficiently good. The signal frequency dependence of the ferroelectric polarization reversal was also investigated by varying the measuring frequency from 10 Hz to 1 kHz, as shown in Fig. 3(b). With the increase in the signal frequency, the E_c at the same applied field increased, and the squareness of the hysteresis was somewhat degraded. This is closely related to the dynamic switching time for the ferroelectric polarization. These obtained results reflect the general trends of metal–P(VDF-TrFE)–metal capacitors and indicate that the P(VDF-TrFE) thin film showed good ferroelectric characteristics, even after the full fabrication procedures were terminated.

Fig. 4(a) and (b) shows the drain-current–gate-voltage (I_D–V_G) transfer characteristics of the BG oxide TFT and TG M-TFT, respectively, which were individually fabricated using the DG M-TFT. All of the measurements were performed using a double sweep mode in the forward and reverse directions of V_G. The gate width/length (W/L) values of the evaluated TFTs were 40/20 μm. The BG oxide TFT was confirmed to have good performances such as a high field-effect mobility (saturation regime at a V_D of 15.5 V) of 13.7 cm^2 V^{-1}s^{-1} and a low SS of 0.24 V/dec. The gate leakage current (I_G) and TFT OFF-current were confirmed to be as low as approximately 10^{-13} A. The I_D hysteresis caused by an undesirable charge trapping/detrapping process was completely negligible, even though the turn-on voltage ($V_{\rm on}$) was measured to be more-or-less negatively shifted. On the other hand, the TG M-TFT demonstrated ferroelectric-driven memory behaviors representing the counterclockwise hysteresis of I_D in the transfer curve, as indicated by the arrows. The difference in the V_G values for the forward and reverse sweeps, which is generally defined as the memory window, was found to be approximately 4.9 V at a voltage sweep range of -14 to 10 V. These results clearly suggested that the individual BG oxide TFT and TG M-TFT devices operated in a very sound manner.

Then, the DG configuration of the fabricated M-TFT was characterized, as shown in Fig. 5(a), in which the I_D–V_G characteristics were measured when the TG voltage ($V_{\rm TG}$) was swept from -14 to 10 V with a floating condition for the BG voltage ($V_{\rm BG}$). When the measurements were repeatedly carried out three times at a V_D of 1.0 V, the device behaviors, including the $V_{\rm on}$ and the memory window width, were confirmed to be almost the same at each measurement. This is very desirable and shows the device stability when operating the memory device with the same driving conditions every time. We are aware that this result can be guaranteed only when both

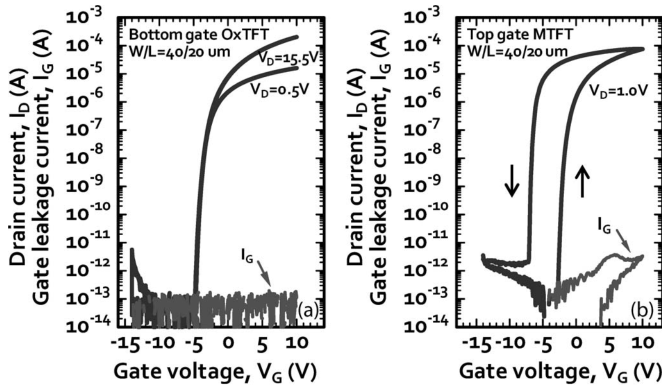

Fig. 4. I_D–V_G transfer characteristics and gate leakage currents of the fabricated (a) BG oxide TFT at V_D's of 0.5 and 15.5 V and (b) TG ferroelectric M-TFT at a V_D of 1.0 V. The measurements were performed in a double sweep mode of V_G. The W/L values of evaluated TFTs were 40/20 μm. Arrows indicated in (b) represents the hysteresis direction for the forward and reverse sweeps in V_G.

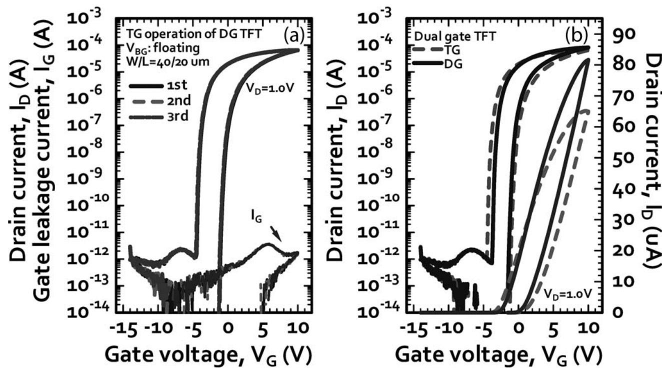

Fig. 5. (a) I_D–V_G transfer characteristics of the DG M-TFT when V_{TG} was swept from -14 to 10 V with the floating condition of BG. The measurements were repeatedly carried out three times at a V_D of 1.0 V. (b) Comparisons of the transfer curve between the TG-only and DG configurations for the fabricated DG M-TFT. The plots in linear scale were also described.

the bulk and interface of the active and GI layers are carefully controlled by optimizing the fabrication process. Fig. 5(b) shows comparisons of the transfer curves between the TG and DG configurations for the fabricated DG M-TFT. The measured I_D of the DG configuration was approximately 1.3 times higher than that of the TG configuration, which was well confirmed by the plots described on a linear scale. The field-effect mobilities at the linear region (μ_{lin} at a V_D of 1.0 V) for the TG and DG configurations were estimated to be 38.5 and 32.1 cm^2 V^{-1}s^{-1}, respectively, in which the actual gate capacitances for the cases of the TG (C_{TG}) and DG (C_{DG}) operations were examined by C–V measurements to calculate the μ_{lin} values. The C_{TG} and C_{DG} at the accumulation region were measured to be 1.1×10^{-7} and 1.6×10^{-7} F, respectively. For the DG operation, two parallel-connected P (VDF-TrFE) and Al_2O_3 capacitors were exploited to control the twofold channels. A small decrease in μ_{lin} for the DG case may originate from the asymmetric relations between the C_{TG} and C_{DG} of the TG and BG operations. The SS values for the TG and DG configurations were measured to be 0.17 and 0.13 V/dec, respectively. Although the improvements in the transistor performances observed for the DG M-TFT were

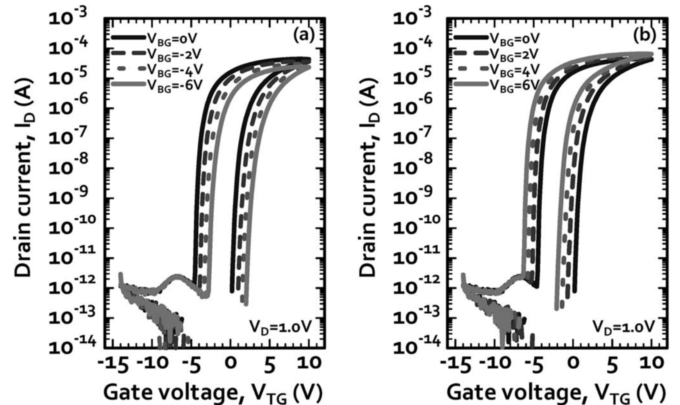

Fig. 6. Variations in the I_D–V_{TG} characteristics of the DG M-TFT when V_{TG} was normally swept from -14 to 10 V and the fixed bias applied to BG was changed (a) from 0 to -6 V and (b) from 0 to 6 V. V_D was set to be 1.0 V.

not as remarkable as those for the TG operation, the obtained characteristics were evaluated to be sufficiently good for the demonstrated DG M-TFT with both oxide and M-TFTs in a vertical direction.

The most expected and interesting behavior of the DG M-TFT is the ability to arbitrarily control the V_{on} location. Fig. 6(a) and (b) shows the variations in the I_D–V_{TG} characteristics when the fixed bias condition of V_{BG} was changed from 0 to -6 V and from 0 to 6 V, respectively. The V_{on} of the DG M-TFT was dynamically modulated to -2.1, -1.4, -0.7, 0.2, 1.0, 1.5, and 2.0 V when the fixed V_{BG} was set to 6, 4, 2, 0, -2, -4, and -6 V, respectively. It is also noticeable that this V_{on} control can be reversibly obtained without any change in the width of the memory window. In particular, the positive V_{on} values obtained at a negative V_{BG} of less than -2 V are expected to be very beneficial for the M-TFT, because the read-out and retention operations can then be carried out at a V_{TG} of 0 V, and the TFT does not have a current flow in the stand-by state. This situation is also significant, because it is preferable for the memory window of the DG M-TFT to be located with its center around a V_G of 0 V, which is very favorable for obtaining a longer retention time for the programmed data [39]. It is supposed that the fixed bias condition for the V_{BG} could be reduced by controlling the film thickness of the BGI.

Next, the programming behaviors of the DG M-TFT were examined, particularly when a fixed bias condition for the V_{BG} was set during write and read-out (W/R) operations. Fig. 7(a) and (b) simply describes the terminal information of the DG M-TFT and the timing diagram for W/R operations, respectively. Positive or negative voltages were applied to TG for the *on* and *off* programming events, respectively, in which the voltage amplitudes (V_{TGP}) could be appropriately determined according to the obtained transfer characteristics. At the same time, the BG was pulled down to a given negative voltage (V_{BGP}) for both the *on* and *off* programming. During the retention period, all of the terminals were maintained at 0 V or more naturally cut off. For the read-out operation, the BG was pulled down again to the same voltage (V_{BGR}) level as the V_{BGP}, and V_{DS} was turned on. Although a specified bias for V_{TG} can sometimes be applied to maximize the memory margin, which is generally determined at the negative region, it

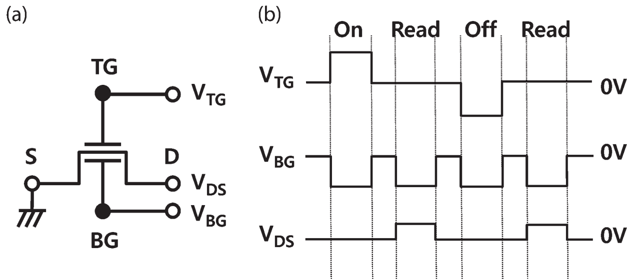

Fig. 7. (a) Device terminal configuration of the DG M-TFT. (b) Timing diagram for the *on* and *off* programming, and read-out operations.

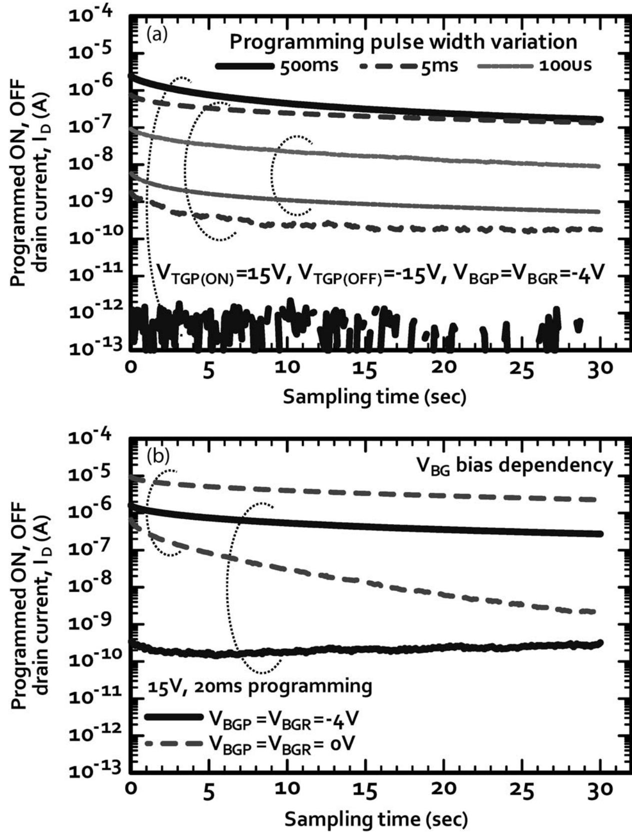

Fig. 8. Variations in the programmed I_D for the ON- and OFF-states with the lapse of sampling time. (a) $V_{\rm TGP}$, $V_{\rm BGP}$, and $V_{\rm BGR}$ were set to be ±15, −4, and −4 V, respectively, and the programming pulsewidth was changed to 500 ms, 5 ms, and 100 μs for the *on* and *off* programming events. (b) The amplitude and duration of $V_{\rm TGP}$ were ±15 V and 20 ms, respectively, and $V_{\rm BGP}$ and $V_{\rm BGR}$ was changed to −4 and 0 V. The bias conditions of all terminals were maintained at 0 V during the retention and read-out periods.

is more desirable to deduce the optimized operating conditions without additionally biasing the $V_{\rm TG}$. Fig. 8(a) shows the variations in the programmed I_D values for the ON- and OFF-states with the passage of sampling time when the $V_{\rm TGP}$, $V_{\rm BGP}$, and $V_{\rm BGR}$ were set to ±15 V, −4 V, and −4 V, respectively. When the programming pulse-width was changed to 500 ms, 5 ms, and 100 μs, the memory *on*/*off* ratio was measured to be approximately 2.0×10^6, 4.3×10^2, and 1.6×10, respectively. Even though the memory margin decreased with the decrease in the programming pulsewidth, it was very encouraging to obtain a memory *on*/*off* ratio of more than 10, even with a 100-μs width. This result shows a dramatic improvement in programming speed for the M-TFT using the P(VDF-TrFE) GI.

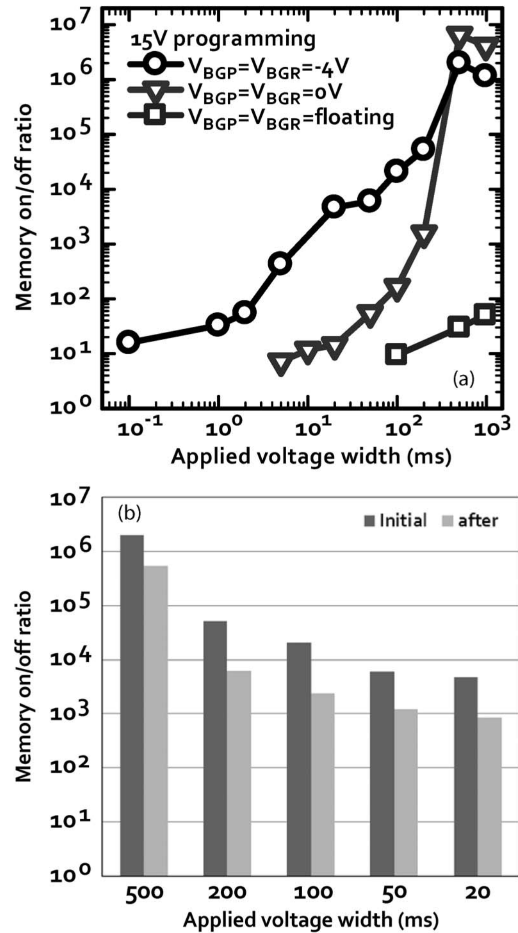

Fig. 9. (a) Summary of the variations in memory *on*/*off* ratio when $V_{\rm BGP}$ and $V_{\rm BGR}$ were changed to −4 V, 0 V, and floating during the programming events, in which the pulse duration was varied from 100 μs to 1 s. (b) Changes in the memory *on*/*off* ratio from the initially programmed values to the states after a lapse of 30 s. $V_{\rm BGP}$ and $V_{\rm BGR}$ were set to be −4 V, and the programming pulse duration was varied from 500 to 20 ms. The ON- and OFF-states were programmed by applying a $V_{\rm TG}$ of 15 and −15 V, respectively.

The retention time for each memory state with a different *on*/*off* ratio is also one of the most important points to be evaluated. For the conventional single-gate configuration, the retention behavior of the M-TFT was closely related to the polarization states of the ferroelectric GI, in which the use of a saturated ferroelectric hysteresis loop (a larger *on*/*off* ratio) was very desirable for obtaining more stable memory operations [40]. On the other hand, it could be found from the obtained results for the proposed DG M-TFT that the variations with time evolution of the I_D values programmed with different *on*/*off* ratios did not show such markedly different behaviors, even for the case of a smaller *on*/*off* ratio, as shown in Fig. 9(b). In these measurements, the initial *on*/*off* ratios were differently programmed by changing the programming pulsewidth from 500 to 20 ms, setting the bias conditions of $V_{\rm BGP}$ and $V_{\rm BGR}$ to −4 V. The extents of the decreases in the memory *on*/*off* ratios with the passage of sampling time were observed to be almost the same when they were initially determined to be in the ranges of 2.0×10^6 to 4.7×10^3. This suggests the feasibility of more stable memory operations for the DG M-TFT from the viewpoint of data retention.

The V_{BG} bias dependence on the programming capability was evaluated under the programming conditions for a V_{TGP} of ± 15 V and 20 ms, as shown in Fig. 8(b). While stable memory operations for both the ON/OFF-states could be conducted at a V_{BG} of -4 V, the *off* operation could not normally be carried out at a V_{BG} of 0 V. The initially programmed memory margin was also critically reduced from 4700 to 14 when the V_{BG} was varied from -4 to 0 V. Fig. 9 summarizes the obtained memory *on/off* ratio as a function of the V_{TGP} pulsewidth when the bias conditions (V_{BGP} and V_{BGR}) of BG were changed to -4, 0 V, and floating. From this result, we can find two important features of the nonvolatile memory operations for the proposed DG M-TFT: 1) Keeping the bias potential of the active channel at a specified status is very preferable to obtain a sufficient memory margin for the M-TFT using the P(VDF-TrFE) GI and oxide semiconductor active channel layers. This can be accomplished by implementing the DG configuration, in which we can individually control the ferroelectric field effect and the body bias of the active channel. As can be seen in the figure, a memory *on/off* ratio of more than 10^6 could be obtained for the cases where the V_{BGP} and V_{BGR} were biased at specified points. In contrast, for the case where the BG floated, which corresponded to an operating condition similar to a conventional single-gate TFT, a memory margin of 100 at the best was obtained even for a pulsewidth as long as 1 s. (2) It is very inspiring that the dynamic optimization of the V_{BGP} and V_{BGR} could effectively reduce the required duration for the V_{TGP} and guarantee a given memory margin. In order to obtain a memory *on/off* ratio of more than 10^3 while a pulsewidth of approximately 1 ms was necessary at a V_{BG} of -4 V, the application of V_{TGP} for more than 10 ms was required at a V_{BG} of 0 V. As a result, we could confirm a memory margin of larger than 10, even when the V_{TGP} pulse duration was shortened to 100 μs. These confirmed benefits for the proposed DG M-TFT may result from the fact that the channel conductance of the active layer could be effectively modulated by controlling the bias condition of the BG. Consequently, by using the DG configuration for the proposed M-TFT, a higher memory margin can be expected with a shorter programming time.

IV. Conclusion

A nonvolatile M-TFT with a DG configuration has been proposed to effectively solve the technical issues of an M-TFT using a ferroelectric copolymer GI and an oxide semiconducting active channel, including the dynamic control of the V_{on} and the improvement in programming speed. An ALD-grown Al_2O_3 thin film with a thickness of 70 nm and spin-coated P(VDF-TrFE) thin films with a thickness of 120 nm have been chosen for the TGI and BGI, respectively. As a common active channel layer, a 10-nm-thick amorphous IGZO has been prepared using the sputtering method. We have confirmed that the fabricated DG M-TFT showed excellent device characteristics for both transistor and memory performances and that the fabrication procedures and device structure were well designed and optimized. The μ_{lin}, SS, *on/off* ratio, and gate leakage current for the DG M-TFT have been found to be 32.1 cm^2 V^{-1}s^{-1}, 0.13 V/dec, 10^8, and 10^{-12} A, respectively. Two goals of this approach have been successfully demonstrated. The V_{on} of the proposed DG M-TFT has been dynamically modulated by controlling the fixed bias condition of V_{BG}. When the fixed V_{BG} was changed from -6 to 6 V, the V_{on} varied in a range of 2.0 to -2.1 V. It was also found that control of V_{BG} was effective at enhancing the programming speed and corresponding memory margin. The required pulse duration to obtain a memory margin of more than 10 could be reduced to 100 μs when V_{BG} was set at -4 V, which is a thousand times faster than the case of the floating BG condition. We can reach the following conclusions based on the results obtained. 1) The employment of the DG configuration for the proposed M-TFT can be a good solution for improving the device controllability of V_{on} and the programming speed. This feature provides the benefits of both low power and high performance for the proposed DG M-TFT. 2) This DG configuration does not cause any additional complexity in the fabrication process because the driving circuitry composed of oxide TFTs should eventually be integrated with the memory array in the real system. Furthermore, the vertical formation of the DG M-TFT does not result in a feature size loss for the device to improve its performances. 3) The suitable convergence of the organic GI and inorganic active layers can be one of the best candidates to provide a highly functional memory device, even at a lower process temperature. Although the detailed physical mechanisms of device operations should be further investigated in future works, it can finally be concluded that the proposed organic/inorganic hybrid DG-type M-TFT is very promising as a nonvolatile memory device embeddable into the next-generation large-area electronics.

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