A Low-Power Scan Driver Circuit for Oxide TFTs

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***Abstract*—The scan driver composed of oxide thin-film transistors (TFTs) tends to exhibit anomalously high power consumption because the oxide TFT often has negative threshold voltage. In order to resolve this problem, we have invented a new scan driver circuit in which most TFTs are turned off with negative V_{GS} and no TFT with zero V_{GS} is located between the high and low supply voltages. As a result, we could maintain the power consumption within six times of the normal value in spite of the negative threshold voltage of the oxide TFT.**

***Index Terms*—Low power, negative threshold voltage, oxide thin-film transistors (TFTs), scan driver.**

I. Introduction

As THE frame rate and the resolution of the active-matrix liquid-crystal display (AMLCD) are enhanced, the on-current of the thin-film transistor (TFT) should be improved, as well as the signal line conductance, to deliver the data voltage to each pixel within limited switch-on time [1]. The prevailing amorphous silicon (a-Si) TFT has reached the limit and is no more suitable for higher performance AMLCDs. Although the polycrystalline silicon (poly-Si) TFT meets this requirement, the process complexity of the poly-Si TFT is still a critical obstacle to large-area AMLCD television application. TFTs employing metal–oxide–semiconductors such as In–Ga–Zn–O (IGZO) have attracted much attention in recent years because they exhibit high on-current and low process cost. The oxide TFT is also expected to be used in the active-matrix organic light-emitting diode display because it is more stable than the a-Si TFT and has better short-range uniformity than the laser-annealed poly-Si TFT [2], [3].

However, the oxide TFT often exhibits negative threshold voltage (V_T) by process fluctuation and external influences such as illumination and bias stress [4]–[7]. Accordingly, a considerable amount of current flows at zero gate-to-source bias (V_{GS}). Due to the possible negative V_T of the oxide TFTs, it is not desirable to utilize conventional circuit scheme when we make driving circuitry on a display panel. Kim *et al.* have reported new scan driver circuits that properly operate with the oxide TFTs by applying negative V_{GS} to turn off the TFTs [8], [9]. However, some TFTs are turned off with zero V_{GS} in each stage of their scan driver. The leakage current through these TFTs brings about anomalously large power consumption. In this letter, we propose a low-power scan driver circuit in which no TFT with zero V_{GS} is located between the high and low supply voltages.

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II. Operation of the Scan Driver

Each stage of the new scan driver is composed of eight TFTs and three capacitors, as shown in Fig. 1(a). Four clock signals, i.e., CK, CKB, CKL, and CKLB are used [see Fig. 1(b)]. CK and CKL have the same waveform except that the low voltage level of CKL is lower than that of CK. Thus, do CKB and CKLB [see Fig. 1(c)]. The low level of CKL and CKLB is also lower than V_{SSL} and V_{SS} to turn off the TFTs completely.

TFT M1 admits the carry signal CR[N-1] of the previous stage. M2 transfers the CK signal to the output with the aid of bootstrapping when the current stage have received a high level of CR[N-1]. Capacitor C_B facilitates the bootstrapping effect. M3 and M4 keep OUT[N] low alternately when OUT[N] should be low. M4 is controlled by the pulldown (PD) node that follows the waveform of CKL by M5 and C_{PD} except when the F node is boosted. When the F node is boosted by bootstrapping to make OUT[N] high, M6 is turned on with V_{GS} much higher than V_{DD}. Therefore, the voltage of the PD node falls almost down to V_{SS}, although M5 is turned on. In this case, the pulldown TFT M4 is almost turned off, and OUT[N] reaches the same high level of CK. At the same time, the carry signal of the current stage CR[N] is also high because M7 is turned on and M8 is turned off. In the following phases, the F node is pulled down to V_{SS} periodically through M1 of the current stage and M7 and M4 of the previous stage. When the F node is not connected to V_{SS} (M1 is off), its voltage becomes lower than V_{SS} due to the capacitive coupling with the falling transition of CKLB through C_{IN}. During this period, CR[N-1] is connected to V_{SSL} that is lower than V_{SS} to help keeping the F node below V_{SS}.

Most of the power consumption in a scan driver is used by clock signals when the TFTs have enhancement-mode characteristics. However, power dissipation due to the leakage current through incompletely-turned-off TFTs anomalously increases as V_T becomes negative because there are thousands of such TFTs in a scan driver. To resolve this problem, it is effective to reduce the TFT leakage current in hundreds of

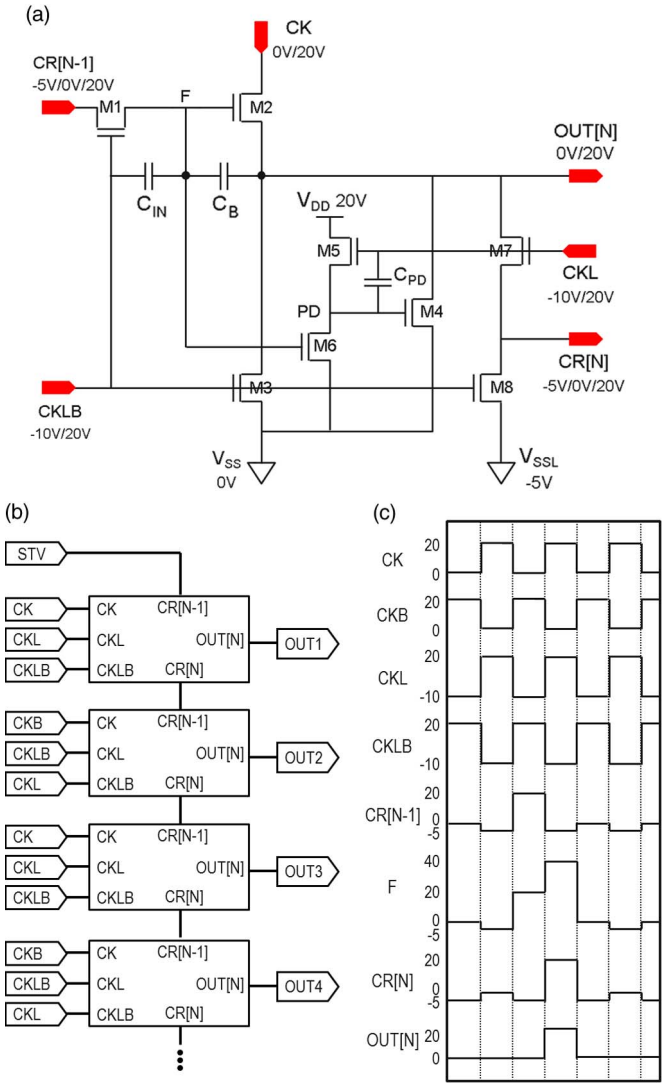

Fig. 1. (a) Unit circuit diagram of the scan driver for oxide TFTs. (b) Block diagram of the scan driver with the signal input/output indicated. (c) Timing diagram of the input/output signals.

low-output stages rather than the current in a single high-output stage.

In the proposed circuit, there are three TFTs, i.e., M2, M5, and M6, that may lie between V_{DD} and V_{SS} when the output is low. However, they are completely turned off with negative V_{GS} as follows. First, V_{DS} of M2 is $V_{DD}-V_{SS}$ only when CK is high. During this period, M2 is turned off with negative V_{GS} because the F node has been pulled down below V_{SS} by the capacitive coupling with the falling transition of CKLB. The F node is also connected to the gate of M6 of which V_{DS} is $V_{DD}-V_{SS}$ during this period. Therefore, M6 is also completely turned off, and the current path through M6 and M5 is blocked while CK is high. When CK is low and CLKB is high, the voltage of the F node is same with V_{SS}, and M6 is not completely turned off. However, M5 is turned off with negative V_{GS} by CKL in this time. In addition, the PD node is pulled down close to V_{SS} by the capacitive coupling through $C_{\rm PD}$ at the falling transition of CKL. This also prevents the positive dc V_{GS} stress on M4, the negative V_{GS} stress on M5, and the dc V_{DS} stress on M6.

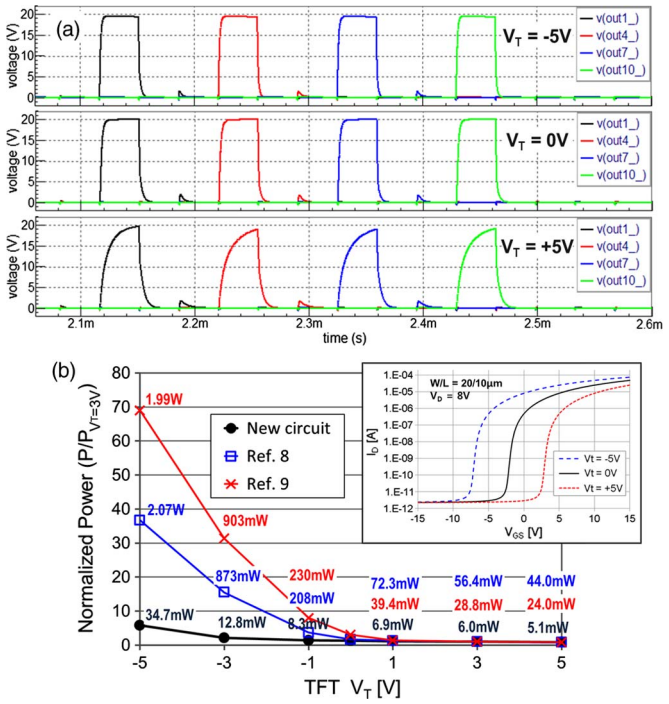

Fig. 2. SPICE simulation results of the scan driver for various TFT V_T values. (a) Output-voltage waveforms. (b) Normalized power consumption for VGA (480 lines) panel. Frame rate = 60 Hz. Gate line load = 5 kΩ and 50 pF.

III. Simulation Results

We used SmartSpice in simulating the operation of the new scan driver circuit. First, we made a TFT model by fitting a typical IGZO TFT characteristic that we measured. Then, we generated many models with different V_T values by the parallel shift of the original model. The gate–source/drain overlap capacitance is 1.45 nF/m in our TFT model. Assuming a video graphics array (VGA) (640 × 480) AMLCD panel, we attached a 5-kΩ resistor and a 50-pF capacitor to every output node to emulate the gate line load. The channel widths of M1–M8 are 100, 180, 50, 40, 30, 80, 80, and 50 μm in order, and the channel lengths are all 10 μm. To drive a larger load, the output buffer M2 should be wider. The capacitances of $C_{\rm IN}$, C_B, and $C_{\rm PD}$ are 0.3, 4, and 0.5 pF, respectively.

Fig. 2(a) shows the simulated voltage waveforms at the load capacitances of the first, fourth, seventh, and tenth stages. The circuit properly works, although the V_T value of the TFTs varies from −5 to +5 V. TFT model characteristics used in the simulations are shown in the inset of Fig. 2(b).

We calculated the power consumption of the new scan driver and the previous scan drivers reported in the references [6], [7]. Most of the simulation conditions were made the same for the circuits in comparison, e.g., TFT model parameters, 5-kΩ and 50-pF gate line load, 480 stages, and 60-Hz frame rate. However, the TFT sizes in the previous circuits were kept the same as described in the references because it might lead to an unfair comparison to change the TFT sizes as we like. The sums of TFT widths in a single stage of the previous circuits are about 3.5 times larger than that of the new one. In addition, the output voltage swings of the previous circuits are also larger (25 V). Therefore, the power consumption of the previous circuit is much higher than that of the new one (56.4 and 28.8 mW

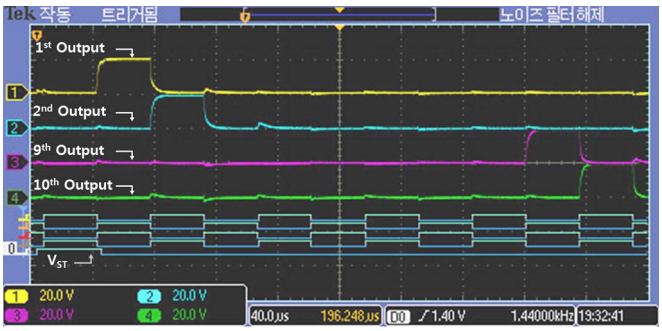

Fig. 3. Measured output waveforms of the scan driver fabricated by the IGZO TFT process. Logic levels of the clock and start signals are also shown. Clock frequency is 14.4 kHz.

versus 6.0 mW for $V_T = +3$ V). In order to compare the power consumption fairly for the negative V_T range, we normalized the data based on the value of $V_T = +3$ V. The results in Fig. 2(b) show that the power consumption of the new circuit for $V_T = -5$ V increases less than six times (6.0 $\rightarrow$ 34.7 mW), whereas those of the previous ones increase about 37 times (56.4 mW $\rightarrow$ 2.07 W) and 69 times (28.8 mW $\rightarrow$ 1.99 W), respectively. Even for $V_T = -3$ V and -1 V, the new circuit is remarkably superior in suppressing the power consumption increase due to leakage currents.

IV. Fabrication Results

Fig. 3 shows the measured output waveforms of the fabricated scan driver using IGZO TFTs. The V_T value of the TFTs ranged from -4 to $+5$ V. The field-effect mobility measured in the saturation mode was 9 ± 1 cm$^2/$(V $\cdot$ s), and the subthreshold slope ranged from 0.21 to 0.27 V/dec. The fabrication process is described in [4]. The critical dimension and the layer-to-layer misalign margin in the mask layout are 10 and 2 μm, respectively. Logic levels of the clock and start signals are also shown. The clock frequency was set to be 14.4 kHz in order to make the output pulsewidth 34.7 μs like the simulation condition. Although the V_T value of the fabricated TFT ranged from -4 to $+5$ V, the circuit successfully worked. The power consumption of the fabricated circuit with 10 stages ranged from 10 to 21 mW, although it was 5.86 mW in the simulation for $V_T = -5$ V. This difference is attributed to the mismatch of TFT characteristics between the simulation and the real fabrication.

V. Conclusion

A low-power scan driver circuit based on the metal–oxide TFT having negative V_T has been developed. The scan driver employs two additional clock signals falling below V_{SS} and the clock feedthrough to turn off the TFTs with negative V_{GS}. As a result, there is no TFT turned off with zero V_{GS} between V_{DD} and V_{SS} in any low-output stage. The severe increase in the power consumption due to the leakage current through the oxide TFT in the conventional circuit has been reduced from 37 to 6 times in the new one. The fabrication result also confirms that the new scan driver circuit stably works with the oxide TFTs with negative V_T values.

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