Solid-State Electronics 89 (2013) 171–176

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Comparative studies on electrical bias temperature instabilities of In–Ga–Zn–O thin film transistors with different device configurations

Min-Ki Ryu [a], Sang-Hee Ko Park [a], Chi-Sun Hwang [a], Sung-Min Yoon [b,*]

[a] *Convergence Components & Materials Laboratory, Electronics and Telecommunications Research Institute (ETRI), Yuseong, Daejeon 305-700, Republic of Korea*
[b] *Department of Advanced Materials Engineering for Information and Electronics, Kyung Hee University, Yongin, Gyeonggido 446-701, Republic of Korea*

ARTICLE INFO

Article history:
Received 10 March 2013
Received in revised form 15 May 2013
Accepted 20 August 2013
Available online 18 September 2013

The review of this paper was arranged by Dr. Y. Kuk

Keywords:
Oxide semiconductor
Thin-film transistor
In–Ga–Zn–O (IGZO)
Top-gate
Bottom-gate

ABSTRACT

We investigated the effect of positive bias temperature stress (PBTS) on the device stabilities of In–Ga–Zn–O thin film transistors with bottom gate and top gate structures. Under the PBTS conditions at the gate voltage of +20 V and the temperature of 60 °C, the turn-on voltage experienced a negative shift of −1.5 V for the top gate device, while a larger positive shift of 3.0 V was observed for the bottom gate device. From the variations in transfer characteristics at various temperatures and the discussions on the thermal activation energy, it was suggested that these different behaviors of two devices originated from interface trap densities caused by the plasma damage and the pinning of Fermi energy level for the bottom and top gate devices, respectively. It was very encouraging that the variation of the turn-on voltage could be minimized when the top gate device was fabricated to have a very controlled interface.

© 2013 Elsevier Ltd. All rights reserved.

1. Introduction

Technical potentials of oxide semiconductor thin-film transistors (TFTs) have been aggressively exploited as promising backplane devices for large-area and high resolution flat-panel displays such as active-matrix organic light-emitting diode (AMOLED) and active-matrix liquid crystal display (AMLCD) [1–4]. For the full-scale commercialization of these panels, device reliabilities of oxide TFT backplanes should be carefully controlled with their high performances including high field-effect mobility and superior uniformity. Amorphous In–Ga–Zn–O (α-IGZO) is one of the most typical material compositions of the oxide semiconductors and have been mainly employed for the fabrication of oxide TFTs [5–7]. So far, device reliability characteristics of α-IGZO TFTs have been investigated under various stress conditions such as negative/positive gate bias stress (NBS/PBS) [8,9], negative gate bias illumination stress (NBIS) [11,12,10], gate bias temperature stress (BTS) [13,14], drain bias stress [15,16], constant current stress [17], and ambient effects [18–21], in which instability mechanisms at various stress situations and suitable strategies for stability improvements have been actively discussed. Typical observations could be classified into two kinds of feasibilities: (1) hole trapping into the gate insulator bulk and/or at the interface between the gate insulator and oxide channel layer, (2) changes of carrier density in the active channel due to the additional state creation. Related discussions and investigations on these issues are now on process and definite conclusions are still controversial. Furthermore, these stability characteristics of oxide TFTs were observed to be very sensitively affected by the process methodologies and device structures [22–24]. Actually, we previously demonstrated an excellent NBS and NBIS characteristic of the α-IGZO TFT by introducing the interface protection layer (PL) between the gate insulator and active channel layers [25]. On the other hand, most devices evaluated in many literatures were fabricated to be bottom gate (BG) structures. Gate insulators of the BG oxide TFTs are easy to be damaged during the sputtering process of IGZO channel layer, even though they can be manufactured by using conventional fab facilities for the a-Si TFTs. Consequently, the top gate (TG) structure can be also a promising alternative to obtain both high performance and excellent stability for the practical applications of oxide TFT backplanes. From these viewpoints, systematic comparative studies on device reliabilities between the BG and TG-structured α-IGZO TFTs would provide some very interesting and important insights to understand the stability issues of oxide TFTs. In this letter, two types of BG and TG α-IGZO TFTs were fabricated and their positive gate bias temperature stabilities (PBTS) were investigated and compared. The degree of instabilities and possible mechanisms were totally different between two types of devices. From the obtained results, it was elucidated that the

* Corresponding author. Tel.: +82 31 201 3617; fax: +82 31 204 8114.
E-mail address: sungmin@khu.ac.kr (S.-M. Yoon).

0038-1101/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2013.08.008

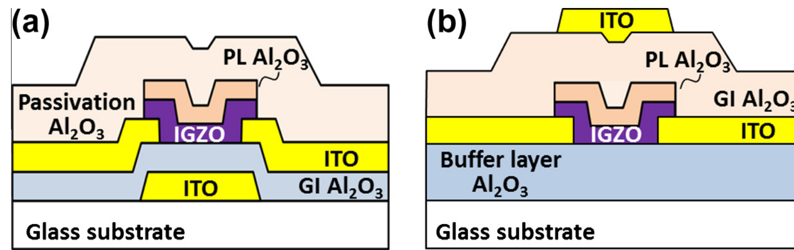

Fig. 1. Schematic cross-sectional diagrams of the fabricated (a) bottom-gate and (b) top-gate α-IGZO TFTs. All the electrodes were patterned by ITO layers. The first Al_2O_3 layers correspond to the gate insulator and buffer layers for the bottom- and top-gate TFTs, respectively. The second Al_2O_3 layers are worked as the passivation and gate insulator layers for both TFTs, correspondingly.

appropriate design scheme for the device structure and fabrication process are very important to realize highly reliable α-IGZO TFTs.

2. Experimental details

α-IGZO TFTs with BG and TG structures were fabricated with following procedures. For the first step, a 150 nm thick indium-tin-oxide (ITO) thin film was deposited by radio-frequency (rf) magnetron sputtering and patterned into gate electrodes on the glass substrate of BG device. Al_2O_3 films with thickness of 185 nm were prepared via atomic layer deposition (ALD) method using an Al precursor of trimethylaluminium and water vapor at 150 °C for both TFTs, which correspond to the gate insulator and buffer layers for the BG and TG devices, respectively. The second ITO layers were deposited and patterned into source/drain (S/D) electrodes. 25 nm thick α-IGZO active layer was formed by rf sputtering of a single IGZO (In:Ga:Zn = 1:1:1 atomic ratio) target as active channel layers of both devices. The deposition process was carried out in a mixed atmosphere of Ar and O_2 [Ar:O_2=4:1] at room temperature.Al_2O_3 layers with thickness of 9 nm were subsequently formed by ALD method at 200 °C as interface PLs to protect underlying IGZO active layers from chemical damages during the channel patterning process [25]. For this reason, the PL was introduced right before the active patterning process for both TG and BG devices. Then, 176 nm thick Al_2O_3 layers were prepared on the patterned active channels as passivation and main gate insulator 150 °C for BG and TG devices, respectively. The last ITO film was deposited and patterned into gate electrodes of TG device. Fig. 1 (a) and (b) illustrates the cross-sectional schematic diagrams of the fabricated BG and TG devices, respectively. The fabricated devices were finally annealed at 250 °C for 2 h to guarantee sound device behaviors, which is generally performed for the oxide TFTs. The electrical characteristics of the TFTs were evaluated using a semiconductor parameter analyzer (Agilent B1500A) in a dark box. The PBTS stress tests for the devices were carried out on a hot chuck equipped on the probe positioning system from room temperature to 100 °C in an air ambient.

3. Results and discussions

Fig. 2(a) and (b) shows the drain current (I_{DS})-gate voltage (V_{GS}) transfer curves for the fabricated BG and TG devices, respectively. The measurements were successively carried out at two drain voltages (V_{DS}'s) of 0.1 and 10.1 V at forward and reverse sweeps of V_{GS} for each device with the gate width (W) and length (L) of 40 and 20 μm, correspondingly. For the BG device, the field effect mobility (μ_{fe}), threshold voltage (V_{th}), turn-on voltage (V_{on}), which was defined as the voltage when the I_{DS} launched from the off-current level, and subthreshold swing (SS) were measured to be 15.0 cm^2 - V^{-1} s^{-1}, 0.68 V, −0.37 V, 0.09 V/dec, respectively. The same device parameters of the TG device were obtained to be 14.9 cm^2 V^{-1} s^{-1}, 0.38 V, −0.49 V, and 0.08 V/dec, respectively. Both devices exhibited excellent device behaviors and there were not so marked differences between the devices. Irrespective of these good characteristics, it is important to check the electrical bias and/or temperature instabilities of the devices. In order to confirm the variations in PBS stabilities of the BG and TG devices, a V_{GS} of +20 V was applied to the gate terminals for 10^4 s at room temperature and corresponding transfer curves (linear and logarithmic) were measured at V_{DS} of 10.1 V, as shown in Fig. 2(c) and (d), respectively. As can be seen in figures, it can be very noticeable that the characteristics did not experience any remarkable instability for both devices. After the PBS stress for 10^4 s, the μ_{fe},V_{on}, and SS values of BG and TG devices were measured to be 16.3 and 16.2 cm^2 V^{-1} s^{-1}, −0.26 and −0.32 V, and 0.10 and 0.10 V/dec, respectively. Although small positive shifts in V_{on} were observed, both fabricated devices showed good immunity to the PBS stress at room temperature. On the other hand, for the cases of NBS and NBTS evaluations, there were no marked variations in their transfer characteristics for 10^4 s and no marked differences between the BG and TG devices. If any electron–hole pair would not be generated by a photon energy with illumination effect, as expected during the NBTIS test, undesirable hole trapping caused by the NBTS would not be a critical issue for the well-fabricated IGZO TFTs.

The next evaluations were carried out at 60 °C, in which a V_{GS} of +20 V was also applied to the gate terminals for 10^4. Fig. 3(a) and (b) shows the variations in I_{DS}–V_{GS} transfer characteristics for the fabricated BG and TG devices with the lapse of stressed time, respectively. The increase in temperature under the positive gate bias made big differences in device characteristics from those tested at room temperature as well as between the BG and TG devices. Fig. 3(c) and (d) summarize variations in V_{on}, SS, and μ_{fe} for both devices with the evolution of PBTS test time, respectively. The most marked difference was that the instability in V_{on} of the BG device was much larger than that of the TG device. The positive shift in V_{on} under PBTS condition without marked degradation of the μ_{fe} and SS can be generally explained to be due to the electron trapping into the bulk region of gate insulator and/or interface between the gate insulator and active channel layers [8]. It can be considered that a large ΔV_{on} of more than 3.0 V for the BG device was caused by some plasma-induced mechanical damages to the gate insulator during the sputtering process for the IGZO formation. Especially, considerable increase in trap sites at the interface may greatly influence on the electron trapping mechanism at an elevated temperature. On the other hand, it is also very important to note that the instability of the TG device appeared to be some negative shift of the V_{on}, which was completely different from the general trend observed for the PBTS condition. This anomalous behavior confirmed for our TG device suggests that its PBTS instability could be caused by other possibilities than the electron trapping mechanism. We believe that this negative shift in V_{on} under PBTS can be observed for only limited devices fabricated with

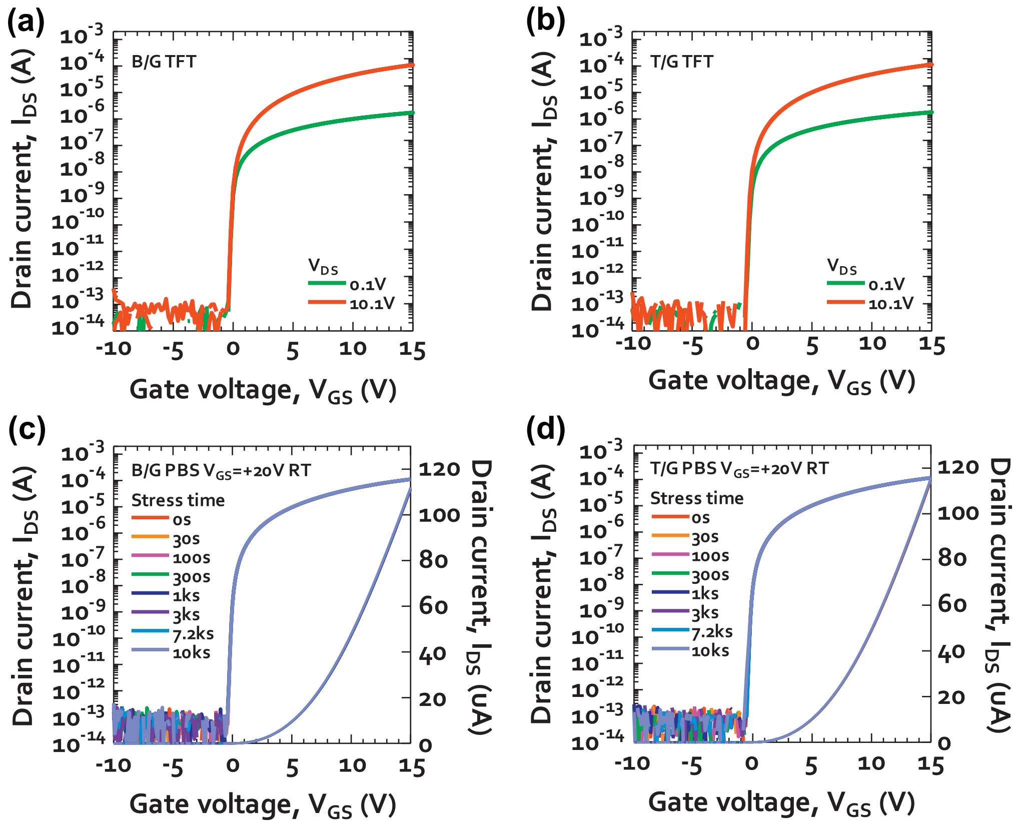

Fig. 2. I_{DS}–V_{GS} transfer characteristics of the fabricated (a) bottom-gate and (b) top-gate α-IGZO TFTs. The gate width and length of each device was 40 and 20 μm, respectively. The measurements were successively carried out in forward and reverse directions of V_{GS} at two V_{DS}'s of 0.1 and 10.1 V. Variations in the I_{DS}–V_{GS} characteristics for the (c) bottom-gate and (d) top-gate TFTs as a function of the stressed time for 10^4 s at room temperature under the positive bias stress at V_{GS} of 20 V.

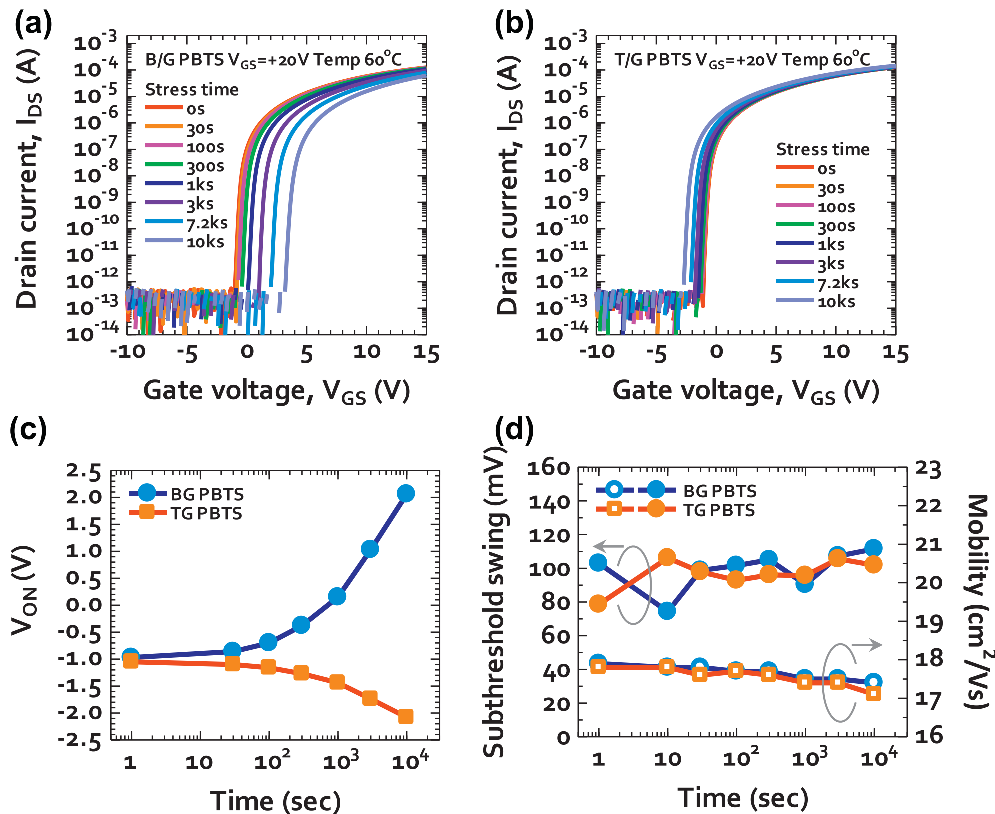

Fig. 3. Sets of I_{DS}–V_{GS} transfer curves of the (a) bottom-gate and (b) top-gate α-IGZO TFTs with the lapse of stressed time at 60 °C under the positive bias stress condition at V_{GS} of 20 V. Variations in (c) V_{on}, (d) SS and μ_{fe} for the bottom- and top-gate TFTs as a function of the stressed time for 10^4.

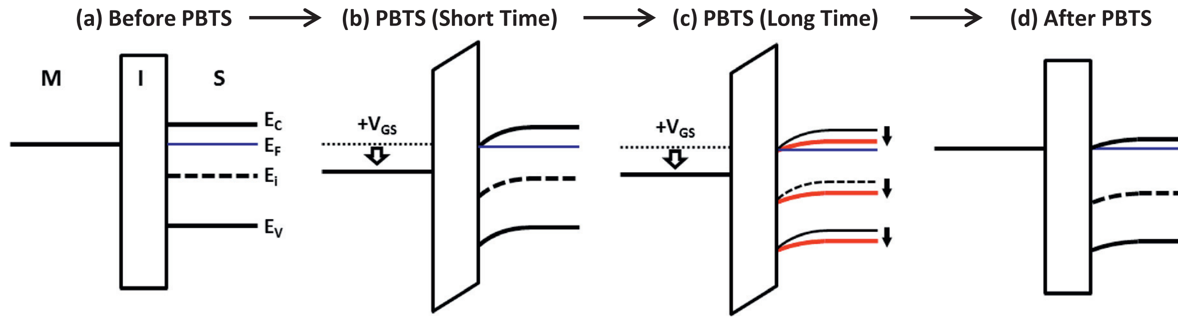

Fig. 4. Schematics of changes in energy band diagrams for (a) before the PBTS, (b) initial stage during the PBTS, (c) final stage during the PBTS, and (d) after the PBTS.

careful prescriptions for the very excellent interface quality. Otherwise, the electron trapping phenomena are dominantly activated and the positive shift of V_{on} is conventionally defined as the PBTS instabilities. From this reason, there have hardly been oxide TFTs reported to experience the negative shift of V_{on} under the PBTS tests among previous literatures. Some feasibility can be expected for these behaviors of the TG device. One possible scenario is that the excess holes injected from the ITO gate electrode into the ITO/Al_2O_3 interface, which might be a little damaged by the sputtering process of ITO, can cause the negative shift in V_{on} under the PBTS. However, it is supposed that the V_{on} does not shift as much as for the case of charges trapped near the IGZO/Al_2O_3 interface because the trapped charges are near the gate. Although we cannot completely rule out the hole injection mechanism, an observed ΔV_{on} of approximately −1.5 V for our fabricated TG device can also be explained as shown in Fig. 4(a)–(d).

Before the test of PBTS, the energy band diagram for the metal–insulator-semiconductor (MIS) structure can be described in Fig. 4(a), in which the work function difference between the metal and semiconductor is assumed to be negligible. If the positive bias with a given electric field starts to be applied to the gate terminal, the energy difference between the Fermi level (E_F) and the intrinsic level (E_i) locally increases at the interface compared with that in the bulk region due to the energy band bending [Fig. 4(b)]. This is the initial stage of PBTS test, which is not so different from the normal gate-bias condition. On the other hand, a continuous application of positive bias stress at a higher temperature may induce additional carriers below the conduction band minimum (E_c) and near the tail states. These carriers can be generated from the shallow donors originated by the hydrogen doping effect. The residual hydrogen within the PL of ALD-grown Al_2O_3 film can be supposed to be incorporated into the IGZO channel at an elevated temperature condition with the lapse of stressed time during the PBTS tests. As results, the amount of free electrons contributing the electronic conduction is expected to increase [26]. However, the free electrons accumulate even in the extended states of the conduction band and band bending is somewhat released, which results from the fact that the E_F is subject to be pinned due to the extrinsically generated bulk defects within the IGZO. Consequently, the energy difference between the E_F and the E_C is reduced and the energy band diagram changes as shown in Fig. 4(c). At this situation, the electron density, which is determined by the difference between the E_F and E_i, increases from the bulk to the interface regions. The energy bands modified due to the Fermi level pinning is not recovered even when the PBTS is terminated as shown in Fig. 4(d). Therefore, an accumulation mode of electrons at interface may cause the small negative shift in V_{on} after the PBTS test. It was found from lots of evaluation of devices that this negative shift in V_{on} cannot be observed for the device having severely damaged interfaces with a lot of interface trap sites for electrons.

For the same reason, the Fermi level pinning can also be considered for the BG device. It is expected that the negative shift of V_{on} could be observed even for the BG device if its IGZO/Al_2O_3 interface quality was guaranteed in an excellent manner. Actually, we have found the BG device experiencing the negative shift of V_{on} after the PBTS test when the gas mixing ratio of Ar/O_2 was specifically controlled to 9:1 during the IGZO deposition. However, in this work, the Ar/O_2 mixing ratio of 8:2 was chosen as a typical process parameter, because we had a difficulty in obtaining sufficient process window for the device fabrication and reproducibility in device characteristics. In other words, it can be said for the BG device that the effect of Fermi level pinning was screened owing to the dominant action of electron trapping mechanism. It can be found from these results that the plasma damage into the interface, which was caused by the ion bombardment effect of oxygen ions, might have a dominant influence on the device performances of the BG device rather than on the IGZO film quality itself.

Here, we have to note that the differences in amounts of interface trap density between the BG and TG devices are not so large as to be reflected in a marked variation in the SS value, which is an important criterion to evaluate the interface quality. Actually, both devices exhibited similar values of SS even after the PBS evaluations. These results strongly suggest that both devices were basically well fabricated and optimized with a sufficiently good interface properties. However, under more severe evaluation tests such as PBTS, it would be important to note that only a very small difference could make considerable changes in device reliabilities.

In this work, a detailed investigation on the temperature dependent PBTS could not be carried out because the temperature during the PBTS tests was fixed at 60 °C. However, the negative shift in V_{on} was typically confirmed to be accelerated for the IGZO-based oxide TFTs with the increase in the stress temperature during the PBTS test. In order to clearly claim the above-mentioned explanation, the temperature instabilities of BG and TG devices were investigated before [Fig. 5(a) and (b)] and after [Fig. 5(c) and (d)] the PBTS tests, respectively, in which I_{DS}–V_{GS} transfer curves were measured at the temperatures of 40, 60, 80, and 100 °C. Before the positive bias stress was applied to the device, the V_{on} was observed to be shifted into the negative direction for both devices with the increase of measurement temperature. This negative shift in the V_{on} with increasing the temperature can be explained by the thermal excitation process of the subthreshold drain current, that is, the activated electrons into the conduction band of the IGZO channel. The I_{DS} in the subthreshold region for amorphous, polycrystalline Si, and oxide semiconductor TFTs has been described by the Arrhenius model related to the thermal activation process [27–29]. In other words, at elevated temperature, more negative gate voltage is required to completely turn-off the TFTs. In this model, thermally activated electrons from the deep states of trap sites into the conduction band contribute to the current flow of I_{DS}. The observation that a relatively large shift in the

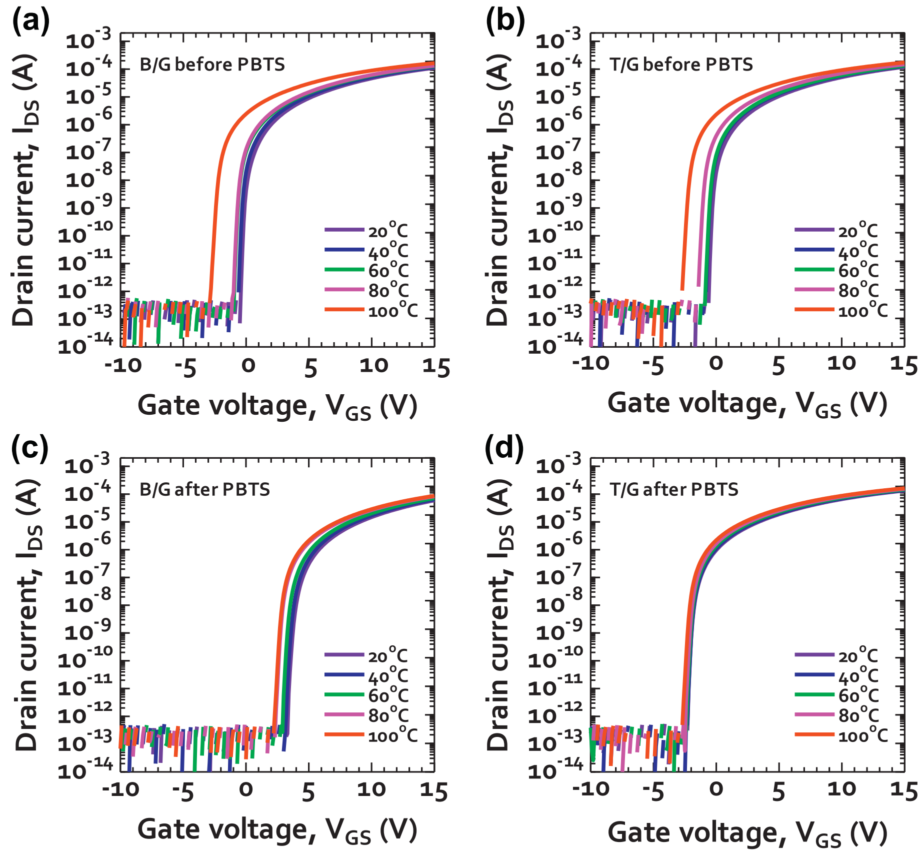

Fig. 5. Variations in the I_{DS}–V_{GS} characteristics of the (a) bottom-gate and (b) top-gate α-IGZO TFTs before the PBTS tests when the measurement temperature was varied to 40, 60, 80, and 100°C from room temperature. Comparisons of variations in the I_{DS}–V_{GS} characteristics of the stressed (c) bottom-gate and (d) top-gate α-IGZO TFTs after the PBTS tests at the same temperature conditions.

V_{on} was observed between 80 and 100 °C, as shown in Fig. 5(a) and (b), can be related to the fact that there are some relationship between the generated shallow donors and the threshold value of required energies.

After the PBTS tests, the activated electron carriers are expected to be differently behaved between the BG and TG devices according to their initial situations. For the case of BG device, the V_{on} was also negatively shifted from the point where it had been positively shifted during PBTS due to the electron trapping mechanism, as shown in Fig. 5(c). Parts of activated electron carriers contribute to the negative shift in V_{on} and remains may be simultaneously trapped at shallow interface traps beneath the conduction band, because the temperature of 100 °C is too low for trapped electrons to be completely relieved. Eventually, the ΔV_{on} of negative shift was smaller than that for the initial BG device. On the other hand, for the case of TG device, the V_{on} finally obtained from the previous PBTS test did not change any more even at the elevated temperature up to 100 °C, as shown in Fig. 5(d). It can be postulated that there was no additional shift in the V_{on} with the temperature increase because the Fermi level was already pinned at certain position near the conduction band, especially for the interface region, during the PBTS tests.

It was sometimes reported that the heat treatment performed at around 100 °C could lead to the thermal recovery of instabilities caused by the positive bias stress [30]. Therefore, it is important to check whether the high-temperature measurements may cause some additional effects after the PBTS tests. For our devices, the annealing process at the temperature of higher than 200 °C was found to be necessary for the PBTS recovery. It was also confirmed that the device characteristics were almost the same when the device was heated to 110 °C and cooled down to room temperature. Consequently, the results obtained in Fig. 5 can be concluded to fairly describe the differences in PBTS instabilities between the BG and TG devices and their temperature dependences without any recovery effect.

As mentioned above, the increase in the I_{DS} at a given V_{GS} would be limited by the thermal excitation of the carriers trapped at energy states located in deep levels within the band gap. If the electrons thermally activated from these deep trap sites into the conduction band are assumed to transport quickly toward the drain electrode owing to the laterally applied electric field, the rate-determining process would be the thermal excitation of the trapped electrons [31]. Thus, the corresponding activation energy (E_A) for the conductance of the activated electrons can be calculated as a function of V_{GS} from the Arrhenius plot using the following equation.

$$I_{DS} = I_{DS0} \cdot exp(-E_A/\kappa T) \quad (1)$$

where I_{DS0} and κ are the constant current factor for a given V_{GS} and the Boltzmann constant, respectively. In this discussion, the E_A is defined as ($E_C - E_F$) by assuming the Boltzmann statistics [27,28]. From this background, it would be very useful to compare the location of V_{GS} for the maximum E_A and the changing rate of E_A as a function of V_{GS} in understanding the internal natures of device structures. Fig. 6(a) and (b) shows variations in E_A of I_{DS} as a function of V_{GS} for the BG and TG devices, respectively, in which the estimated values of E_A of each device were compared between before and after the PBTS tests. For the BG device, the maximum E_A value of 1.91 eV, which corresponds to the highest energy barrier for thermal activation of trapped electrons, was calculated at a V_{GS}

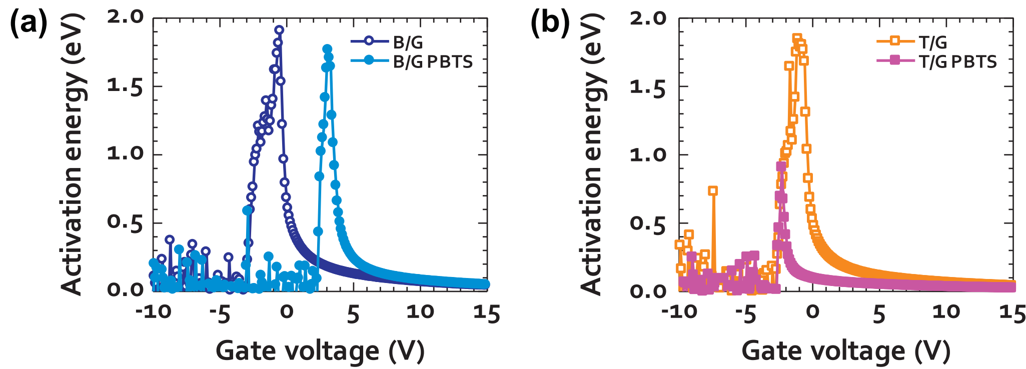

Fig. 6. Changes in the thermal activation energy of I_{DS} as a function of V_{GS} for the (a) bottom-gate and (b) top-gate α-IGZO TFTs before (blank symbols) and after (solid symbols) the PBTS tests. Corresponding values of the E_A at a given V_{GS} were calculated with the I_{DS}–V_{GS} characteristics obtained in Figs. 4 by an Arrhenius model.

of −0.5 V. After the PBTS, while the maximum E_A (1.77 eV) did not change so much, the corresponding V_{GS} was positively shifted to 3.1 V, as shown in Fig. 6(a). In contrast, the maximum E_A value of 1.85 eV for the TG device was observed at a V_{GS} of −1.1 V and dramatically decreased to 0.91 eV at a V_{GS} of −2.3 V after the PBTS, as shown in Fig. 6(b). These results suggest that there was big difference in energy level and density of the trap states within the band structure composed of gate insulator and IGZO active channel between BG and TG devices after the PBTS tests. While only the movement of flatband position occurs due to the dominant electron trapping mechanism during the PBTS for the BG device, the change in the Fermi level affected the decrease in the E_A for the TG device. The actual evaluations on the energy distribution of the total trap densities, including the gap-state density of the active channel and interface trap density, will be performed by careful calculation using Meyer-Neldel rule [29] as future works. It can be concluded from the obtained results that appropriate prescription should be carefully optimized according to the device structures and employed fabrication processes in order to ensure the electrical bias and/or temperature stabilities of IGZO TFTs.

4. Conclusions

In summary, the effect of PBTS on the device behaviors of IGZO TFTs with BG and TG structures was investigated. While there was no marked differences between the BG and TG devices under only PBS, a much larger variation of V_{on} was observed for the BG device compared to the TG device under the PBTS condition at the temperature of 60 °C. Furthermore, it was very impressive that the directions of V_{on} variations were totally different, those are positive and negative, for the BG and TG devices, respectively. An adverse physical damages by ion bombardment to the gate insulator during the IGZO deposition was one of the main origins for the generation of larger interface trap density and the eventual positive shift of V_{on} due to the electron trapping mechanism for the BG device. On the other hand, for the TG device, thanks to the absence of considerable trap sites at the interface, only a small negative shift of V_{on} was observed because of the pinning of Fermi energy level in the semiconductor band gap. The estimations on the thermal activation energy of the subthreshold drain current as a function of V_{GS} well explained these situations. From these comparative studies on the bias and temperature instabilities of IGZO TFTs with BG and TG structures, the strategies to optimize the device reliabilities can be suitably planned for the IGZO TFTs with specified device structures.

Acknowledgement

This work was supported by the Industrial Strategic Technology Development program (project number 10035225, Development of Core Technology for High Performance AMOLED on Plastic) funded by MKE/KEIT.

References

[1] Kwon JY, Son KS, Jung JS, Kim TS, Ryu MK, Park KB, et al. IEEE Electron Dev Lett 2008;29:1309.
[2] Ohara H, Sasaki T, Noda K, Ito S, Sasaki M, Endo Y. Jpn J Appl Phys 2010;49:03CD02.
[3] Lu HH, Ting HC, Shih TH, Chen CY, Chuang CS, Lin Y. SID Int. Symp. Digest Tech. Papers; 2010. p. 1136.
[4] Osada T, Akimoto K, Sato T, Ikeda M, Tsubuku M, Sakata J. Jpn J Appl Phys 2010;49:03CC02.
[5] Nomura K, Ohta H, Takagi A, Kamiya T, Hirano M, Hosono H. Nature 2004;432:488.
[6] Kamiya T, Nomura K, Hosono H. Sci Technol Adv Mater 2010;11:044305.
[7] Fortunao E, Barquinha E, Martins P. Adv Mater 2012;24:2945.
[8] Suresh A, Muth JF. Appl Phys Lett 2008;92:033502.
[9] Stryakhilev D, Park JS, Lee J, Kim TW, Pyo YS, Lee DB, et al. Electrochem Solid-State Lett 2009;12:J101.
[10] Ji KH, Kim JI, Jung HY, Park SY, Choi R, Mo YG, et al. Microelectr Eng 2011;88:1412.
[11] Chowdhury MDH, Migliorato P, Jang J. Appl Phys Lett 2010;97:173506.
[12] Oh H, Yoon SM, Ryu MK, Hwang CS, Yang S, Ko Park SH, et al. Phys Lett 2010;97:183502.
[13] Kim B, Chong E, Kim DH, Jeon YW, Kim DH, Lee SY. Appl Phys Lett 2011;99:062108.
[14] Chang GW, Chang TC, Jhu JC, Tsai TM, Syu YE, Chang KC, et al. Appl Phys Lett 2012;100:182103.
[15] Huang SY, Chang TC, Lin LW, Yang MC, Chen MC, Jhu JC, et al. Appl Phys Lett 2012;100:222901.
[16] Hsieh TY, Chang TC, Chen TC, Tsai MY, Chen YT, Jian FY, et al. IEEE Electron Dev Lett 2012;33:1000.
[17] Nomura K, Kamiya T, Kikuchi Y, Hirano M, Hosono H. Thin Solid Films 2010;518:3012.
[18] Park JS, Jeong JK, Chung HJ, Mo YG, Kim HD. Appl Phys Lett 2008;92:072104.
[19] Jeong JK, Yang HW, Jeong JH, Mo YG, Kim HD. Appl Phys Lett 2008;93:123508.
[20] Lee KH, Jung JS, Son KS, Park JS, Kim TS, Choi R, et al. Appl Phys Lett 2009;95:232106.
[21] Sung SY, Choi JH, Han UB, Lee KC, Lee JH, Kim JJ, et al. Appl Phys Lett 2010;96:102107.
[22] Ji KH, Kim JI, Jung HY, Park SY, Mo YG, Jeong JH, et al. J Electrochem Soc 2010;157:H983.
[23] Bak JY, Yoon SM, Yang S, Kim GH, Ko Park SH, Hwang CS. J Vac Sci Technol B 2012;30:041208.
[24] Abe K, Takahashi K, Sato A, Kumomi H, Nomura K, Kamiya T, et al. IEEE Trans Electron Dev 2012;59:1928.
[25] Ko Park SH, Cho DH, Hwang CS, Yang S, Ryu MK, Byun CW, et al. ETRI J 2009;31:653.
[26] Nomura K, Kamiya T, Ohta H, Ueda K, Hirano M, Hosono H. Appl Phys Lett 2004;85:1993.
[27] Slade HC, Shur MS, Deane SC, Hack M. Appl Phys Lett 1996;69:2560.
[28] Pichon L, Mercha A, Carin R, Bonnaud O, M-Brahim T, Helen Y, et al. Appl Phys Lett 2000;77:576.
[29] Jeong J, Jeong JK, Park JS, Mo YG, Hong Y. Jpn J Appl Phys 2010;49:03CB02.
[30] Chowdhury MDH, Migliorato P, Jang J. Appl Phys Lett 2011;98:153511.
[31] Jeong JK, Yang S, Cho DH, Ko Park SH, Hwang CS, Cho KI. Appl Phys Lett 2009;95:123505.