Enhanced bias illumination stability of oxide thin film transistor through insertion of ultrathin positive charge barrier into active material

Cite as: Appl. Phys. Lett. **99**, 022105 (2011); https://doi.org/10.1063/1.3610476
Submitted: 27 May 2011 . Accepted: 23 June 2011 . Published Online: 12 July 2011

Himchan Oh, Sang-Hee Ko Park, Chi-Sun Hwang, Shinhyuk Yang, and Min Ki Ryu

Enhanced bias illumination stability of oxide thin film transistor through insertion of ultrathin positive charge barrier into active material

Himchan Oh,[a] Sang-Hee Ko Park, Chi-Sun Hwang, Shinhyuk Yang, and Min Ki Ryu
Oxide Electronics Research Team, Electronics and Telecommunications Research Institute, Daejeon 305-700, Republic of Korea

(Received 27 May 2011; accepted 23 June 2011; published online 12 July 2011)

A novel strategy to enhance the bias and illumination stress stability of oxide thin-film transistors (TFTs) is presented. The ultrathin positive charge barrier is employed to block the movement of photo-generated charges toward the interface between gate insulator and semiconductor under negative gate bias and illumination. This method can break through the limitation in stability enhancement caused by the inevitable oxygen vacancy and facilitates the fabrication of highly stable oxide TFTs at low process temperature. © *2011 American Institute of Physics*. [doi:10.1063/1.3610476]

Recently, oxide thin film transistors (TFTs) have been attracted tremendous interests as backplane technology for next generation displays such as large active matrix organic light emitting diode (AMOLED) display, flexible displays in various display modes, etc.[1,2] For the application of oxide TFTs as backplanes of such display modes, high operational stability should be guaranteed. Needless to say, process optimization to achieve fine quality gate insulator (GI), oxide semiconductor films, and interface between them is prerequisite for the high stability.[3] With efforts toward the well-made devices, discovery of ambient effects, such as adsorptions of oxygen or water on the active layer which aggravate instability of oxide TFTs, is the one of the most significant advance in brief history of study on the reliability issues of oxide TFTs.[4] Fortunately, dense passivation layers made of SiO_2, Al_2O_3, etc. eliminate these environmental effects and allow oxide TFTs to operate very stably under bias, current and temperature stress in the absence of incident light.[5]

However, it has been turned out that negative gate bias stress and simultaneous illumination cause huge threshold voltage shift to negative direction even the device is highly stable in the dark state.[6] In most display modes, switching TFTs are negatively biased to keep the off-state and exposed to the light from the various sources such as backlight of LCD, OLED itself, daylight for transparent display and so on. This condition is called negative bias illumination stress (NBIS). Thus, the instability induced by NBIS must be resolved to ensure proper operation of display modes.

Since the first report on this NBIS issue by Shin *et al*., underlying mechanism has considerably been studied. The negative shift of threshold voltage under NBIS has commonly been attributed to the accumulation of photo-generated holes at the GI/semiconductor interface in the reported articles.[7,8] Notably, even sub-band light can bring negative bias instability due to the fully occupied sub-gap states near the valence band maximum. They effectively reduce the band gap and make oxide semiconductors response to sub-band light. These sub-gap states were originated from oxygen vacancy (V_O) according to first principle studies[9–11] and experimental observations.[12] They can be photo-excited from V_O to V_O^{1+} or V_O^{2+}. These ionized oxygen vacancies will be neutralized to V_O via the subsequent photo-excitation of electrons from the valence band and leave the free holes in there, or will keep the holes by themselves (V_O^{1+} or V_O^{2+}) as depicted in Figure 1. These are the sources of positive charges which cause the negative shift of turn-on voltage (V_{ON}, corresponding to the gate voltage that brings 10 pA of drain current with 10 V of drain voltage).[13–17] Therefore, reduction of their amount and migration to the GI/semiconductor interface is the key to improve the bias illumination stability of oxide TFTs.

In this context, we can suggest three strategies to improve the stability under NBIS motivated by the idea that oxygen vacancy is the immediate cause. The first one is the reduction of active layer thickness, which can be done simply to diminish the total amount of oxygen vacancy. The next one is lowering the defect concentration related to oxygen deficiency by adding elements which have high oxygen bond-ability or by post treatments to supply oxygen. Lastly, the insertion of ultrathin positive charge barrier (UPB) into the active material is presented in this letter.

The reduction of active thickness could be a very effective way if one only considers the stability under NBIS condition. Indeed, by simply reducing the active thickness from 20 nm to 5 nm, V_{ON} shift by NBIS decreased drastically as shown in Figures 2(a)–2(c). This is an obvious result, because the total amount of oxygen vacancy decreased with reduced active layer thickness. This might be straight clue that the stability under NBIS strongly depends on the active bulk properties. However, very unfortunately, the positive bias stability became worse and worse as the active thickness decreased as shown in Figures 3(a)–3(c). This is due to the increased charge density under accumulation gate voltage with decreased active thickness and therefore the steeper surface band-bending in case of thinner active layer. Then, the much more electrons will be trapped and cause larger positive shift of V_{ON}. The positive shift of V_{ON} results reduced output drain current and non-uniformity in V_{ON}, leading to serious problems in applications. For example, decrease in luminance of OLED pixel, image sticking problem, etc. Therefore, the thinned active layer is not a good choice when consider bipolar stability.

Second strategy, i.e., lowering the defect concentration related to oxygen deficiency is the direct way to improve stability under NBIS condition according to the studies on the instability mechanism. Park *et al*. reported highly stable device by adopting Hf incorporated In-Zn-O (HIZO) active material.[18] Similarly, Zr

[a]Author to whom correspondence should be addressed. Electronic mail: fullchan@etri.re.kr.

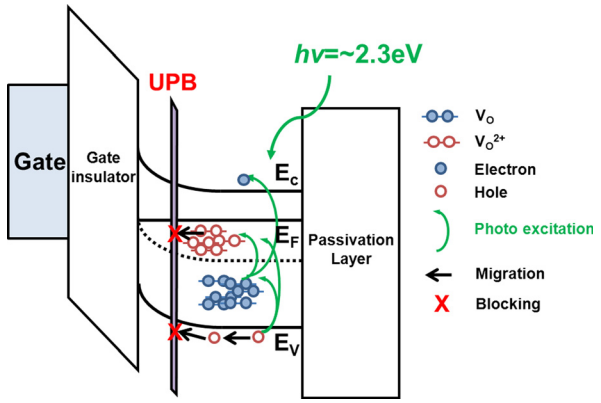

FIG. 1. (Color online) The schematic band diagram under negative bias stress with illumination.

incorporated Zn-Sn-O (ZTZO) was presented by Yang *et al.*[16] They suggested that strong bond-abilities of Hf and Zr with oxygen reduce the oxygen vacancy. Ji *et al.* reported that O_2 high pressure annealing (HPA) can also bring the decrease in oxygen vacancy concentration.[15] However, these defect reduction methods have limitations. Active layers like HIZO or ZTZO become more stable as the contents of adding element increased. However, there is significant mobility expense caused by Hf or Zr incorporation. Meanwhile, HPA might need higher temperature ($\geq$250 °C) to effectively cure the defects although the mobility is not affected considerably. But the most crucial problem for both is that the perfect annihilation of oxygen vacancy is almost impossible due to rather low process temperature to reach the defect free state as long as glass or plastic substrate is used. Thus, there must be a limitation in stability enhancement by adjusting their intrinsic properties.

To break through this limitation, we propose the third strategy, insertion of the UPB into active layer in this communication. We expected the UPB to block the inevitable photo-generated positive charges which move to the GI/semiconductor interface by applied negative bias. In doing so, we tried to achieve highly improved NBIS stability and positive bias stability at the same time unlike the thinned active layer. Furthermore, by adjusting the inserted position of the UPB, we were able to preserve the high mobility of ZnO TFT unlike the Hf or Zr incorporation methods. We believe that one can improve the stability under NBIS condition by inserting the UPB beyond the limit of controlling the intrinsic properties of oxide semiconductors.

To block the photo-generated positive charges, i.e., holes and ionized oxygen vacancies effectively. The UPB must have large valence band offset when stacked with oxide semiconductors to be felt as large injection barrier for holes. Al_2O_3 meets this requirement better than other common insulating materials such as SiO_2, SiN_x, HfO_2, etc. as proven by the first-principle study and experimental observation.[17,19] Moreover, the higher bond energy of Al-O than that of Zn-O is expected to suppress the diffusion of ionized oxygen vacancies toward the GI/semiconductor interface.[20,21]

We fabricated bottom-gated TFTs having 176 nm thick Al_2O_3 GI deposited by atomic layer deposition (ALD) technique and sputtered transparent indium tin oxide (ITO) source/drain and gate electrode in common. The ZnO active layers were grown by plasma-enhanced ALD (PEALD) method. As the reference devices, TFTs with 5, 10, and 20 nm ZnO active layer without the UPB were fabricated. The UPB was inserted by in situ growth of 18 Å thick Al_2O_3 between the depositions of two ZnO layers which were seperated by the UPB. The thickness of underlying ZnO layer determined the inserted position of the UPB and overall thickness of ZnO including the upper one was controlled to 20 nm for all the UPB inserted devices. A precise control of thickness and position of the UPB was possible by virtue of the excellent thickness controllability of ALD on the atomic scale through alternating injections of the sources and reactants. All of the examined devices were passivated by 120 nm thick Al_2O_3 to exclude the ambient effects. Maximum processing temperature did not exceed 200 °C.

The field-effect mobility (μ_{FE}) decreased from 3.3 cm^2/Vs (for the 20 nm thick ZnO TFT without the UPB) to 2.8 cm^2/Vs as the inserted position of the UPB getting closer to the GI/semiconductor interface. This deterioration of transfer properties of the UPB inserted ZnO TFTs can be explained as follows. First, the conductivity of formed channel layer is decreased because insulating Al_2O_3 displaces semiconducting ZnO. Second, electron flow from beyond the UPB to the drain electrode

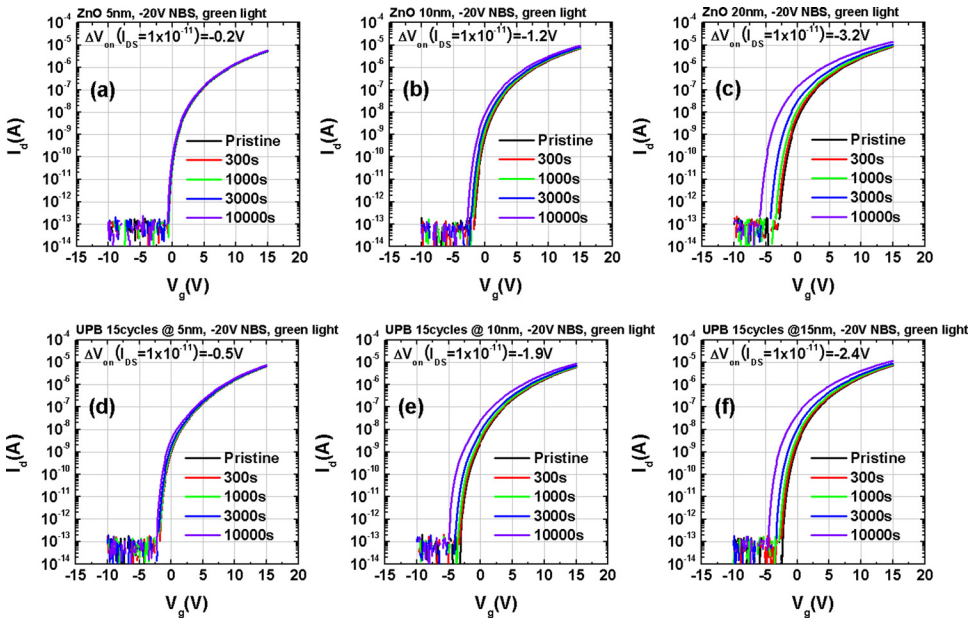

FIG. 2. (Color online) The evolutions of transfer characteristics for the devices without the UPB having (a) 5 nm, (b) 10 nm, and (c) 20 nm thick ZnO layer and those for the devices with the UPB inserted at (d) 5 nm, (e) 10 nm, and (f) 15 nm depth from the GI/semiconductor interface as a function of negative bias illumination stress time.

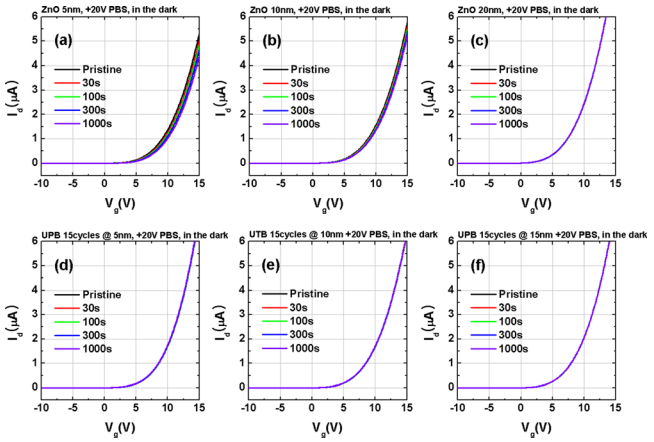

FIG. 3. (Color online) The evolutions of transfer characteristics for the devices without the UPB having (a) 5 nm, (b) 10 nm, and (c) 20 nm thick ZnO layer and those for the devices with the UPB inserted at (d) 5 nm, (e) 10 nm, and (f) 15 nm depth from the GI/semiconductor interface as a function of positive bias stress time.

can be blocked by the UPB. Therefore, we employed "ultrathin (<20 Å)" Al_2O_3 layer to minimize the loss in transfer properties.

For the NBIS test, we shined the green light with a wavelength of 530 nm and an intensity of 1 mW/cm^2 on top of the devices. Active layers of our devices are fully exposed to the light due to transparent ITO gate and source/drain electrodes. Note that this is a very harsh condition compared to the other groups' reports on the NBIS test using devices with light shielding metal gate and source/drain electrodes. Figures 2(d)–2(f) show the evolution of transfer characteristics as a function of the NBIS ($V_{GS} = -20$ V, $V_{DS} = 0$ V) duration for the UPB inserted devices. Also, plots of ΔV_{ON} versus NBIS time of the UPB inserted ZnO TFTs with various inserted positions of the UPB are shown in Figure 4. By insertion of the UPB at depth of 5 nm from the GI/semiconductor interface, V_{ON} shift of 20 nm thick ZnO TFT after 10,000 s under NBIS were decreased from −3.2 V to −0.5 V, which is comparable to that of 5 nm thick ZnO TFT. We believe that the UPB blocks the photo-generated positive charges, which were originated from the rest 15 nm ZnO active layer as depicted in Figure 1. Note that they were also stable under positive bias stress unlike the thinned active layer as shown in Figures 3(d)–3(f). The additional ZnO layer on the UPB is indispensable to ensure positive bias stability because it shares positive gate voltage with ZnO layers under the UPB and therefore

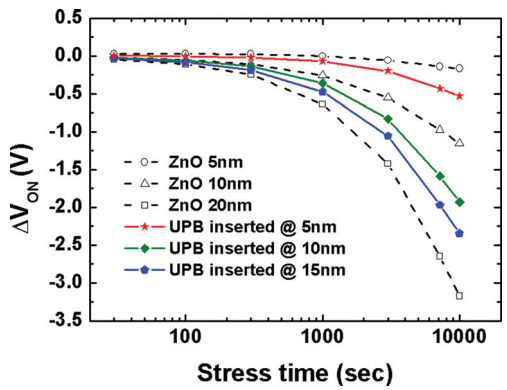

FIG. 4. (Color online) ΔV_{ON} versus NBIS time of the UPB inserted ZnO TFTs with various inserted positions.

prevent the steeper band bending which occurs for thinner active layers. The device, which has the UPB inserted at 5 nm from GI/semiconductor interface, will be a good choice if the NBIS stability is important than any other properties ($\Delta V_{ON} = -0.5$ V, only 15% of the reference) with little expense of μ_{FE}, (2.8 cm^2/Vs, 85% of the reference). Furthermore, at the 15 nm depth, the electrical properties were completely recovered to those of the reference device, still exhibiting better NBIS stability ($\Delta V_{ON} = -2.4$ V) than the typical 20 nm thick ZnO TFT without the UPB.

In summary, a novel strategy to enhance the NBIS stability of oxide TFTs was presented. The UPB was employed to block the movement of photo-generated charges to the GI/semiconductor interface under negative gate bias. By inserting the UPB at close to GI/semiconductor interface, ΔV_{ON} is significantly decreased from −3.2 V to −0.5 V with little expense of μ_{FE} (from 3.3 cm^2/Vs to 2.8 cm^2/Vs). Also, we were able to preserve the original electrical properties of typical ZnO TFT and achieve better NBIS stabilities at the same time by adjusting the inserted position of the UPB. We expect that this method can break through the limitation of stability enhancement caused by the inevitable oxygen vacancy and facilitate the fabrication of highly stable oxide TFTs at low process temperature.

This work was supported by the IT R&D program of ETRI. [Development of core technology for transmittance variable transparent display].

[1]H. D. Kim, J.-S. Park, Y.-G. Mo, and S. S. Kim, International Meeting on Information Display, 35 (2009).
[2]M. Ito, M. Kon, T. Okubo, M. Ishizaki, and N. Sekine, *Proceedings of the International Display Workshop* 2006, p. 663.
[3]S.-H. Ko Park, D.-H. Cho, C.-S. Hwang, S. Yang, M. K. Ryu, C.-W. Byun, S. M. Yoon, W.-S. Cheong, K. I. Cho, and J.-H. Jeon, Electron. Telecommun. Res. Inst. J. **31**, 653 (2009).
[4]J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett. **93**, 123508 (2008).
[5]M. K. Ryu, S. Yang, S.-H. Ko Park, C.-S. Hwang, and J. K. Jeong, Appl. Phys. Lett. **5**, 173508 (2009).
[6]J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. Ko Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee, and H. Y. Chu, Electron. Telecommun. Res. Inst. J. **31**, 62 (2009).
[7]K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, and S. Lee, Appl. Phys. Lett. **95**, 232106 (2009).
[8]K. H. Ji, J.-I. Kim, Y.-G. Mo, J. H. Jeong, S. Yang, C.-S. Hwang, S.-H. Ko Park, M.-K. Ryu, S.-Y. Lee, and J. K. Jeong, IEEE Electron Device Lett. **31**, 1404 (2010).
[9]T. Kamiya, K. Nomura, M. Hirano, and H. Hosono, Phys. Status Solidi A **206**, 860 (2009).
[10]A. Janotti and C. G. Van de Walle, Appl. Phys. Lett. **87**, 122102 (2005).
[11]H. Seo, C.-J. Park, Y.-J. Cho, Y.-B. Kim, and D.-K. Choi, Appl. Phys. Lett. **96**, 232101 (2010).
[12]K. Nomura, T. Kamiya, H. Yanagi, E. Ikenaga, K. Yang, K. Kobayashi, M. Hirano, and H. Hosono, Appl. Phys. Lett. **92**, 202117 (2008).
[13]H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. Ko Park, Appl. Phys. Lett. **97**, 183502 (2010).
[14]H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. Ko Park, Appl. Phys. Lett. **98**, 033504 (2011).
[15]K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, C. S. Hwang, D. Lee, H. Hwang, and J. K. Jeong, Appl. Phys. Lett. **98**, 103509 (2011).
[16]B. S. Yang, M. S. Huh, S. Oh, U. S. Lee, Y. J. Kim, M. S. Oh, J. K. Jeong, C. S. Hwang, and H. J. Kim, Appl. Phys. Lett. **98**, 122110 (2011).
[17]B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, Appl. Phys. Lett. **97**, 022108 (2010).
[18]J. C. Park, S. Kim, S. Kim, C. Kim, I. Song, Y. park, U.-I. Jung, D. H. Kim, and J.-S. Lee, Adv. Mater. **22**, 5512 (2010).
[19]J. H. Kim, U. K. Kim, Y. J. Chung, and C. S. Hwang, Phys. Status Solidi Rapid Res. Lett. **5**, 178 (2011).
[20]D. G. Rethwisch and J. A. Dumesic, Langmuir **2**, 73 (1986).
[21]L. Wang, T. Maxisch, and G. Ceder, Phys. Rev. B. **73**, 195107 (2006).