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Effect of a rapid thermal annealing process on the electrical properties of an aluminum-doped indium zinc tin oxide thin film transistor

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We report the effect of a rapid thermal annealing process (RTP) on the electrical properties of an aluminum-doped indium zinc tin oxide (Al-IZTO) thin film transistor (TFT) with a back-channel etched (BCE) structure. First, the RTP temperatures were varied from 250 to 350 °C, and their effect on Al-IZTO TFT was investigated. The 250 °C RTP produced the best transfer characteristics (subthreshold swing = 0.11 V/dec, hysteresis = −0.25 V, and mobility = 26.42 $cm^2 V^{-1}s^{-1}$), and as the temperature increased, the TFTs showed slightly degraded properties in hysteresis and subthreshold swing. Through the transmission line method (TLM), the channel shortening effect and contact properties according to the annealing temperature were studied. The reliability against a negative gate bias stress under illumination (NBIS) was also analyzed. At high RTP temperature (>300 °C), stability under NBIS was considerably improved, and the 350 °C RTP device showed turn-on voltage shift of −1.7 V. The microwave photoconductivity decay (μ-PCD) method revealed that the RTP effectively reduced shallow localized states, which enhanced the NBIS stability at high temperature. Finally, the RTP was compared with the conventional furnace process at the same temperature in terms of transfer characteristics and uniformity. Even with a much shorter process time for the RTP, Al-IZTO TFTs exhibited similar or better transfer properties and uniformity to or than the furnace annealing.

1 Introduction Amorphous oxide semiconductors (AOSs) have been intensively researched for their use in switching and driving thin film transistors (TFTs) thanks to their excellent properties, such as high mobility, low off-current, and large area processibility. After the first AOS TFT using a-IGZO was reported by Hosono group in 2004 [1], various AOSs including a-IZO, a-ZTO, and a-IZTO were investigated [2–4]. In addition, to achieve high performance oxide TFTs, different approaches by modifications of active channel structure such as double-channel and vertical-channel were also developed [5, 6].

The most simple and effective method to improve the properties of oxide TFTs is post-treatment. In many studies, plasma treatment utilizing N_2O-plamsa [7, 8], O_2 plasma [9, 10], and Ar plasma [11, 12] and post-annealing [13–16] resulted in the improvement of electrical properties such as mobility as well as reliability owing to the reduction of interface and bulk defects. For the post-annealing process, the devices are thermally annealed at a temperature above 250 °C in a vacuum, N_2, or air conditions. During such an annealing process, thermal energy activates and stimulates structural recovery and relaxation of chemical bonds,

resulting in densification of the film [16]. Additionally, recent studies revealed that thermal annealing could effectively diminish trap sites in the channel region [17, 18], resulting in the improvement of stability under gate bias stress. In addition to the traditional thermal annealing, some interesting methods such as wet annealing [19], wet O_2 annealing [18], and high-pressure annealing [20] were also introduced to compare the annealing effects scrupulously.

In general, the thermal annealing process is performed using a furnace or an oven, which takes a long time due to the slow heating/cooling rate and long annealing time. This gives rise to some disadvantages, such as a high thermal budget and long manufacturing period. In addition, as the size of the substrate becomes larger and the mobility of the TFT increases, the problem of temperature uniformity comes up. To solve such side effects, alternative annealing methods have been adopted for fabricated oxide TFTs: rapid-thermal annealing process (RTP) [15, 21] and microwave annealing [22], and pulse UV light annealing [23]. Among them, the RTP is a promising technique due to its intrinsic advantages, including short process time and precise control of the heating/cooling rate and temperature. Notwithstanding frequent uses of the RTP in many studies, however, there have only been a few studies on the effect of RTP on the electrical properties and uniformity of oxide TFTs.

In this work, we investigated the effect of RTP on the electrical properties of high mobility aluminum-doped indium zinc tin oxide (Al-IZTO) TFTs. Al-IZTO TFTs with a back-channel etched (BCE) structure were prepared, and they were annealed using the RTP at various temperatures (250–350 °C). We studied the electrical performances, including the transfer characteristics, channel shortening effect, contact properties, and stability under negative bias illumination stress (NBIS).

2 Experimental The oxide thin film transistors with a BCE structure were fabricated (inset in Fig. 1(a)). The Mo gate electrode (150 nm) was deposited by sputtering on a glass substrate and patterned. For the gate insulator, a SiO_2 layer with a thickness of 200 nm was formed by a plasma-enhanced chemical vapor deposition (PE-CVD) method at temperature of 380 °C. Then, active layer deposition of Al-doped In-Zn-Sn-O (Al-IZTO) was performed by RF sputtering with a Ar/O_2 gas ratio of 8:2. The thickness of the Al-IZTO layer was set at 30 nm. The 150 nm-thick Mo was sputtered for the source/drain electrode and patterned after active patterning. Then, the SiO_2 was deposited by PE-CVD with a thickness of 200 nm for the passivation of the TFT. Before the deposition of the passivation film, the back channel of the Al-IZTO layer was treated by N_2O plasma to control the conductivity of the active layer. The fabricated Al-IZTO BCE TFTs were annealed using RTP equipment (KORONATM L2-RTP, AP systems) at various temperatures (250–350 °C) in air. To minimize the thermal stress during the RTP, the heating process was divided into two steps: fast-up and slow-up. During the fast-up step, the temperature was increased with a heating rate of 2 °C s^{-1}. For the slow-up step, the samples were heated to the target temperature with a heating rate of 1 °C s^{-1}. Then, the temperature was held for 1200 s.

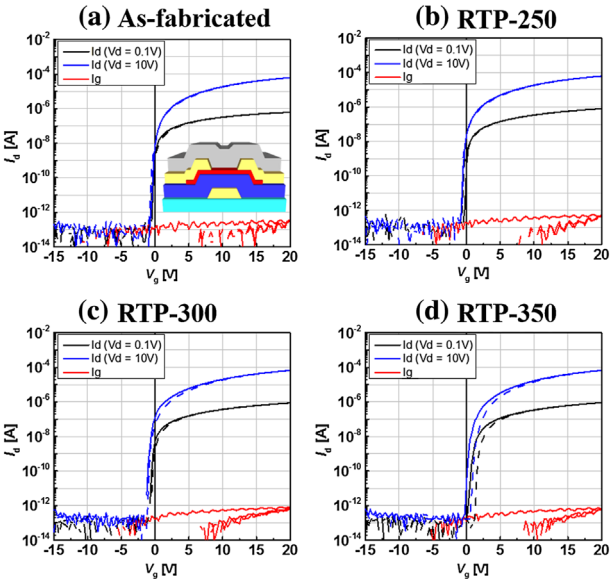


Figure 1 The transfer curves of the Al-IZTO TFTs (a) before annealing and after RTP at (b) 250 °C, (c) 300 °C, and (d) 350 °C ($V_d = 0.1$ and 10 V). The inset in (a) shows a schematic diagram of a fabricated back-channel etched TFT structure. The channel width and length were 10 and 10 μm, respectively.

The electrical properties of the TFTs were analyzed by an Agilent B1500A semiconductor parameter analyzer with a 3-tips probe station. The field-effect mobility (μ_{FE}) was extracted in the linear region using the following equation:

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{ds}}, \quad (1)$$

where W and L are the channel width and length, respectively. C_i is the capacitance of gate insulator per unit area and V_{ds} is 0.1 V. The g_m is the transconductance at a low drain voltage and defined as $\partial I_{ds}/\partial V_{gs}$. The turn-on voltage ($V_{on}$) is defined as the gate voltage that corresponds to a drain current of $W/L \times 10$ pA. The microwave photoconductivity decay (μ-PCD, KOBELCO) method was used to analyze the annealing effect on the Al-IZTO film.

3 Results and discussion High mobility BCE structured oxide TFTs are very important to realize large-sized high resolution TFT-LCD. The transfer curves of the as-fabricated and RTP-annealed at 250, 300, and 350 °C Al-IZTO BCE TFTs (RTP-250, 300, and 350, respectively) are shown in Fig. 1. Their electrical characteristics are summarized in Table 1. The measured channel width/length was 10 μm/10 μm. The mobility values were obtained

Table 1 Summary of electrical properties of the transfer curve, effective channel length, and contact resistance of the Al-IZTO TFTs before and after the RTP annealing.

sample	SS (V/dec)	V_{on} (V)	hysteresis (V) @$V_{ds} = 0.1$ V	$\mu_{FE,\ Eff}$[a] ($cm^2 V^{-1}s^{-1}$)	ΔL (μm)	R_C (Ω cm)
as-fabricated	0.11	−0.5	−0.25	17.53	0.6	50.7
RTP-250 °C	0.11	−0.25	−0.25	26.42	1.14	5.2
RTP-300 °C	0.13	−0.75	0.25	26.11	1.87	5.1
RTP-350 °C	0.20	0.25	1	25.24	3.4	13.1

[a]Mobility extracted using the effective channel length (L_{Eff}).

using the effective channel length in consideration of the channel shortening effect. All TFTs showed good transfer behavior with an on/off ratio of 10^7 at $I_{DS} = 0.1$ V. By virtue of the optimized fabrication process, even the as-fabricated Al-IZTO TFT had a small hysteresis of −0.25 V, subthreshold swing (SS) of 0.11 V/dec, and mobility of 17.53 $cm^2 V^{-1}s^{-1}$. When the RTP was carried out at 250 °C, the device exhibited much improved mobility of 26.42 $cm^2 V^{-1}s^{-1}$, while the other factors, such as SS, V_{on}, and hysteresis, were kept on similar levels. Such enhancement of mobility was mainly attributed to the reduction of the defects in the interface [16, 17].

In contrast, at higher temperatures of 300 and 350 °C, the Al-IZTO TFT showed slightly deteriorated transfer curves. The RTP-300 exhibited an SS of 0.13 V/dec, a hysteresis of 0.25 V, and a mobility of 26.11 $cm^2 V^{-1}s^{-1}$. After the 350 °C RTP, the SS, hysteresis, and mobility were 0.2 V/dec, 1 V, and 25.24 $cm^2 V^{-1}s^{-1}$, respectively. While the mobility was comparable among the devices, the SS and hysteresis slightly deteriorated as the annealing temperature increased. This may have originated from stress during the rapid heating process. It is known that some mechanical stress of films could be generated during RTP annealing [24]. In addition, a rapid increase to high temperature also induces high thermal budget in films [25]. Such stress could generate defects in the active layer, inducing deteriorated SS and hysteresis [22, 26]. Furthermore, reactive oxygen supplied to the back channel of Al-IZTO during N_2O plasma treatment at 300 °C could diffuse to the active bulk region during 350 °C RTP. This interstitial oxygen is well known as a charge trapping source, which causes higher SS and hysteresis [27]. Although the main purpose of N_2O plasma treatment is to suppress back channel leakage current, excess N_2O plasma treatment could yield worse TFT performance after the annealing process.

In oxide TFTs, channel shortening generally occurs, which results in a shorter effective length (L_{Eff}) than the photo-mask pattern-size (L_{Mask}). Here, L_{Eff} means the length of the actual channel where charge carriers flow through an oxide semiconductor between the source and drain electrodes. Since defining an accurate channel length is critical to designing and evaluating oxide TFTs, the channel shortening effect should be carefully considered. The channel shortening mainly occurs during the thermal process, therefore, it is important to confirm the effect of RTP on channel shortening in oxide TFTs.

To expose the channel shortening effect of RTP on the Al-IZTO TFTs, a transmission-line method (TLM) was employed [28–30]. The total resistance (R_{Tot}) can be determined in the linear region as a function of the channel resistance (R_{CH}) and source/drain contact resistance (R_C):

$$R_{Tot} = R_{CH} + R_C,$$

$$R_{Tot} \cdot W = \frac{L_{Mask} - \Delta L}{\mu_{FE} \cdot C_{ox} \cdot \left(V_{gs} - V_{th} - \frac{1}{2}V_{ds}\right)} + R_C \cdot W, \quad (2)$$

where W and L_{Mask} are the optically measured channel width and length, respectively, ΔL is the reduced length of the channel, and C_{ox} is the unit area capacitance of the dielectric. For the devices with various widths and lengths, the reduction of the channel length (ΔL) was extracted by plotting $R_{Tot} \times W$ as a function of channel length (L) at different gate voltages. To perform the TLM analysis, we measured the transfer curves with various W/L values (5/5, 6/6, 8/8, 10/10, 20/20, and 40/40 μm) in the linear region. All the devices showed clear transfer characteristics at the various W/L values. Then, using Eq. (2), we calculated the width-normalized total resistances as plotted in Fig. 2 as a function of the channel length. The corresponding linear fitted lines are also indicated as solid lines. The x- and y-coordination of the intersection between the fitted lines indicate the reduced channel length (ΔL) and contact resistance (R_C), separately. The summaries of ΔL and R_C are listed in Table 1.

The as-fabricated TFT showed ΔL of 0.6 μm even though they were not annealed. We considered that this occurred during the deposition process of the passivation layer (SiO_2) at a temperature of 300 °C. After the RTP, the reductions in the channel length of the RTP-250, RTP-300, and RTP-350 were 1.14, 1.87, and 3.4 μm, respectively. We expect that this greater ΔL originated from the diffusion of Mo into the active contact region during the post-annealing [31, 32]. The driving force of such diffusion is related to thermal budget; therefore, as the RTP temperature increases, more channel shortening is observed with an

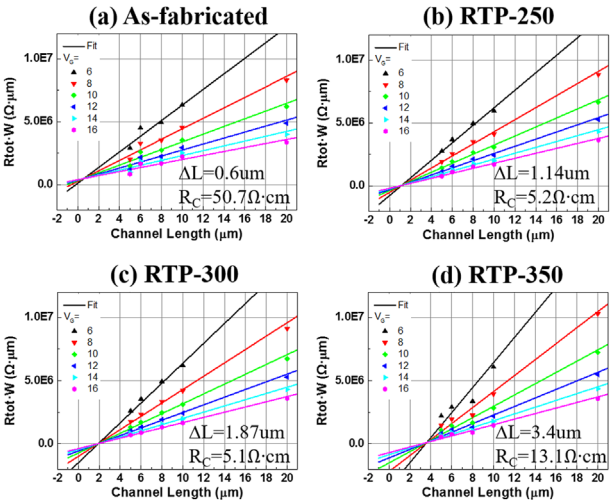


Figure 2 Plots of the width normalized total resistance (R_{Tot} W) as a function of channel length (L) for the devices (a) before annealing and after RTP at (b) 250 °C, (c) 300 °C, and (d) 350 °C. The plots were performed at different gate voltages (6, 8, 10, 12, 14, and 16 V). The linear-fitted results are indicated as solid lines.

increased ΔL. In addition, in the RTP-350, ΔL increased dramatically compared with the RTP-300. This is possibly due to oxidization of Mo and formation of an oxygen deficiency region, which resulted in elongation of the conductive region. To extract the precise mobility of the Al-IZTO TFTs, the effective channel length (L_{Eff}) was obtained from L_{Mask}-ΔL, where the L_{Mask} was the optically measured pattern length. In this work, the L_{Mask} for the 10 μm-size pattern was 10.52 μm. When the mobility was calculated using $L_{Mask} = 10.52$ μm without considering the channel shortening effect, as-fabricated, RTP-250, RTP-300, and RTP-350 devices had mobilities of 18.6, 29.63, 31.75, and 37.3 $cm^2 V^{-1}s^{-1}$, respectively. However, these values were re-calculated to 17.53, 26.42, 26.11, and 25.24 $cm^2 V^{-1}s^{-1}$ using a L_{Eff} of 9.92, 9.38, 8.65, and 7.12 μm for the as-fabricated, RTP-250, RTP-300, and RTP-350 devices, respectively. This result suggests that it is meaningful to consider the channel shortening effect during mobility extraction, especially in the case of the TFT annealed at high temperatures.

Generally, the mobility of oxide TFTs increased further in higher temperature annealing because of better defect curing and incorporation of hydrogen [17, 33]. In our study, however, the Al-IZTO TFT showed a similar mobility regardless of the annealing temperature in the range of 250–350 °C. To clarify this result, we examined the contact property between the S/D electrode and active layer. The R_C critically affects the electrical properties of the oxide TFT, and a high R_C induces a low turn-on current and decreased mobility of TFTs [15, 32]. The as-fabricated device had a very high R_C of 50.7 Ω cm. After the RTP annealing, however, the R_C was decreased, with R_C of 5.2, 5.1, and 13.1 Ω cm for the RTP-250, RTP-300, and RTP-350, respectively. The reduction of R_C was related to the improvement of the contact region between the S/D electrode and active layer due to the thermal energy [15, 34]. Interestingly, the R_C of the RTP-350 increased to 13.1 from 5.1 Ω cm (RTP-300). As discussed above, this time, formation of MoO_x at the contact area after high temperature annealing at 350 °C would induce a relatively higher contact resistance. The increase of R_C caused degradation of mobility after RTP at 350 °C.

To confirm the effect of RTP on the reliability of the Al-IZTO TFTs, we measured the stability under negative gate bias stress with illumination (NBIS), and the transfer behaviors are displayed in Fig. 3. A negative gate bias of −20 V ($V_g = -1.0$ MV/cm) with illumination of 0.5 mW cm^{-2} was applied for 10000 s. We measured the transfer curves just before and after 10000 s to avoid the compensation effect during measurement of the transfer curve in mid-time. The result indicated that the RTP annealing effectively improved the NBIS stability, especially at a high annealing temperature. Compared to the as-fabricated device with a ΔV of −7.2 V, the RTP-300 and RTP-350 showed much better stability, with ΔV_{on} of −4.9 and −1.7 V, respectively. In addition to the V_{on} shift, the change in SS after NBIS was negligible in the RTP-350 compared to other devices. In the as-fabricated, RTP-250, and RTP-300 devices, SS values were degraded to 0.24, 0.3, and 0.36 V/dec, respectively, after NBIS. In those devices, a hump phenomenon in the subthreshold region also occurred. In contrast, the RTP-350 showed only a little change in SS during NBIS ($SS_{before} = 0.2$V/dec and $SS_{after} = 0.22$ V/dec) with no hump formation. According to the previous studies, the instability during NBIS can

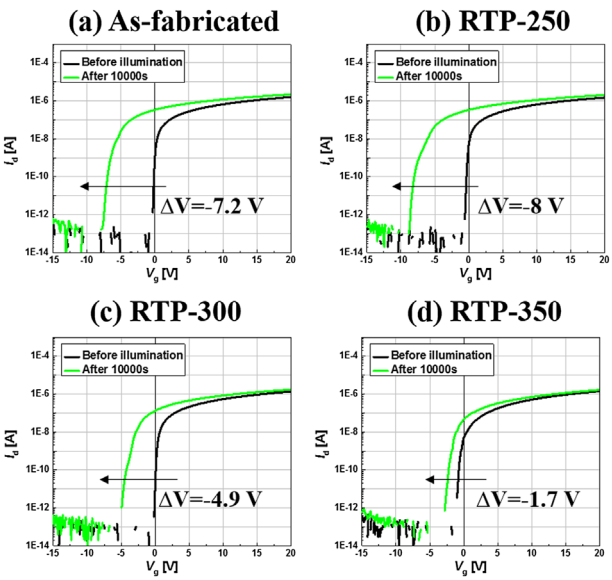


Figure 3 Transfer curves before and after negative gate bias stress with illumination (NBIS, $V_g = -1.0$ MV/cm, illumination of 0.5 mW cm^{-2}) of the Al-IZTO TFTs (a) before and after RTP annealing at (b) 250 °C, (c) 300 °C, and (d) 350 °C. The channel width/length was 40/20 μm.

be attributed to the donor-like defect states below the conduction-band minimum (CBM) [35, 36]. These states also degraded the SS characteristics and formed the hump [37–39]. This result indicates that the RTP at high temperature (>300 °C) effectively reduced donor-like defects related to the oxygen deficiency of Al-IZTO film and improved stability against NBIS.

For further investigation of such improvement on NBIS stability, the μ-PCD method was employed. The μ-PCD measurement is a very useful method to estimate mobility and defect-like states in an oxide semiconductor film. In the μ-PCD analysis, after photo-excitation, the density of the carriers obey the following equation [40, 41]:

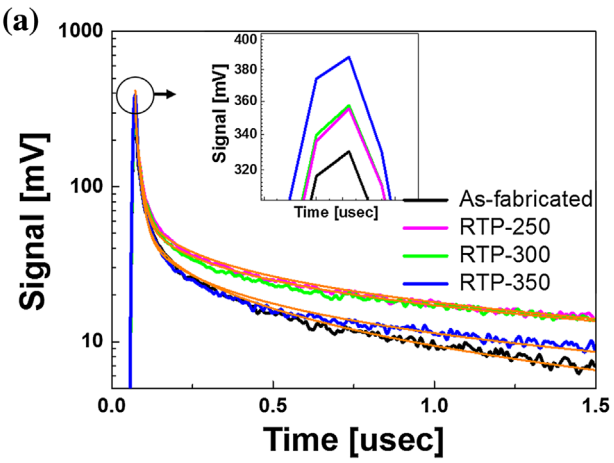
$$n(t) = n_0\left\{\exp\left(-\frac{t}{\tau_1}\right) + \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta}\right]\right\}, \qquad (3)$$

where n_0 is the carrier density just after photo-excitation, τ_1 and τ_2 are the fast and slow decay constants, respectively, and β is the stretching exponent. Just after photo-excitation, the peak value is indicated, and it is closely correlated with the mobility of the oxide film [42]. The term of slow decay (τ_2) is mainly dominated by the re-emission rate of the trapped carriers, serving information of shallow localized states [41]. For the sample of μ-PCD measurement, a mimicked sample of SiO_2/Al-IZTO/SiO_2 on glass substrate was prepared and annealed under the same conditions as the devices.

The photoconductivity responses, fitted curves using Eq. (3), and a summary of the main parameters from μ-PCD measurement are indicated in Fig. 4. The peak of μ-PCD results according to RTP temperatures showed a higher value with a higher temperature. This result suggests that RTP can reduce sub-gap states in Al-IZTO film and increase mobility of Al-IZTO TFTs. The TFT annealed at 350 °C, however, showed a similarly effective mobility as the ones annealed at 250 and 300 °C due to the increased R_C of RTP-350, as discussed above.

The result of slow decay showed a clear correlation between ΔV under NBIS and a value of τ_2. The τ_2 value of the as-fabricated sample was 17.5 ns, and it increased to 22.2 ns after the 250 °C annealing. Then, the τ_2 value sharply decreased to 16.2 and 5.9 ns for the RTP-300 and RTP-350 sample, respectively. These values of τ_2 directly corresponded to the results of NBIS. Considering the meaning of slow decay (τ_2), which represents the shallow localized states just below CBM, the improvement of NBIS through the RTP annealing mainly stems from the elimination of shallow localized states [41].

Finally, the effect of RTP on the electrical properties of Al-IZTO TFTs is compared with conventional furnace annealing at the same temperature. Based on the results of the transfer curves according to the RTP temperature (Fig. 1 and Table 1), we chose a temperature of 250 °C, which resulted in smaller SS and hysteresis. Figure 5(a) indicates the schematic comparison between the annealing processes



(b)

sample	peak (mV)	τ_2 (ns)
as-fabricated	330	17.5
RTP - 250	357	22.2
RTP - 300	359	16.2
RTP - 350	388	5.9

Figure 4 (a) Photoconductivity responses for the as-fabricated and RTP-annealed samples as a function of the annealing temperature. The inset depicts an enlarged view of the peak region. The fitted curves are indicated as orange solid lines. (b) Summary of main parameters from μ-PCD measurement.

using RTP and a furnace. In general, in the furnace process it takes a long time to increase the temperature and needs a long annealing time. In this work, the furnace annealing took 3000 s to reach the target temperature of 250 °C. Then, we annealed the devices for 7200 s to get a sufficient effect of furnace annealing. In other words, the total duration was about 10200 s. In contrast, the total duration for the RTP sample was only 1350 s (the sum of the heating and annealing steps) because the heating speed of the RTP system was very fast. In addition, since it can be precisely controlled, the heating step is divided into fast-up (a heating rate of 2 °C s) and slow-up (a heating rate of 1 °C/s), as described in Section 2.

To evaluate the electrical properties and their uniformity, we fabricated Al-IZTO TFTs on glass wafers with a 6-inch size and measured 32 different points with a short width/length of 5/5 μm, as depicted in Fig. 5(b). Uniformity is the most important factor in the mass-production industry, and it is known that uniformity as well as electrical properties can be improved through the annealing process. To confirm this annealing effect, the distributions of transfer characteristics in terms of V_{on}, SS, mobility, and hysteresis are displayed as a percent plot. Their electrical properties in terms of the average value and standard deviation (σ) are also listed in Fig. 5(c)–(f). It is clear that both furnace and RTP annealing improved uniformity for all parameters. The as-fabricated TFTs showed large non-uniformity with a big

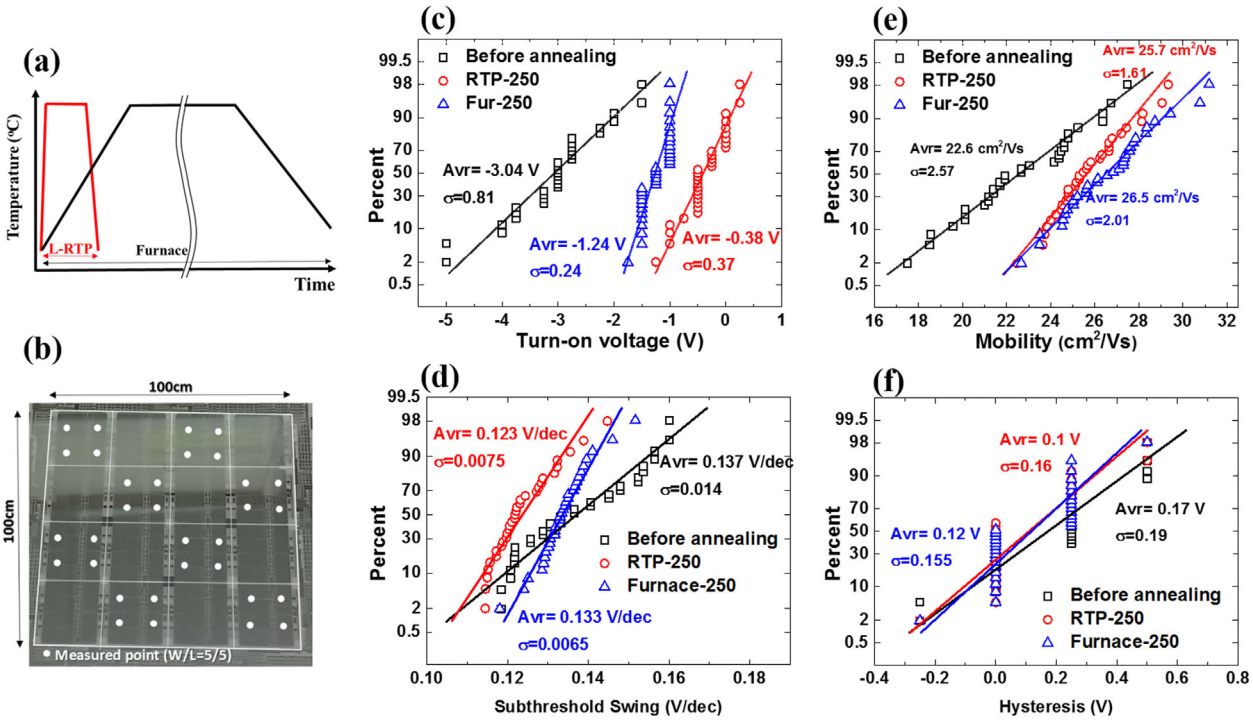


Figure 5 (a) Schematic diagram of the annealing process using the RTP (red) and furnace (black) equipment according to annealing time. (b) Image of the fabricated Al-IZTO TFTs on glass substrate with a size of $100 \times 100\,cm^2$ for the uniformity test. White dots indicate measured points with a *W*/*L* of 5/5 μm. Uniformity plots for (c) turn-on voltage (V_{on}), (d) subthreshold swing (SS), (e) mobility, and (f) hysteresis of TFTs before annealing and after RTP and furnace annealing at 250 °C.

standard deviation (σ) value showing V_{on} (-3.04 ± 0.81 V), SS (0.137 ± 0.014 V/dec), mobility ($24 \pm 2.27\,cm^2\,V^{-1}s^{-1}$), and hysteresis ($0.17 \pm 0.19$ V). After the annealing process using a furnace at 250 °C for 2 h, the TFTs exhibited not only improved uniformity with a small σ value, but also improved transfer properties, V_{on}, SS, mobility, and hysteresis of -1.24 V, 0.133 V/dec, $26.5\,cm^2\,V^{-1}s^{-1}$, and 0.12 V, respectively, on average. On the other hand, in the same manner, after RTP at 250 °C, all parameters showed more uniform distribution compared with those of the as-fabricated TFTs. The RTP annealed devices exhibited V_{on}, SS, mobility, and hysteresis of -0.38 ± 0.37 V, 0.123 ± 0.0075 V/dec, $25.7 \pm 1.61\,cm^2\,V^{-1}s^{-1}$, and 0.1 ± 0.16 V, respectively. Some parameters, such as SS and V_{on} had better properties than the furnace annealing even with much shorter process time of RTP annealing. This means that the RTP produces more effective and efficient annealing than furnace annealing. In addition, it should be noted that the value of SS of the RTP-device exhibited a much smaller value than that of the furnace sample. It is known that the SS value is closely related to the total trap density (N_{Tot}) in the bulk of the channel layer and at active/gate insulator interface, which is expressed by following equation: $SS = qk_BT(N_{SS}t_{ch} + D_{it})/C_i\log(e)$, where q is the electron charge, k_B is the Boltzmann constant, T is the absolute temperature, t_{ch} is the channel layer thickness, N_{SS} is the total trap density in the bulk region of the channel layer, and D_{it} is the total trap density at the active/gate insulator interface [3, 43]. The calculated values of N_{Tot}, (here N_{Tot} denotes overall trap density in the region of bulk and interface including terms of N_{SS} and D_{it}), were 2.31×10^{11}, 2.25×10^{11}, and $2.08 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for the as-fabricated, furnace and the RTP-annealed device. This result suggests that even with shorter process time, the RTP can eliminate the sub-gap state of the Al-IZTO layer in better way than furnace annealing.

4 Conclusions In this work, we studied the effect of annealing using RTP on electrical properties of the Al-IZTO TFTs. After the RTP, all TFTs exhibited increased mobility. The 250 °C-annealed TFT had the best properties, and as the annealing temperature increased above 250 °C, the Al-IZTO TFT showed slightly degraded properties in SS and hysteresis. The TLM results showed that the channel shortening effect became dominant at a higher than 250 °C annealing temperature. In addition, RTP effectively reduced the contact resistance between the source/drain electrode and the active layer. The reliability under NBIS was much improved after RTP at >300 °C. The μ-PCD measurement revealed that such improvement on NBIS was due to reduced shallow localized states after RTP annealing. Finally, the effects of RTP and furnace annealing were compared in terms of transfer properties and uniformity. Even with the much shorter process time of RTP, the RTP-treated TFTs showed competitive or superior properties and uniformity to those annealed by furnace, which confirmed

that the RTP system is a more efficient and effective annealing method than a furnace method.

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