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# The effects of buffer layers on the performance and stability of flexible InGaZnO thin film transistors on polyimide substrates

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We demonstrated the fabrication of flexible amorphous indium gallium zinc oxide thin-film transistors (TFTs) on high-temperature polyimide (PI) substrates, which were debonded from the carrier glass after TFT fabrication. The application of appropriate buffer layers on the PI substrates affected the TFT performance and stability. The adoption of the $SiN_x/AlO_x$ buffer layers as water and hydrogen diffusion barriers significantly improved the device performance and stability against the thermal annealing and negative bias stress, compared to single $SiN_x$ or $SiO_x$ buffer layers. The substrates could be bent down to a radius of curvature of 15 mm and the devices remained normally functional. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4864617]

Recently, active matrix organic light-emitting diode (AMOLED) displays have attracted more attention than active matrix liquid crystal displays (AMLCDs) because they are faster, thinner, lighter, and more power efficient than AMLCDs. Glass has been widely used as the substrate for AMOLEDs due to its advantages of transparency and stability. However, its critical disadvantages such as excessive fragility and heaviness necessitate its replacement with new substrates such as plastic or metal foils, which can be used to fabricate displays that are much thinner, lighter, and unbreakable.[1–3]

Some researchers have demonstrated flexible AMOLED displays with various types of thin film transistors (TFTs).[2–5] In particular, many groups have reported the fabrication of TFTs on flexible substrates using amorphous indium-gallium-zinc oxide (a-IGZO) as an active channel.[5–12] The TFTs showed surprisingly high field effect mobility ($>\sim 10\ cm^2/Vs$) and on/off ratio even for amorphous oxide semiconductors deposited near room temperature, compared with conventional amorphous silicon and organic semiconductors.[6]

However, in order to realize flexible AMOLED backplanes, the most critical issues are found in the flexible substrate materials and device structures, which enable compatibility with existing TFT fabrication facilities and the long-term operational stability. Even though metal foil substrates have high process temperatures due to its high melting temperature (e.g., 1400 °C for stainless steel) and excellent diffusion barrier properties against moisture and oxygen, a large coefficient of thermal expansion [CTE; SUS 304 (∼18 ppm/K) compared to non-alkali glass (∼3 ppm/K)] resulting in severe bending problems, poor surface roughness which requires expensive chemical mechanical polishing (CMP), large parasitic capacitance, and difficult particle-free handling still need to be resolved.[4,5,7]

This work reports the electrical performance and stability of a-IGZO TFTs with a top-gate structure, fabricated on flexible polyimide (PI) substrates, which have merits of high glass transition temperature (∼360 °C) and low CTE (∼3.4 ppm/K) properties. In particular, in order to suppress the moisture diffusion from the PI which acts as a water reservoir,[13,14] we investigated the effect of diffusion barrier layers including $SiO_x$, $SiN_x$, and $SiN_x/AlO_x$ structures between the a-IGZO layer and PI substrate. It is found that the appropriate combination of $SiN_x$ and $Al_2O_3$ as a barrier stack results in the optimum device properties and stability.

The schematic diagram of flexible and top-gate a-IGZO TFT on PI is shown in Fig. 1. The PI film with about 20 $\mu$m thickness was coated onto the carrier glass (alkali-free glass with the thickness of 0.7 mm) and then baked at 300 °C under an air-ambient. It was kept that way during the entire device fabrication and was separated mechanically from the carrier only when the device formation was completed. The 50 nm thick silicon nitride ($SiN_x$) and silicon oxide ($SiO_x$) buffer films were deposited over entire substrate area by plasma enhanced chemical vapor deposition (PECVD, deposition temperature of 250 °C) as diffusion barriers against ambient atmosphere such as $O_2$ and $H_2O$. In order to reduce the formation of hydrogen related defect in the semiconductor layer originating from the hydrogen-rich $SiN_x$ buffer layer, separate devices were prepared by depositing $AlO_x$ films with the thickness of 10 nm and 100 nm by atomic layer deposition (ALD) onto the $SiN_x$ buffer. Consequently, various buffer layers on PI substrates were prepared: $SiN_x$ 50 nm (Device A), $SiN_x$ 50 nm/$AlO_x$ 10 nm (Device B), $SiN_x$ 50 nm/$AlO_x$ 100 nm (Device C), and $SiO_x$ 50 nm (Device D). As the source/drain (S/D) electrodes, the 100 nm thick InSnO (ITO) film was sputter-deposited on the buffer layer and patterned using conventional photolithography. The

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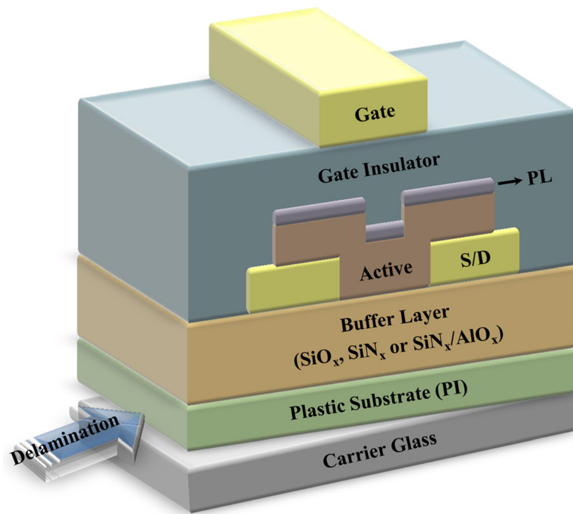


FIG. 1. Schematic of flexible, top-gate a-IGZO TFTs with various buffer layers on the PI substrate.

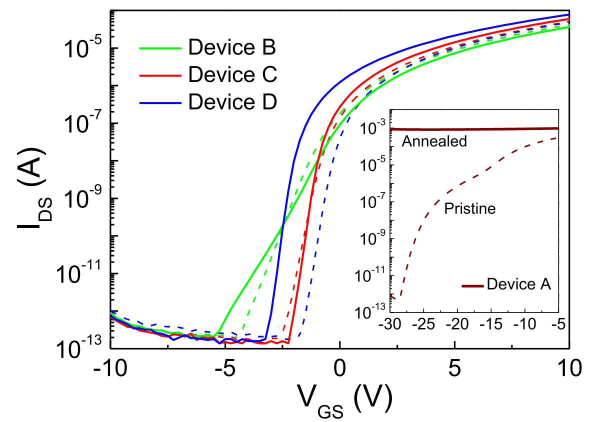


FIG. 2. The typical transfer characteristics of pristine (dashed line) and 250 °C-annealed TFTs (solid line) with various buffer layers of $SiN_x$ 50 nm (Device A; inset), $SiN_x$ 50 nm/$AlO_x$ 10 nm (Device B), $SiN_x$ 50 nm/$AlO_x$ 100 nm (Device C), and $SiO_x$ 50 nm (Device D).

a-IGZO film was deposited by room temperature rf-sputtering with the rf power of 400 W at $O_2/Ar + O_2$ ratio of 20%. A 9 nm thick $AlO_x$ film was then grown as a protection layer (PL) at the temperature of 250 °C by ALD. After patterning IGZO and PL layer using diluted hydrofluoric acid at once, another layer of $AlO_x$ was deposited as the gate dielectric at the temperature of 150 °C by ALD. The contact pad of S/D electrode was opened by wet etching process. Sputtered Mo-Ti alloy was used as a gate electrode and patterned by wet process. The channel width (W) and length (L) of the devices under consideration were 40 $\mu$m and 20 $\mu$m, respectively. The fabricated devices were subjected to thermal annealing at 250 °C for 2 h in air.

The electrical device performance was characterized by HP 4155A semiconductor parameter analyzer. The device stability under negative bias temperature stress (NBTS; $V_{GS}$ was set to $-20$ V at substrate temperature of 60 °C and the stress duration was 3600 s) was analyzed as a function of ambient conditions (i.e., in air with 60% relative humidity). The density of localized gap states (DOS) for a-IGZO TFTs was extracted by Meyer-Neldel (MN) rule method, which was described elsewhere in detail.[15,16]

The representative transfer characteristics of the devices are shown in Figure 2. Several important parameters such as threshold voltage ($V_{th}$), saturation mobility ($\mu_{sat}$), and sub-threshold swing (SS) were extracted based on the gradual channel approximation[17] and are listed in Table I. Device A, which has a single $SiN_x$ buffer, has very poor transfer characteristics with the highly negative $V_{th}$ value of $-24$ V and becomes completely conductive once annealed at 250 °C. It is assumed that the hydrogen related defects that may have diffused from the $SiN_x$ acted as carrier donors.[18,19] Such an effect was observed to be reduced by the insertion of a $AlO_x$ buffer layer between $SiN_x$ and the a-IGZO semiconductor, as shown by devices B and C. Device B exhibits a $\mu_{sat}$ of 13.07 cm$^2$/Vs, SS value of 0.55 V/decade and $V_{th}$ of $-0.69$ V, and from the SS value it can be deduced that hydrogen effects arising from the $SiN_x$ layer still remain compared to device C. The $SiN_x/AlO_x$ stack with a thicker $AlO_x$ layer of 100 nm (device C) results in a higher $\mu_{sat}$ of 14.20 cm$^2$/Vs and lower SS value of 0.3 V/decade. After thermal annealing process at 250 °C in air, a value of $\mu_{sat}$ and SS in device C were slightly improved up to ~14.4 cm$^2$/Vs and ~0.24 V/decade, respectively, whereas, significant degradation in $\mu_{sat}$ and SS occurred in device B, resulting in a $\mu_{sat}$ of 11.75 cm$^2$/Vs and SS value of 0.83 V/decade, respectively. On the other hand, it is noted that there was a high negative shift in $V_{th}$ (~1.5 V) upon annealing in device D, which may be attributed to the higher water permeability of the $SiO_x$ film[20,21] and the donor activation of the water molecules,[22,23] originating from the PI substrate which can act as a reservoir of $H_2O$.[13,14]

TABLE I. Extracted electrical parameters of a-IGZO TFTs and water vapor transmission ratio (WVTR, Mocon Test) results, depending on various buffer layers.

| | Buffer layer/annealing condition | $V_{th}$ (V) | $\mu_{sat}$ (cm$^2$/V s) | SS (V/decade) | WVTR (g/cm$^2$ day) |
|---|---|---|---|---|---|
| TFT parameter and buffer Properties | A (Prinstine) | −23.93 | 3.31 | 0.76 | 0.82 |
| | A (250 °C) | ND | ND | ND | |
| | B (Prinstine) | −0.69 | 13.07 | 0.55 | 0.51 |
| | B (250 °C) | −0.87 | 11.75 | 0.84 | |
| | C (Prinstine) | −0.72 | 14.20 | 0.31 | 0.033 |
| | C (250 °C) | −1.25 | 14.43 | 0.24 | |
| | D (Prinstine) | −0.35 | 14.50 | 0.26 | 1.33 |
| | D (250 °C) | −2.19 | 14.88 | 0.22 | |

A: $SiN_x$ 50 nm, B: $SiN_x$ 50 nm/$AlO_x$ 10nm
C: $SiN_x$ 50 nm/$AlO_x$ 100 nm, D: $SiO_x$ 50 nm

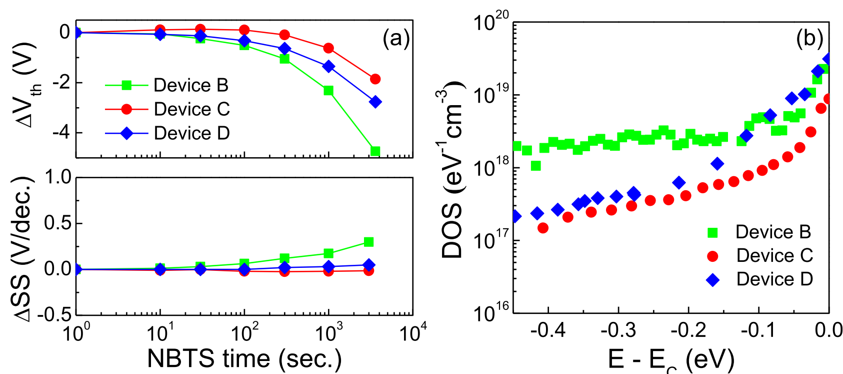


FIG. 3. (a) Threshold voltage shift ($\Delta V_{th}$) and variation ($\Delta SS$) as a function of NBTS time for a-IGZO TFTs with various buffer layers. (b) Extracted DOS distribution as a function of the energy ($E-E_c$) for a-IGZO TFTs with various buffer layers.

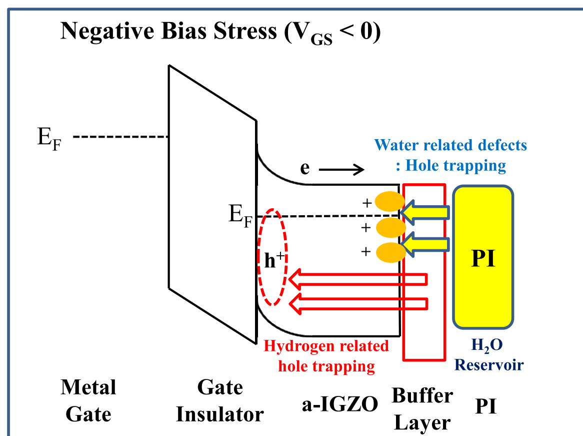


FIG. 4. Schematic energy diagrams of the flexible a-IGZO TFTs on buffered PI substrate under NBTS condition.

Figure 3(a) shows the time dependence of threshold voltage shift ($\Delta V_{th}$) and variation ($\Delta SS$) for a-IGZO TFTs with various buffer layers under negative gate bias ($V_{GS} = -20$ V) and temperature (60 °C) stress. Parallel shifts of $\Delta V_{th}$ occurred for device C ($-1.86$ V) and D ($-2.76$ V) without any degradation in the mobility and SS. However, the considerable changes in $\Delta V_{th}$ ($-4.74$ V) and $\Delta SS$ (0.29) for device B occurred with degradation of the mobility (is not shown, $\Delta\mu_{sat} = -0.71$ cm$^2$/Vs). To understand the origins of TFT instabilities, the following two mechanisms are well known: charge trapping and defect creation.[18,19,24] The charge trapping mechanism would be the possible origin of degradation for devices C and D, since the SS values are not affected significantly. On the other hand, the defect creation mechanism is more appropriate to explain the degradation of device B because there are significant changes in parameters such as $\mu_{sat}$ and SS value. The difference of device degradation mechanism is clearly related to the different barrier layers, which suggest that the appropriate suppression of diffusion from the PI or $SiN_x$ layer is important to obtain devices with good performance and stability.

The sub-bandgap DOS of the TFTs was investigated to understand the different electrical characteristics resulting from various buffer layers, as shown in Figure 3(b). The DOS calculations were performed by experimentally obtained activation energy ($E_a$), defined as the energy difference between the conduction band minimum ($E_C$) and the Fermi level ($E_F$) near the semiconductor-insulator interface.[15,16] It is observed that the total DOS for device B was much larger than those of devices C and D over the entire energy range extracted. It is suggested that the significantly high density of deep level states may have affected the excess electron generation because the electrons can be easily activated by external parameters such as gate bias and temperature. The induced excess electrons in the channel layer would lead to negative shift of $V_{th}$ as well as degradation of SS value. In addition, hydrogen related defects may also have generated hole carriers within the a-IGZO layer, and upon negative gate bias stress, hole trapping near the semiconductor-gate dielectric could have occurred, thus resulting in negative $V_{th}$ shifts.[18] It is also suggested that the relatively larger shallow DOS distribution for device D as compared to device C would be related to the presence

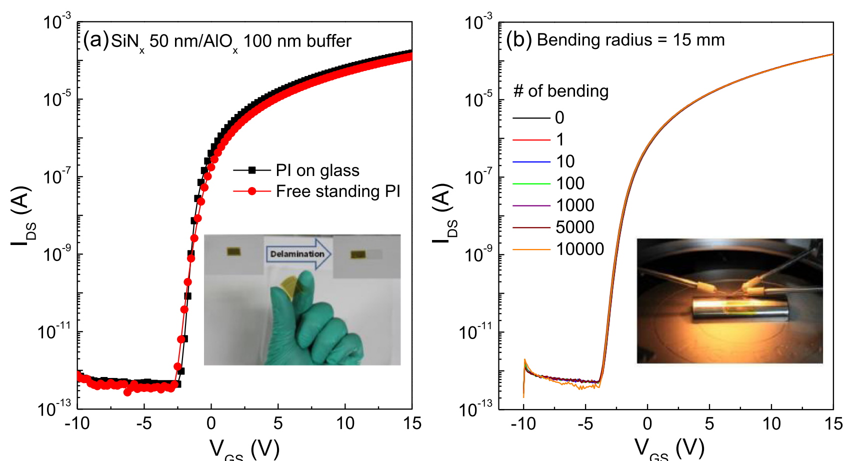


FIG. 5. (a) Representative transfer characteristics of a-IGZO TFT with $SiN_x$ (50 nm)/$AlO_x$ (100 nm) buffer layer before (squares) and after (circles) debonding from the glass substrate. Inset: A photograph of the flexible a-IGZO TFTs on the free standing PI substrate. (b) Evolution of the transfer characteristics of the flexible a-IGZO TFTs with increasing number of bending at radius (R) of 15 mm. Inset: A photograph go the flexible a-IGZO TFTs bent at R = 15 mm.

TABLE II. Extracted electrical parameters of a-IGZO TFTs with $SiN_x$ (50 nm)/$AlO_x$ (100 nm) buffer layer before and after debonding from the glass substrate.

| | $V_{th}$ (V) | $\mu_{sat}$ ($cm^2$/Vs) | SS (V/decade) |
|---|---|---|---|
| PI on glass | −1.09 | 15.42 | 0.23 |
| Free standing PI | −0.86 | 13.9 | 0.32 |

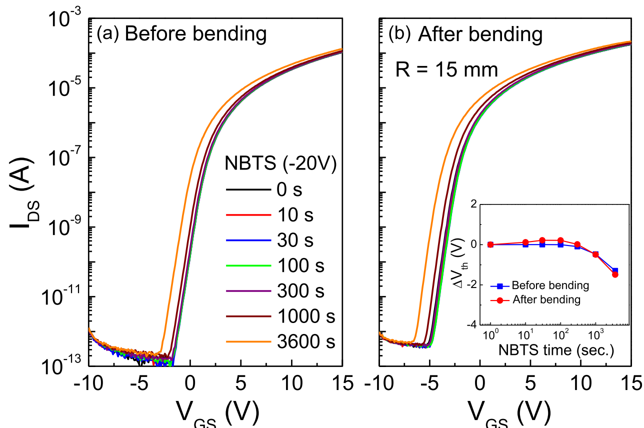


FIG. 6. Evolutions of the transfer curves as a function of the applied NBTS time for flexible a-IGZO TFTs on the free standing PI substrates before (a) and after (b) bending at R = 15 mm. Inset: The negative shift of the extracted $V_{th}$ values as a function of the NBTS time.

of donor-like states originating from water molecules, which were diffused through the $SiO_x$ layer from the PI substrates. This is illustrated as a schematic diagram in Figure 4.

The transfer properties of device C before and after the PI is removed from the glass substrate are shown in Figure 5(a). A slight degradation in the device performance is observed (Table II); however, it is seen that the devices on free standing PI are very stable with respect to mechanical stress. The PI was bent several times to a radius of curvature of 15 mm, and it is shown in Figure 5(b) that even upon repeated bending up to 10 000 times, the transfer characteristics are not significantly affected. The corresponding TFTs were also subjected to negative bias stress before and after bending, and the results shown in Figure 6 indicate that the application of mechanical stress does not affect the device stability under negative bias stress.

To summarize, a-IGZO TFT devices were fabricated onto flexible PI substrates. The application of different buffer layers between the active and the PI resulted in different device properties, and it was suggested that the simultaneous suppression of moisture and/or hydrogen diffusion from the underlying layers including PI substrates to the semiconductor would be an important factor to fabricate flexible oxide TFTs reliably. The use of a $SiN_x$/$AlO_x$ with a relatively thick $AlO_x$ film (100 nm) resulted in the best TFT performance and stability under negative bias stress. Once the PI is detached from the glass substrate, bending experiments were carried out, and the TFT characteristics were not affected by mechanical stress even at a radius of curvature down to 15 mm. Also, the application of mechanical stress did not affect the stability of the TFT device under negative bias stress.

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