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Water-related abnormal instability of transparent oxide/organic hybrid thin film transistors

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We have fabricated fully patterned transparent oxide/organic hybrid transistors on glass substrates that contain In-Ga-Zn-O as the active layer and a poly(4-vinyl phenol-comethyl methacrylate) copolymer as the dielectric layer. These devices exhibit a saturation mobility of 6.04 $cm^2/V\,s$, a threshold voltage value of 3.53 V, a subthreshold slope of 360 mV/decade, and an on-off ratio of 1.0×10^9 at a maximum processing temperature of 200 °C. We found that the bias stability characteristics of the hybrid transistors are dependent on the ambient conditions, but can also be dramatically improved by applying a hydrophobic organic passivation layer to the gate insulator. [doi:10.1063/1.3551536]

In spite of many efforts in recent decades to develop flexible active matrix (AM) displays by using organic light emitting diodes (OLEDs), thin film transistor (TFT) liquid crystal displays, and electrophoretic paper, there are still no flexible displays with suitable performance. Low-temperature and low-cost processing, device-flexibility, and good electrical performance are essential in such displays. The main hurdles to the realization of these characteristics are the absence of any proven backplane for the flexible substrate and device stability issues.[1] The active layer and gate insulator (GI) are vital to good device performance, stability, and flexibility. There are many types of TFTs, such as a-Si TFTs, low-temperature poly-Si (LTPS) TFTs, and organic TFTs (OTFTs), which could potentially be used as the backplanes of flexible displays. However, these TFTs have critical problems such as low field effect mobilities (a-Si:H and OTFT), relatively high temperature processing (a-Si:H and LTPS), and low uniformity (LTPS).[2–4] Since the report of transparent amorphous oxide semiconductors by Nomura *et al.*[5] and Cho *et al.*,[6] oxide TFTs have received significant attention, because of their potential to overcome these problems. Recently, flexible AM-OLEDs driven by oxide TFTs on a stainless steel plate and with a plastic substrate have been reported. Although the oxide TFT performance is sufficient to drive such OLEDs, these oxide TFTs consist only of inorganic layers, and so processing temperatures are as high as those fabricated on glass substrates.[7] When SiO_2 or SiN_x, the inorganic gate insulator, is deposited at low temperatures by means of plasma enhanced chemical vapor deposition, its electrical characteristics can be worse than those of a well-cured organic layer. To obtain a backplane with real flexibility, we believe that at least the GI must be organic since this layer covers most of the panel surface. However, it is difficult to fabricate an electrically stable TFT with an organic gate insulator even for an oxide TFT. Although oxide TFTs with organic gate insulators can exhibit high mobility, their stability under bias stress is not acceptable and has not yet been reported in detail.[8]

To fabricate an electrically stable oxide TFT, controlling the interface is the most important factor. By using a plasma damage free inorganic layer in the preparation of the interface, oxide TFTs can exhibit high performance.[9] Studies of hybrid transistors that use thin inorganic layers in the channel/gate insulator interface and bulk organic layers to improve the device performance, particularly the flexible backplane, are necessary. Here, we report the fabrication of a transparent oxide TFT with organic and inorganic hybrid layers fabricated at temperature below 200 °C by using a conventional photolithography process on a glass substrate and confirm its applicability to flexible displays. We also investigated the bias instability mechanism of the device with the aim of improving its electrical performance.

Transparent hybrid TFTs with staggered structures were fabricated on glass substrates by using In-Ga-Zn-O (IGZO) as the active layer and poly(4-vinyl phenol-co-methyl methacrylate) (PVP-PMMA) as the dielectric layer. Figures 1(a) and 1(b) show the side-view and top-view of staggered struc-

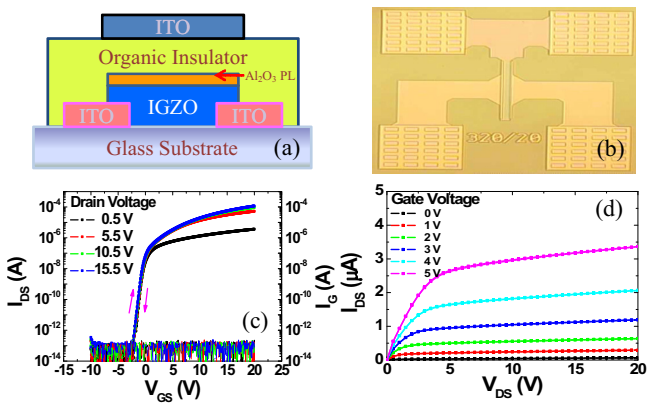

FIG. 1. (Color online) Device structure of hybrid TFTs: (a) side-view and (b) top-view (microscope image); I-V characteristics of hybrid TFTs at a maximum process temperature of 200 °C: (c) transfer curves (d) and output curves (W=320 μm, L=20 μm).

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ture device, respectively. Sputtering was used to deposit a 150 nm thick In-Sn-O (ITO) source and drain electrodes which were then patterned with photolithography. A 21 nm thick IGZO active layer with a molar ratio of approximately 2:1:2 was deposited at room temperature by using rf-magnetron sputtering and a 9 nm thick Al_2O_3 first gate insulator was grown at 200 °C with atomic layer deposition by using trimethyl aluminum and water as the Al and oxygen precursors, respectively.[9,10] The active and first gate insulator layers were then simultaneously patterned by using wet-etching. A 330 nm thick PVP-PMMA copolymer film was spin-coated and annealed at 180 °C to cross-link the dielectric layer and thus increase its chemical resistivity and dielectric strength.[11] A metal contact hole was formed by dry-etching with oxygen plasma. Finally, a 150 nm thick ITO gate electrode was deposited via rf-magnetron sputtering and patterned by using wet-etching. The fabricated devices were annealed at 200 °C to remove any water and solvent residues from the dielectric layer and to improve the device performance by reducing the active/first gate insulator interface trap density. We measured the I-V and C-V characteristics with an Agilent B1500A semiconductor parameter analyzer placed in a dark box to prevent light effects.

The hybrid TFTs were found to exhibit a saturation mobility of 6.04 $cm^2/V\,s$, a threshold voltage (V_T) value of 3.53 V, a V_{on} (turn-on voltage) value of −1.98 V, a subthreshold slope of 360 mV/decade, and an on-off ratio of 1.0×10^9. To our surprise, these TFTs exhibit negligible hysteresis in the clockwise direction (under 0.1 V) with very low drain-off and gate-leakage currents, which means that the water molecules in the bulk organic insulator do not seriously induce hysteresis, as shown in Figs. 1(c) and 1(d). The transfer characteristics of these TFTs seem to be dominated by the active/GI interface.

We also investigated the bias stress stability characteristics of the hybrid TFTs. These characteristics are affected by several factors, such as the active/GI interface, the bulk properties of the active and GI layers, and the contact between the source/drain electrodes and the active layer. Organic insulators are generally very sensitive to water molecules, other chemicals, and environmental conditions, so detailed studies of the stability of hybrid TFTs are necessary to elucidate their degradation mechanisms and to improve their stability which is a view to their application in flexible devices.

When we applied a gate bias stress of 20 V to the hybrid transistors under air ambient, V_T's were significantly shifted to more negative values, as shown in Fig. 2(a). In the case of IGZO oxide transistor with a single alumina gate insulator, V_T and V_{on} are generally shifted in the positive direction under an applied positive gate bias stress (PGBS) mainly due to the electron trapping at the active/GI interface.[12–14] Our experimental results cannot be explained solely in terms of the active/GI interface charge trapping mechanism; gate field-induced positive charges or polarity might be present in the PVP-PMMA copolymer layer. There are two possible causes in the copolymer layer of these effects: the presence of ionic impurities with a positive polarity that arise during the polymer synthesis process and the presence of absorbed water molecules or solvent in the organic insulator, arising from the air or the wet-processing used to form the fine patterns.[15,16] To distinguish between the effects of the ion impurities and the water molecules, we applied the same PGBS to the device under vacuum and found that the V_T value was shifted in the positive direction, as shown in Fig. 2(b). This direction is opposite to that obtained under air conditions and agrees with that obtained for IGZO TFT with an alumina gate insulator. The ionic impurities are not affected by the vacuum chamber, so this positive shift indicates that the main reason for the abnormal instability is the presence of water molecules absorbed from the air ambient and during the wet-processing.

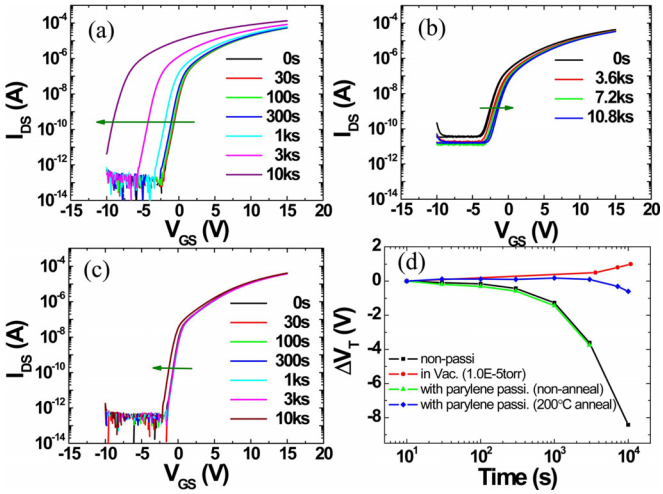

FIG. 2. (Color online) Stability characteristics of the TFTs at a gate bias of 20 V: (a) without passivation and under ambient conditions (W=40 μm, L=20 μm), (b) without passivation and under vacuum conditions (1.0×10^{-5} torr) (W=320 μm, L=20 μm), (c) with a parylene-C passivation layer and under ambient conditions (annealed at 200 °C), and (d) ΔV_T for the different devices and measurement conditions (V_D=10 V).

In the case of inorganic device with top-gate structure, devices were naturally passivated by inorganic insulators such as SiO_2, SiN, and Al_2O_3. However, hybrid TFTs are composed of polymer insulators, water, and oxygen molecules that can easily diffuse from the air and/or during the patterning process to the dielectric layer through the air exposed gate insulator surface. To protect the organic insulator from ambient water molecules, we deposited 500 nm thick parylene-C as a passivation layer, followed by patterning with photolithography and dry-etching. Organic passivation layers are more suitable for flexible devices than inorganic thin films, but their barrier properties are inferior to those of inorganic layers. Hydrophobic parylene-C is however widely used in OTFT fabrication as a passivation layer and in some cases as an insulator and a separator because it exhibits good barrier and adhesion properties.[17] We annealed the devices at 200 °C under vacuum conditions to remove the water molecules generated during the patterning of the passivation layer and applied the same PGBS in air. The bias stability characteristics were found to improve dramatically as a result of the parylene-C passivation layer and the water-removing process, and ΔV_T was −0.6 V during 10 ks, as shown in Fig. 2(c). Although organic layers cannot sufficiently protect devices from water molecules, our results show that this organic passivation layer can effectively protect devices under an applied PGBS. Figure 2(d) shows the V_T variations for different devices and measurement conditions under a PGBS of 20 V.

We applied gate bias stresses of 5, 10, 20, and −20 V to the devices with a passivation layer under air conditions to investigate their field-dependency characteristics. When the

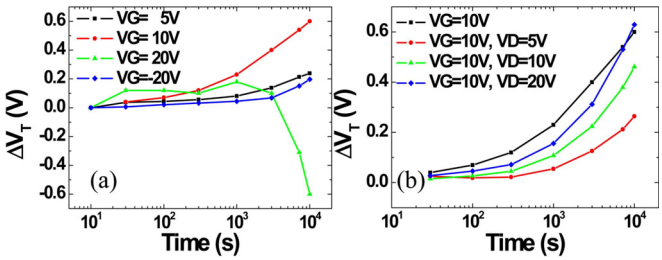

FIG. 3. (Color online) Stability characteristics of hybrid TFTs containing a passivation layer: (a) ΔV_T variation under several gate bias stresses, (b) ΔV_T variation under several gate (10 V fixed)/drain bias stresses (V_D =10 V).

gate bias was increased from 5 to 10 V, ΔV_T was increased from 0.2 to 0.6 V. Not only the V_T variation is different for the low (5 and 10 V) and high (20 and −20 V) field regions, but also the V_T shift is not proportional to the logarithmic time-scale, as shown in Fig. 3(a). Water molecules and electron-trapping effects do still affect this system, and this coexistence of positive and negative shifting factors means that the ΔV_T shifts of the devices are affected by both the stress field and time. Finally, we applied several gate/drain bias stresses (voltage fixed current stress) to the devices containing a passivation layer [see Fig. 3(b)]. When the drain voltage was increased from 0 to 20 V with V_G fixed at 10 V, the normalized current degradation and ΔV_T were also affected by the drain voltage. We believe that the applied drain voltage decreases the gate field near the drain electrode, so that ΔV_T is reduced with respect to that obtained for a gate voltage of 10 V.

In summary, we have carried out a study of the feasibility of the application of organic/oxide hybrid TFTs on glass substrates in flexible displays. The transparent hybrid TFTs were found to exhibit high performance in mobility and bias stress stability. To study the effects of bias stress, we applied a gate bias stress of 20 V to devices with and without a passivation layer. These stability experiments showed that the presence of water molecules is the main reason for the negative V_T shift of the hybrid TFTs under a PGBS, and that the use of an organic passivation layer dramatically reduces the negative V_T shift. However, water molecules and electron-trapping effects cause negative and positive V_T shifts, respectively; ΔV_T of the passivated devices is still affected by both the stress field and time.

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