Positive Interaction Between Charge Trapping and Polarization Switching in Metal-Interlayer-Ferroelectric-Interlayer-Silicon (MIFIS) Ferroelectric Field-Effect Transistor

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***Abstract*— This study employs analytical simulation to illustrate the beneficial correlation between interface trapped charge and spontaneous polarization (P_S) switching behavior in the MIFIS gate stack. We found that there is a positive interaction between charge trapping and polarization switching, comprising three sequential processes. (i) In the process of program (erase) operation, electrons (holes) are introduced from the gate metal and are trapped at the interface between the gate interlayer (gate-IL) and the ferroelectric layer. (ii) The trapped charge amplifies the electric field across the ferroelectric (FE) layer, subsequently enhancing P_S. (iii) The increase in P_S intensified the induced field on the gate-IL which boosts the charge injection. The three processes are reiterated as previously mentioned. The results indicate that the significant memory window (MW) observed in MIFIS ferroelectric field-effect transistor (FeFET) is a consequence of the combined effect of trapped charges and polarization switching charges, rather than separate contributions. Lastly, with the calibrated simulation model, we provide strategies to improve the device performance in terms of MW and operation speed. The experimental findings and analytic comprehension in this work provide a foundation for future researches on FeFET.**

***Index Terms*— FeFET, large memory window, low operation voltage, positive interaction.**

I. Introduction

TODAY, ferroelectric field-effect transistor (FeFET) has attracted massive attention as a promising candidate for next-generation 3D NAND technology. FeFET is suitable for replacing conventional charge trap-based 3D NAND thanks to its low voltage, high scalability, and CMOS compatibility [1]-[6]. However, traditional FeFET featuring a metal-FE-insulator-Si (MFIS) gate stack has a limited MW (≈ 3.1 V), hindering the quad-level-cell (QLC) programmability for high-density non-volatile memory (NVM) applications. In MFIS FeFET, the injected charge from the gate compensates that polarization which consequently limits the MW of the FeFET [7], [8]. This narrow MW has hindered the use of FeFET technology in 3D VNAND [9]. To enlarge the MW characteristic of FeFET, the heterostructure (FE/Al_2O_3/FE) FeFET has been proposed to reduce the capacitance of the FE layer (C_{FE}) while maintaining the optimized thickness of the FE layer for large polarization. It is experimentally verified that MW can be expanded up to 7.1 V without sacrificing the operation speed of the device [10]-[11]. However, it still requires further expansion of MW to replace the conventional 3D charge trap flash NAND. Also, the intricate structures of FeFETs with floating gates [12]-[16] or double gates [17]-[19] render them unsuitable for use with the current 3D vertical NAND mold [20].

Recent study has shown that inserting a gate-IL between the gate and FE layer enhances the MW performance of FeFET, while being compatible with the 3D NAND mold. Contrary to MFIS, the MIFIS gate stack captures charges that are injected from the gate at the interface between gate IL and the FE layer, introducing the favorable charge component Q_{it}', which allows for MW enhancement by utilizing both charge trapping and polarization switching behaviors. A recent study described that MIFIS FeFET has shown impressive MW up to 10.54 V, which is the highest among the reported FeFET, and shown its feasibility on QLC operation for NVM applications [21]-[23].

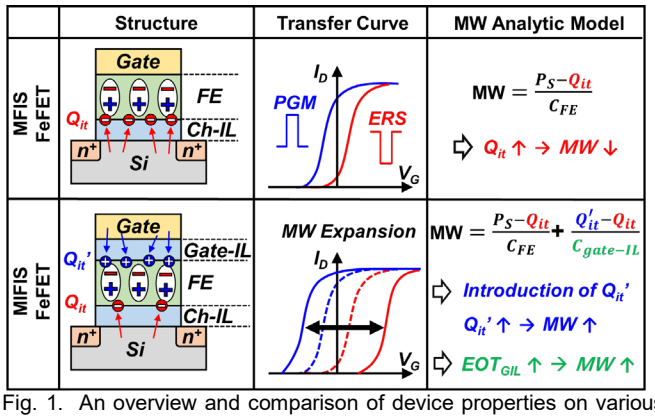

Fig. 1. An overview and comparison of device properties on various stacks of FeFET and the effect of interface trap charge on FeFET performance.

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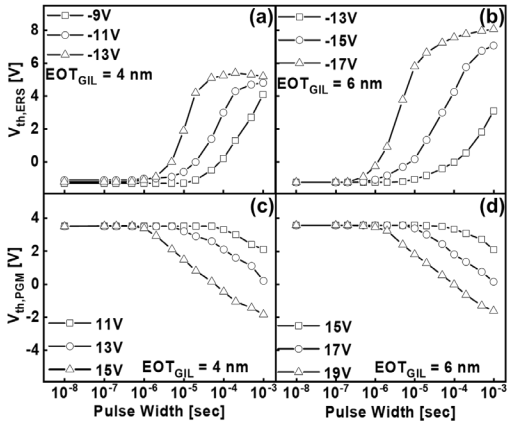

Fig. 2. Measured ERS speed of device with gate-IL of (a) SiO_2 4nm, (b) SiO_2 6nm and PGM speed of (c) SiO_2 4nm, d) SiO_2 6nm.

Furthermore, the numerical MW model regarding to the Q_{it}' and polarization is provided by Lim et al [23], however, the prior work did not consider the interaction between Q_{it}' and P_S which is in need to be analyzed for the further improvement of the device performance of MIFIS FeFET.

This work presents a novel finding of a previously undisclosed interaction between Q_{it}' and polarization switching, where they mutually enhance each other's effects. This discovery is based on experiment results and the calibrated simulation model that captures the transient interaction between a distributed electric field on each layer, charge trapping, and polarization switching. The results indicate that Q_{it}' plays a crucial role not only in the MW enlargement in MIFIS FeFET, but also in facilitating polarization switching behavior. This work provides a clear vision on an interaction between charge trapping & polarization switching and the comprehensive analysis is anticipated to act as a foundation for the realization of high MW MIFIS FeFET.

II. Experimental Details and Results

The devices were fabricated following the process sequence outlined below. To increase the quality of the 15 Å thick ch-IL formed on the p-type wafer, SPM cleaning was used followed by a rapid thermal annealing (RTA) process at 1000 ℃ in a N_2 environment. The $Hf_{0.5}Zr_{0.5}O_2$ film was then produced using a plasma-enhanced atomic layer deposition (PEALD) technique at 320 ℃ chamber temperature. TEMA Hf and TEMA Zr were used as the predecessors for the HfO_2 and ZrO_2 layers. For gate-IL, 40 and 60 Å thick SiO_2 films were prepared by using PEALD, followed by TiN gate metal formation and patterning. Finally, for the crystallization of $Hf_{0.5}Zr_{0.5}O_2$ FE layers, the RTA was carried out at 600 ℃ in an N_2 atmosphere.

Fig. 2(a)-(d) show the measured operating speed of MIFIS FeFETs with gate-IL SiO_2 thicknesses of 4 nm and 6 nm. Notably, the devices have a maximum MW of 7.9 and 9.7 V, respectively. Previous work shows that increasing EOT of gate-IL (EOT_{GIL}) leads to MW expansion based on analytic model for MW [18]. Interestingly, while $V_{th,ERS}$ is increased significantly along with the increase of EOT_{GIL}, the change in $V_{th,PGM}$ is little, implying that there is an unknown physics behind the operation of MIFIS FeFET. However, the previous model fails to account for this finding since it assumes the P_S and Q_{it}' contribute to the MW independently. This model limitation complicates the careful design of the MIFIS gate stack for further performance improvements. In this work, we offer a numerical model that would reveal the underlying beneficial relationship between P_S and Q_{it}'. Furthermore, based on this modeling work, we propose realistic ways for improving the performances of the MIFIS gate stack.

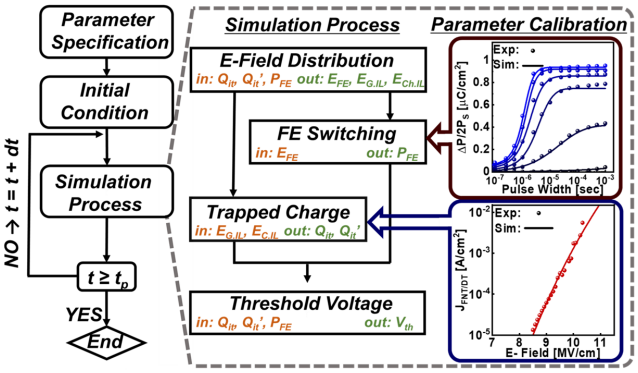

Fig. 3. Modeling framework with calibration data of polarization and tunneling current density.

III. Modeling Framework and Simulation Results

Fig. 3 depicts the modeling framework employed in this investigation. The iterative technique progresses at the given time step (dt = 100ns) utilizing calibrated parameters and specified initial circumstances. The electric field produced on each layer in the gate stack is calculated by dispersing the applied gate voltage and bound charge (Q_{it}, Q_{it}', and P_S) relative to the capacitance of each layer. The Q_{it}, Q_{it}', and P_S are individually computed using the given electric field. The classic Preisach model is limited in its ability to accurately reflect the dynamic switching of P_S [24]. Therefore, the time-dependent Preisach model proposed by Ni et al. is employed [25]. Meanwhile, tunneling current density from the channel (gate) is determined by induced field on the ch-IL (gate-IL) [26]. Once the tunneling current density is determined, it is then multiplied by capture cross-section (σ_t) and trap density [27]. Injected electrons (holes) either trap in the empty trap sites or recombine with the trapped holes (electrons) [28]. Once the trap density is updated, it is then integrated with elementary charge to compute Q_{it} (Q_{it}'). Finally, V_{th} is calculated using the obtained bound charge [12]. The proposed simulation model is calibrated to the experimental values of polarization switching and tunneling current to capture the value of the electric field, trapped charges, and P_S to quantify the values of each component during the operation.

Fig. 4(a) presents the calibration of simulation to experimental output of MIFIS FeFET with gate-IL of SiO_2 6nm. Fig. 4(b)-(d) illustrates simulation result of the tunneling current density, electric field on FE layer (E_{FE}), and P_S respectively during program/erase. Tunneling current density of electrons (J_e) during erase overwhelms the tunneling current density of hole (J_h) during program throughout the pulse time (t_p) (Fig.4(b)), owing to the difference of energy barrier ($\Phi_{B,e}$ = 3.5 eV, $\Phi_{B,h}$ = 5.4 eV) [29]. The high tunneling current density leads to high Q_{it}'. As P_S switches ($t_p = 10^{-6}$ sec), the P_S bound charge induces high field across gate-IL which increases the J_e/J_h. Simultaneously, it creates depolarization field (E_{dep}) over FE layer and decreases the E_{FE} (Fig. 4(c)). To be noted, devices in this work has a channel length/width of 10/50 μm, respectively,

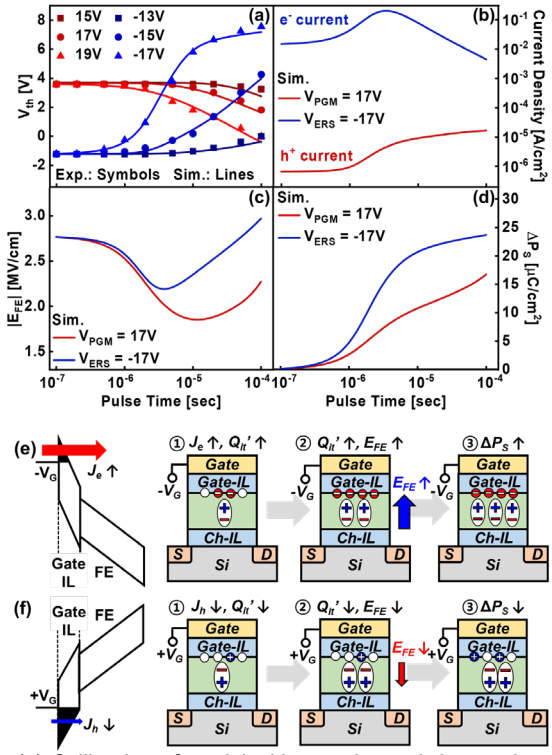

Fig. 4. (a) Calibration of model with experimental data and transient simulation output of (b) tunneling current density, (c) electric field across FE layer, and (d) polarization respect to pulse time. Energy band diagram and snapshots of MIFIS FeFET during (e) erase and (f) program operation.

which results in a relatively slower switching speed. However, it still exhibits faster operation compared to typical charge trap flash devices. After certain period of time, E_{FE} recovers with the help of injected Q_{it}', which compensates P_S and it results in E_{dep} reduction. The asymmetry of operation voltage and the difference in switching speed for PGM/ERS can be explained with the simulation results in terms of Q_{it}' and P_S switching.

IV. Positive Interaction of Charge Trapping and Polarization Switching

The positive interaction between Q_{it}' and P_S comprises the following 3-steps (Fig. 4(e)-(f)): **(1)** According to the Fowler-Nordheim tunneling equation with the Wentzel, Kramers, and Brillouin (WKB) approximation, J_e is significantly higher than the J_h due to low energy barrier [20]. It is intuitive that Q_{it}' during the erase is higher than Q_{it}' during the program owing to the high tunneling efficiency of electrons. **(2)** Along the P_S switching, the P_S bound charge induces E_{dep} on the FE layer which self-disturbs its further switching. Q_{it}' compensates the bound charge since it has the opposite polarity to the P_S bound charge in the FE/gate-IL interface. Furthermore, the polarity of Q_{it}' equivalent to the gate voltage, therefore induces the electric field on the FE layer in an equal direction to the gate voltage and E_{FE} can be larger than its original value. Thanks to high Q_{it}' for ERS, E_{dep} is deceased and E_{FE} starts to increase as Q_{it}' accumulates. Meanwhile, the E_{FE} for the program is lower, owing to the insufficient Q_{it}'. **(3)** With high (low) induced E_{FE}, P_S switching behavior is enhanced (reduced) for erase (program). P_S generates a substantial field across gate-IL leading to a high tunneling current, which again boosts the P_S

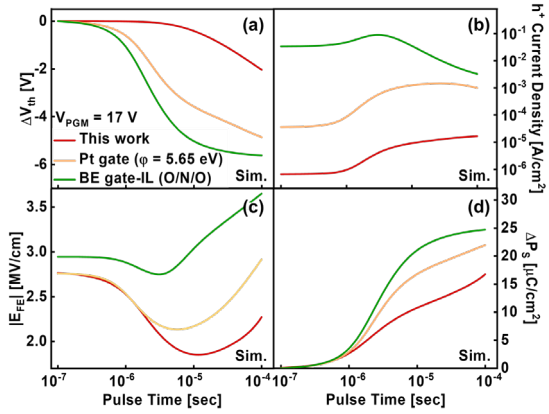

Fig. 5. Simulation data of device with Pt gate and BE gate-IL compared to the fabricated device in this work. (a) ΔV_{th}, (b) hole tunneling current, (c) E_{FE} and (d) ΔP_s during the PGM operation

switching until the P_S is saturated. Once the P_S switching is saturated, injection of Q_{it}' then decreases the induced field on gate-IL as shown in the electron tunneling current drop illustrated in Fig. 4(b). Due to low tunneling efficiency of holes, this positive interaction cannot be fully activated, leading to the limited performance improvement for MW of MIFIS FeFET.

The simulation results imply that increasing the injection Q_{it}' not only enhance the MW but also the operation speed attributed to the positive interaction between charge trapping and polarization switching. Then, it is intuitive that to enlarge the MW and lower the operation voltage during PGM operation, one can either use the gate metal with high work function [30] or utilize the band-engineering gate-IL such as $SiO_2/Si_3N_4/SiO_2$ (ONO) stack which enhances the hole tunneling efficiency [31]. Both strategies are simulated separately by replacing the gate material to Pt and gate-IL to ONO with thicknesses of 1.5, 2.0, and 2.5 respectively (Fig. 5(a)-(d)). We verified that both approaches can increase the MW and operation speed of MIFIS FeFET during the PGM operation (Fig. 5(a)). Since the Pt gate lowers the energy barrier on the valence band side and ONO gate-IL enhances the tunneling efficiency of the hole by utilizing the low valence band characteristic of Si_3N_4, the hole tunneling current density is larger than the fabricated device in this work. This leads to enhanced E_{FE} during the operation and consequently boosts the P_S. Interestingly, despite the lower EOT_{GIL} of ONO compared to SiO_2 6nm, the MW is significantly increased. This result implies that enhancing the hole tunneling current is a more viable approach rather than increasing the EOT_{GIL}.

V. Conclusion

This research investigates the synergetic interplay between Q_{it}' and P_S in the MIFIS gate stack utilizing a combination of modeling work and experimental data. This work highlights that Q_{it}' plays a role in both the MW enlargement and the improvement of the polarization switching. In addition, in order to achieve a large MW for the penta-level cell (PLC) in the MIFIS FeFET, it is crucial to strengthen the positive interaction by improving hole injection during the programming process. Thus, our discoveries can be employed as design principles for the MIFIS FeFET gate stack in future investigations.

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