Device reliability under electrical stress and photo response of oxide TFTs

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Abstract — The stability of oxide TFTs has been the main focus of this research and is probably the most crucial requirement for the successful application to flat-panel displays. Although the high Fermi level of oxide semiconductors makes TFTs basically stable under electrical stress, the device reliability under diverse variations of electrical stress is affected by materials such as active semiconductors and gate insulators, processes for the formation of back/front channels and passivation layers, and device configurations among other things. How these factors affect the device reliability have been investigated and a review of the stability is presented. In addition, several categories of the light instability of oxide TFTs is presented and the origin is discussed.

Keywords — *Oxide TFT, bias stability, passivation, photo response, negative-bias enhanced photo instability.*

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1 Introduction

Since the report on a transparent amorphous InGaZnO thin-film transistor (TFT) by Hosono *et al*.[1] and a polycrystalline ZnO TFT by Wager,[2] oxide semiconductors have rapidly become a focus of intense research and development, not only in academia but in major industrial laboratories[3] mainly with expectations of replacing amorphous- and polycrystalline-silicon-based TFTs for thin-film-transistor (TFT) liquid-crystal displays (TFT-LCDs)[4] and active-matrix organic light-emitting diodes (AMOLEDs)[5] among other things. The expected economic benefits are enormous considering the sheer size of related industries and stem primarily from the possibility to manufacture highly stable TFTs with high mobility at low cost and additionally the nature of visible-light transparency attainable with the materials. Oxide semiconductors are also foreseen to open the door to the possible realization of a variety of electronic and optoelectronic devices such as a memory device.[6,7]

Over the past few years, there have been a number of papers regarding material selections,[8,9] fabrication methods,[10] device structures,[11] and stability issues such as environmental effect,[12,13] gate bias stress,[14–17] and light stability.[18] Being an essential factor for the practical application of oxide TFTs, the TFT stability has become the main focus of recent research works which have significantly contributed to the realization of highly stable oxide TFTs against the gate-bias stress and the constant-current stress. According to Kamiya *et al.*, the origin of high electrical stability of oxide TFTs can be explained in terms of the high Fermi level (E_F) of oxide semiconductors.[19] In oxide semiconductors, there exist high-density subgap states coming from the oxygen vacancies close to the valence-band maximum (VBM) and tail states, which can be significantly reduced by a proper thermal annealing process, especially with water vapor. Furthermore, these deep-level states in amorphous-oxide semiconductors located close to VBM must be inactive due to high E_F and would not affect the n-type TFT operational characteristics. Nevertheless, the TFT stability is governed by the gate insulator, the interface between the active layer and the gate insulator, and the active layer. Especially in the case of oxide semiconductors of which characteristics are affected by water,[20] oxygen,[21] and hydrogen,[22] the passivation layer[23] in the bottom-gate structure would be of importance to get high stability.

Here, we investigate several factors which affect the bias stability and present a review on the stability. In addition, we examine the light-response phenomena of oxide TFT and discuss the origin.

2 Effect of gate insulator on the oxide-TFT stability

For those of every TFT, including a-Si,[24] low-temperature polysilicon (LTPS),[25] and organic TFTs,[26] the quality of the gate insulator is of particular importance in order to obtain high stability because the charge trapping at the interface or the injection into the gate insulator induces the V_{th} shift under the gate-bias stress. Especially, we have to consider the hydrogen content in the gate insulator because the characteristics of oxide semiconductors in TFTs could be variable by the degree of hydrogen incorporation from the gate insulator to the active layer during the ensuing process. Lee *et al.* reported the parallel V_{th} shift of a-IGZO TFT for SiN_x and SiO_2 gate insulators under the gate-bias stress, and they attributed the larger V_{th} shift for the gate insulator of SiN_x, involving more hydrogen content than that of SiO_2, to the charge trapping into the shallow hydrogen-related states at the interface.[27] A similar explanation was also given by Wager *et al.* who reported the rigid V_{th} shift to the positive direction of a-IGZO TFT with a thermal oxide under the $V_{gs} - V_{ds}$

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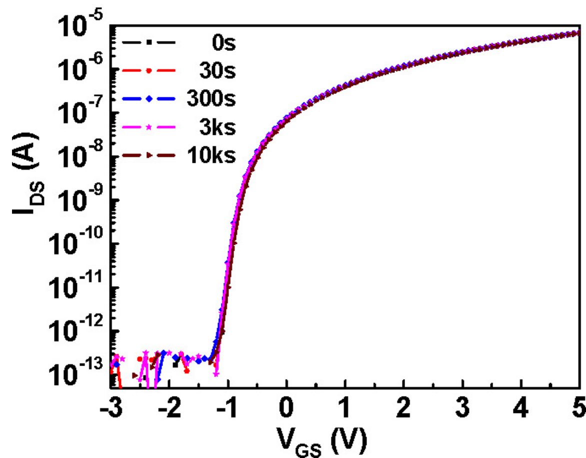

FIGURE 1 — The evolution of the transfer curves at room temperature with a positive gate bias stress of 10 V as a function of the measurement time for the bottom-gate ZITO TFT with an alumina gate insulator (W/L = 40 μm/20 μm).

stress. In this case, the possibility of charge trapping in the gate insulator was excluded due to the small capture cross section of thermal oxide.[28] While SiO_2 and SiN_x grown by plasma-enhanced chemical vapor deposition (PECVD) are mostly used for the gate insulator, alumina deposited by atomic layer deposited (ALD) was also widely used due to their excellent insulating characteristics.[29] Our group has fabricated a number of oxide TFTs with ALD-grown alumina and Ryu *et al.* reported a highly stable ZITO TFT with this gate insulator as shown in Fig. 1.[30] The transistor with the compositional ratio of Zn:In:Sn = 40:20:40 exhibited an excellent subthreshold swing (SS) of 0.12 V/decade, a V_{th} of 0.4 V, and a high $I_{on/off}$ ratio of 10^9 as well as a high μ_{FE} of 24.6 cm^2/V-sec. There was neither any noticeable degradation of the μ_{FE} and SS values nor any measurable shift in the V_{th} value during the positive gate-bias stress (PGVS) for 10^4 sec. The low interfacial trap density of the device resulted in the negligible presence of charge trapping or the injection into alumina and practically no shift of V_{th} after PGVS.

In a top-gate device structure, the gate insulator process affects the TFT performance considerably. To obtain highly stable TFTs, we need to use a damage-free or resistant process minimizing hydrogen incorporation and charge trapping for the gate-insulator formation. The creation of defects at the interface during the formation of the active layer and gate insulator induces the electrical instability of TFTs even with an insulator of high quality. To investigate the effect of interfacial defects on the stability of a top-gate ZnO TFT, we adopted a double-layered gate-insulator structure in which a thin channel protection layer (PL) acts as the first gate insulator as shown in Fig. 2. A dramatic difference in the bias-stress stability was observed, as shown in Fig. 3,[31] for two different PLs of alumina with the same bulk gate insulator: one deposited through the simple surface chemical reaction by ALD using water precursor and the other grown by oxygen plasma precursor. The latter showed much worse stability under a V_{ds}/V_{gs} = 20 V/25 V bias stress, which can be attributed to the plasma damage

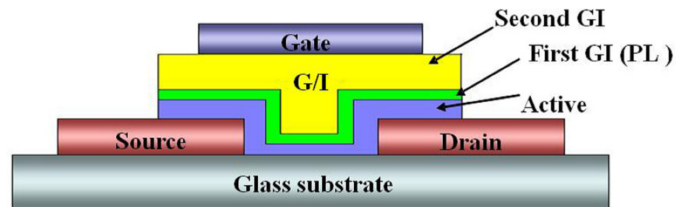

FIGURE 2 — Cross-sectional view of the top-gate oxide TFT consisted of the first gate insulator of the thin PL (protection layer) and second gate insulator.

because the device performance improved with decreasing plasma power. The result implies that the plasma damage at the interface, which may also occur during the formation of active layer or the S/D process in a bottom-gate device and the gate insulator process in a top-gate structure, can degrade the TFT performance. Sometimes, the gate insulator process may also induce the change of active properties such as the number of carriers or/and the density of states. Similar results were also reported for amorphous AlZnSnO (AZTO) TFTs as shown in Fig. 4. The AZTO TFT with a PL of alumina grown by ALD using water precursor appears to be more stable under bias stress with a good transfer curve than

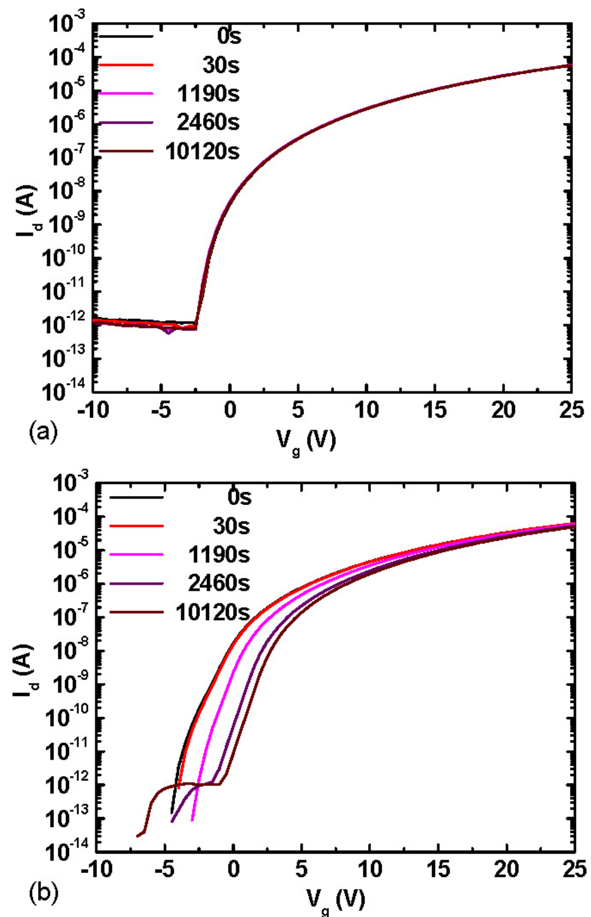

FIGURE 3 — The evolution of the transfer curves for the top-gate ZnO TFT with an alumina first gate insulator of PL at room temperature (a) deposited using water source to prevent the oxygen plasma damage on the ZnO layer and (b) deposited using oxygen plasma as a function of the applied-bias-stress time (W/L = 40 μm/20 μm, V_{gs}/V_{ds} = 25 V/20 V).

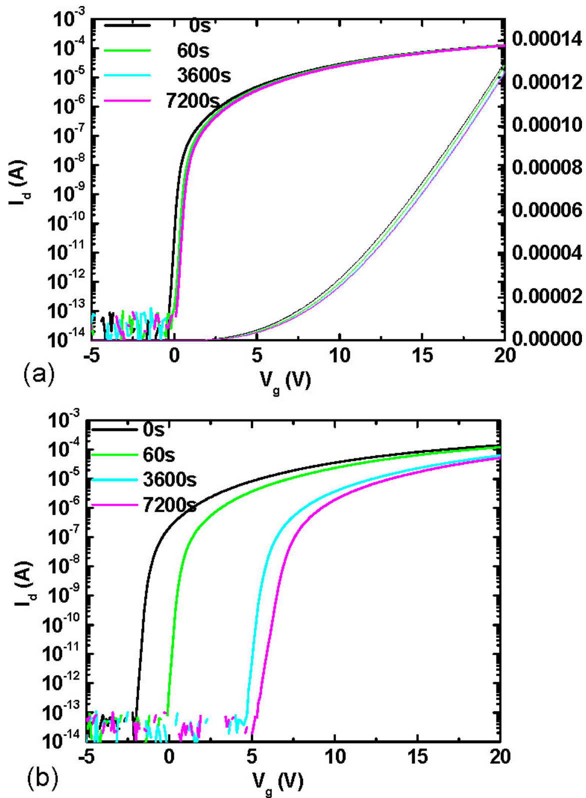

FIGURE 4 — The evolution of the transfer curves for the top-gate AZTO TFT with alumina first gate insulator of PL at room temperature (a) deposited using a water source and (b) deposited using oxygen plasma as a function of the applied-bias-stress time (W/L = 40 μm/20 μm, V_{gs} = 20 V).

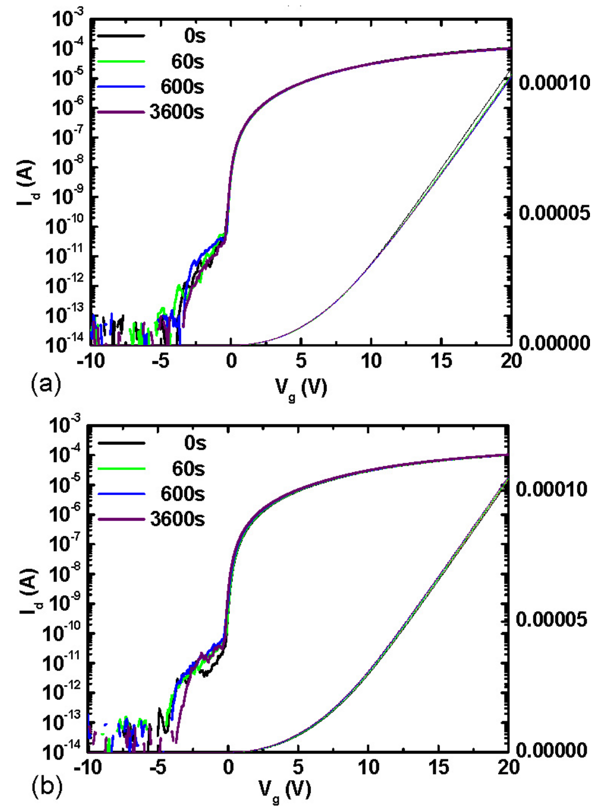

FIGURE 5 — The evolution of the transfer curves for the top-gate AZTO TFT with the alumina first gate insulator of PL deposited using oxygen plasma as a function of the applied-bias-stress time (W/L = 40 μm/20 μm) (a) V_{gs} = 20 V, V_{ds} = 0.1 V @60°C and (b) V_{gs} = –20 V, V_{ds} = 10 V @60°C).

that adopting a PL of alumina grown by an oxygen plasma precursor. Significant parallel shift of V_{th} with little change in SS and mobility is thought to be caused by the charge trapping into the defects at the interface. Since the oxygen plasma process accompanies energetic ion bombardments, more point defects can be introduced at the interface. Therefore, it is obviously advantageous to have a plasma damage-free PL process to obtain a stable oxide TFT. However, we determined that this type of point defect and the density of states formed at the interface and/or in the channel by a plasma process could be substantially reduced with a proper post-annealing process when the active layer of appropriately selected material does not change in carrier density much at a high temperature such as 300°C and with proper active-layer composition.[32] We can fabricate a stable TFT even with a plasma process for the interface formation by virtue of post-annealing depending on the active-layer composition. The mechanism involved may also be assumed in terms of interstitial oxygen in the active layer, formed during the plasma PL process (this will be further discussed later). In amorphous-oxide semiconductors with high density of oxygen vacancy, interstitial oxygen can be easily moved to oxygen vacancy during thermal annealing. If interstitial oxygen moves into oxygen vacancy during high-temperature annealing, good stability would be obtained with the reduction of charge-trapping centers. Meanwhile, semiconductors with less oxygen vacancy may cause generation of high amounts of oxygen interstitial site during the strong oxidant of oxygen plasma PL process to yield a fixed negative charge by electron trapping even after thermal annealing. If so, it could cause a significant positive V_{th} shift under PGBS. The subject is still under investigation. Figure 5 shows the bias stability of another top-gate AZTO TFT having different Al composition with a PL processed using oxygen plasma. We measured the negative-bias temperature stress (NBTS) and positive BTS (PBTS) at 60°C for 1 hour for the AZTO TFT annealed at 300°C, and the V_{th} shift was almost negligible. The hump in the subthreshold region was not the real data but was formed because of the heating chuck problem and we can ignore that. In this case, even with PL using oxygen plasma, TFTs showed high stability and we assume this difference in stability shown in Figs. 4(b) and 5(a) is due to the active-layer composition and proper reduction of defects in the interface.

Recently, the oxide TFT with an organic insulator has also been studied. In the early stages, the high mobility of oxide TFTs with an organic gate insulator was reported without any data on the stability and hysteresis.[33] The mobile charges originating mostly from the hydroxyl group in the insulator layer induced severe hysteresis, which resulted in errors in the calculation of mobility. Meanwhile, the organic gate insulator properly cured at a low temperature showed much improved bias stability. Yang *et al.* reported their work on the oxide TFT with organic/inorganic hybrid gate insula-

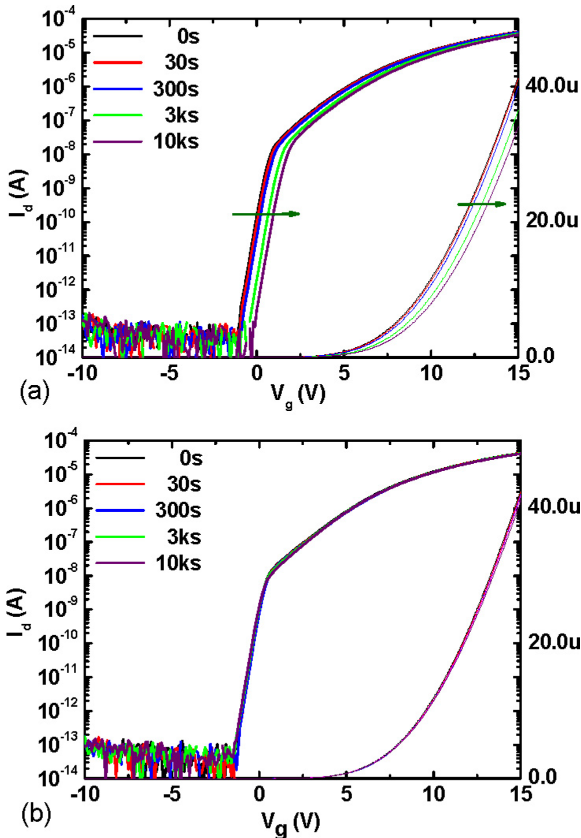

FIGURE 6 — The evolution of the transfer curves for the top-gate IGZO TFT with organic/inorganic hybrid gate insulator of thin alumina/polyimide as a function of the applied bias stress time at room temperature (W/L = 40 μm/20 μm) (a) V_{gs} = 10 V and (b) V_{gs} = –10 V.

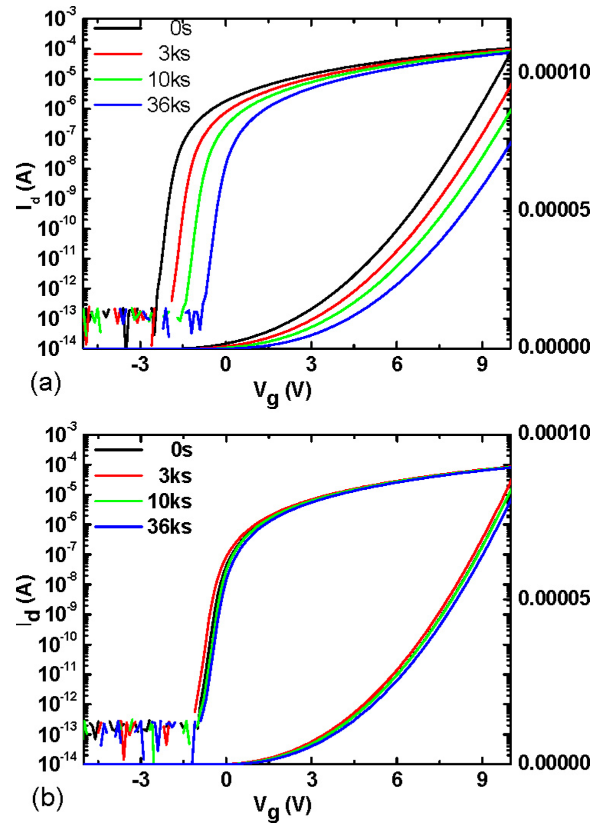

FIGURE 7 — The evolution of the transfer curves for the bottom-gate AlSnZnInO TFTs as a function of the applied bias stress time (W/L = 40 μm/20 μm) at room temperature (V_{gs} = 20 V): (a) device without passivation layer and (b) device with alumina passivation layer deposited using oxygen plasma.

tors[34] which showed a negligible hysteresis, a mobility of 6.65 cm^2/V-sec, an SS of 0.35 V/decades, and a high on–off ratio of 3.9×10^9. After the gate bias is applied for 10^4 sec, the V_{th} shift increased to +0.99 V without a change in mobility and SS as shown in Fig. 6, which shows promise of the organic gate insulator for flexible active-matrix displays driven by oxide TFTs.

3 Effect of passivation layer on the oxide-TFT stability

It is well known that oxide semiconductors are sensitive to oxygen, water, and hydrogen, and these sensitivities directly affect the stability of oxide TFTs. When a TFT is not passivated, we are concerned about the oxygen adsorption and desorption. Jeong *et al.* reported the improvement of bias stability with the use of a passivation layer which has a role in reducing the interaction between the IGZO surface and oxygen in the ambient atmosphere.[20] In their work, the positive V_{th} shift of 1.2 V for an unpassivated device results from both the negative charge trapping at the interface and the increased desorption of negatively charged oxygen under positive-gate-bias stress. Meanwhile, the device passivated with a dense SiO_2 film prevents oxygen adsorption, resulting in a smaller V_{th} shift of 0.42 V.

Similar results were also reported by Levy *et al.* who found that the ZnO TFT passivated by an alumina film showed a V_{th} shift less positive by 1.8 V compared to that of non-passivated TFT.[23] Lim *et al.* investigated the effect of a sputtered SiO_2 passivation layer, which revealed that the passivation layer reduced not only the charge trapping but also the formation of additional defect states. Figure 7 shows the dependence of the V_{th} shift on the gate bias stress for AlSnZnInO TFT with and without the passivation layer. The superior V_{th} stability for the passivated TFT is explained by the prevention of the ambient effect.[35] The water effect on a non-passivated device under the negative bias stress was reported by Liu *et al*.[13] They suggested that the negative bias stress increased the number of holes in the IZO channel, followed by the formation of positively charged species of water (H_2O^+) by the accelerated water adsorption and the electron transfer from water to the holes, which results in the negative shift of V_{th} in air. Therefore, we cannot overemphasize the importance of a passivation layer to obtain a highly stable oxide TFT. The proper selection of a passivation layer affects the TFT performance significantly as mentioned above.

We need to consider three factors in the passivation-layer process, of which the most important issue is the hydrogen incorporation that would make the active layer conductive. It is well known that the passivation layer of

PECVD SiN_x induces severe carrier generation in the channel layer due to the hydrogen incorporation, which makes it difficult for the oxide TFT to be modulated by the gate field.[36] Hayashi *et al.* rather made good utilization of a conductive IGZO film which resulted from the increased number of carriers due to a PECVD SiN_x: they used the conductive layer as a S/D electrode to fabricate a self-aligned bottom-gate TFT.[37] The PECVD-grown SiO_2 film usually generates less hydrogen during the process, and thus is commonly used as a passivation layer. However, since the deposition of SiO_2 by PECVD can also entail carrier increase according to the reaction gases[38], the deposition temperature and reaction gases must be controlled to keep the carrier amount low enough in the active layer.

The second thing to be considered is the defect generation in the back channel. Although the N_2O treatment or the oxygen supply during the passivation process would help control V_{th},[36] it could cause a problem in the bias stability as for the front channel. We investigated the effect of the passivation process on the bias stability with AlSnInZnO TFTs by depositing alumina films using water and oxygen plasma. Although the alumina grown with oxygen plasma brings about less hydrogen incorporation, it could induce defects in the back channel and instability of TFTs, especially under positive bias stress. Figure 8 shows the bias stability of AlSnInZnO TFT passivated with the alumina from water and oxygen plasma. The device with the water alumina showed less V_{th} shift of 0.07 V under the bias stress of V_g = 20 V than that with the oxygen plasma alumina which yielded a V_{th} shift of 0.87 V. This suggests that the passivation process for the formation of the back interface plays as an important role as that for the front interface. The plasma process effect on the back channel formed between the active and passivation layers shows similarly to the interface formation process effect on the front channel as mentioned before. When the active layer made of a properly selected material endures a high annealing temperature without any significant induction of an active-layer change, TFTs with a passivation layer processed by the oxygen plasma shows high stability by the reduction of defects formed in the back channel. Figure 7 shows the evolution of transfer curves as a function of the applied stress time for Al, Sn–In–ZnO TFTs without and with a passivation layer from oxygen plasma. Although the passivation layer was formed using oxygen plasma, the positive V_{th} shift was just ~0.2 V after a stress duration of 36,000 sec.

Lastly, the density of a passivation film needs to be taken into account. Since some oxide semiconductors are sensitive to the water or oxygen adsorption and desorption, we need to prevent the environmental effect by depositing a dense passivation layer. As Jeong *et al.* reported, [20] the IGZO TFT with an acrylate passivation layer showed larger V_{th} shift under the positive bias stress than that with a SiO_2 passivation film. A proper selection of a passivation layer would be a main factor to obtain a highly stable bottom-gate oxide TFT.

4 Effect of device structure on the oxide-TFT stability

There are only a few papers reporting the effect of device configuration on the bias stability. The bias stability of oxide TFT is quite dependent on the interface formation process and particularly sensitive to the plasma damage on the gate insulator during the deposition sequence of the channel and gate dielectric layers. In a top gate (TG), there would be no plasma damage on the gate insulator and rather we have to worry about the defect formation on the channel during the following process. Meanwhile, in a bottom-gate (BG) structure, charge-trapping centers would be easily formed on the gate insulator and/or at the interface during the active-layer deposition as long as we use a plasma process such as sputtering or PEALD. Energetic bombardments on the gate dielectric during the initial channel deposition by a plasma process directly affect the device stability to result in poor stability. We have made comparisons between the performance of AZTO TFTs with a BG structure with that of TG, both being fabricated by the same process and with the same materials. Even after post-annealing, the hysteresis of the BG device does not disappear. We assume that the charge trapping at the front interface of BG is much more severe, especially for the active layer processed by sputter-

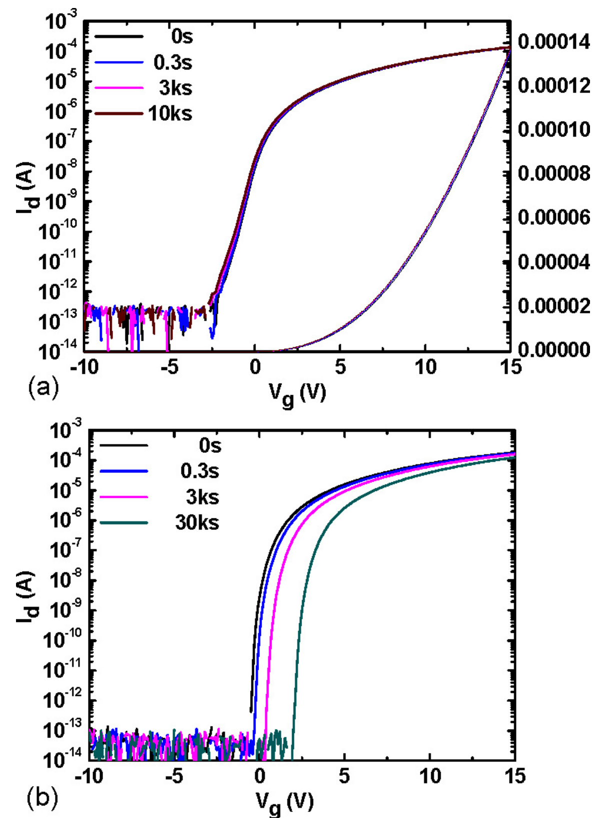

FIGURE 8 — The evolution of the transfer curves for the bottom-gate AlSnZnInO TFTs as a function of the applied-bias-stress time (*W*/*L* = 40 μm/20 μm) at room temperature (V_{gs} = 20 V): device with alumina passivation layer (a) deposited using water precursor and (b) deposited using oxygen plasma.

ing. For the AZTO TFT with an unpassivated BG, the measured values of V_{th}, μ_{FE}, and SS is 3.0 V, 15 cm^2/V-sec, and 0.35 V/decade, respectively while the TG device exhibits a V_{th} of 1.0 V, a μ_{FE} of 11.0 cm^2/V-sec, an SS of 0.17 V/decade. The smaller SS value for the TG device indicates smaller interfacial trap density compared to the BG device. This is further supported by Jeong *et al.* who calculated E_A (= E_C – E_F) as a function of V_{GS} for a passivated AZTO BG device and a TG device, where E_A is an activation energy, E_c is a energy level of the conduction band, and E_F is a Fermi level.[39] The calculated variation rate of E_A as a function of V_{GS} for the passivated BG device is higher to that of the TG device, which suggests that the total trap density of the TG device is smaller than that of the passivated BG device. The defects formed during the sputter deposition of the active layer appear to be responsible for the charge traps at the interface. Figure 9 shows the gate bias stability of the AZTO TFTs with TG and BG. To reduce the environmental effect on the bias-stress experiments, we measured the V_{th} shift for a passivated BG device which was fabricated with the alumina from a water ALD precursor instead of the one from oxygen plasma. While the positive V_{th} shift for the BG device was 9.04 V, that for TG was just 0.43 V after the stress duration of 10,000 sec. Therefore, in order to improve the bias-stress stability, the trap density at the interface should be minimized, which favors a TG TFT structure rather than a BG TFT. The sputtering, being mainly responsible for the plasma damage, is quite necessary to minimize the defect formation during the active-layer deposition in a BG structure. Furthermore, the instability of BG TFTs may also depend on the density of acceptor-like states in an active layer originating from the cation vacancy or oxygen interstitial. Therefore, the instability could be reduced by lowering the oxygen partial pressure during the deposition process of the active layer followed by thermal annealing in the oxygen or water atmosphere to reduce defects.[40]

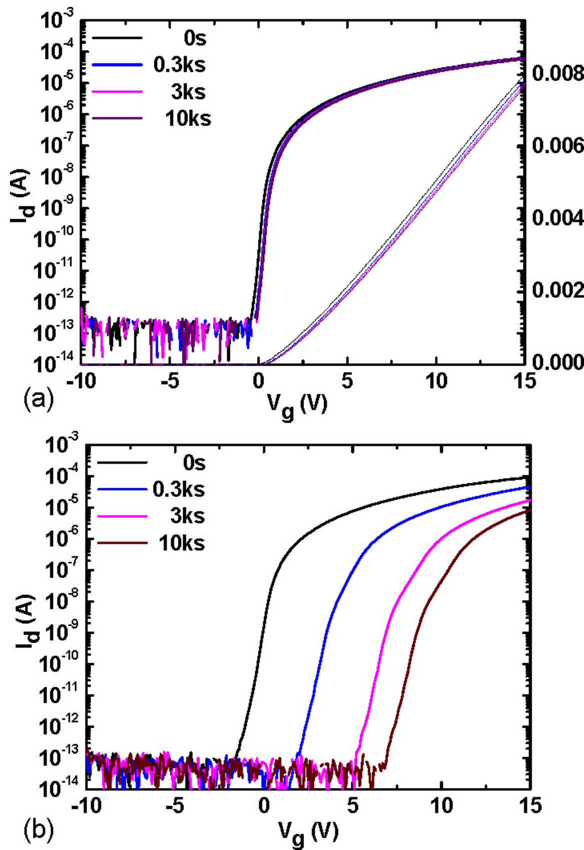

FIGURE 9 — The evolution of the transfer curves as a function of the applied-bias-stress time (W/L = 40 μm/20 μm) at room temperature (V_{gs} = 20 V) for (a) the top-gate AZTO TFT and (b) the bottom-gate AZTO TFT.

To clarify the effect, we investigated the dependency of the BG IGZO TFT bias stability on the oxygen partial pressure.[41] While the V_{th} shift for the IGZO TFT processed at the optimized oxygen partial pressure was negligible, the TFT processed at a higher oxygen partial pressure shifted to the positive direction by +2.2 V with the absence of SS variation under a bias stress for 10,000 sec at V_g = 20 V. The result may be explained in two different ways as follows. Firstly, an optimum or smaller amount of oxygen would reduce the negatively charged oxygen plasma damage on the insulator, which in turn lowers the trap density in the gate insulator and/or at the interface. Secondly, sputtering at higher oxygen pressure could create more acceptor-like defects, *e.g.*, metal vacancies, in the channel which would easily transform to fixed negative charges after trapping electrons. The fixed negative-charge trapping would have an effect of screening the applied positive gate voltage, which is then manifested as a shift in V_{th} in the positive direction. We are still investigating the origin of the large V_{th} shift for the device processed at a high oxygen partial pressure.

5 Light stability of oxide TFTs

Although oxide TFTs with high mobility and high stability have been made feasible with the development of materials and process technologies, there still remains the issue of intrinsic instability for the light illumination. For display applications, it is inevitable for TFTs to be exposed to the light from the backlight in LCDs or the self-emitted light in OLEDs or outdoor daylight, which makes it crucial to evaluate the light stability of oxide TFTs properly in each case. The light response of oxide TFTs has been mostly attributed to the defect creation followed by the new carrier generation in the channel and/or the charge trapping in the dielectric.[42]

There are several concerns about the light stability of oxide TFTs for the application to display backplanes. The first is the stability under ambient light. Despite of the wide band gap of oxide semiconductors, they show response to the UV-visible light. When visible light was irradiated on a ZTO TFT in the absence of bias stress, V_{th} and μ_{FE} decreased and the degree of change was dependent on the light intensity and wavelength.[43] As the light intensity was increased, V_{th} became saturated with increased off-current. In addition, the shorter the wavelength, the higher the level of off-current became. These V_{th} shifts completely recovered in

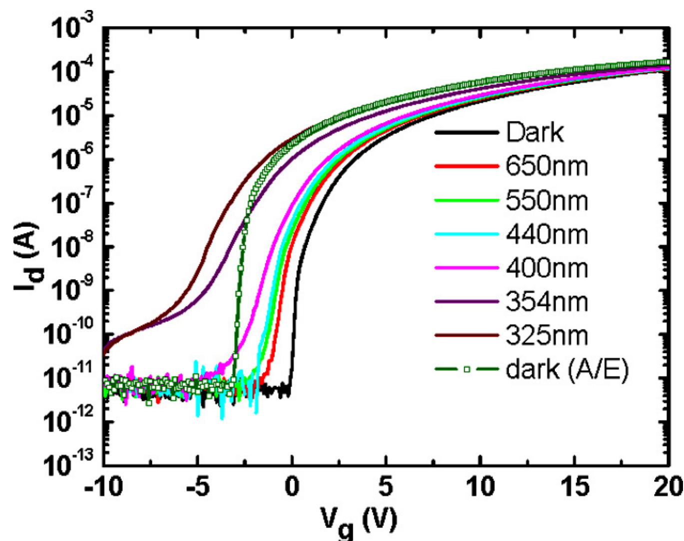

FIGURE 10 — The transfer curves of top-gate AZTO TFT upon illumination for a different wavelength of light (W/L = 40 μm/20 μm) at room temperature.

20 hours at room temperature after the light was turned off. The authors attributed the V_{th} shift to the charge trapping in the dielectric and the defect creation in the channel material. These type of light responses of oxide TFTs were also reported by other groups.[44,45] Although the mobility change during light stress was dependent on each group's device, a common result was the V_{th} shift with an increase in off-current as shown in Fig. 10. Takechi *et al.* compared the UV light response for a BG IGZO TFT and a-Si TFT. Compared to a-Si TFT, the oxide TFT showed 5–6 orders of magnitude higher off-current with a significantly negative V_{th}. This TFT showed a fast recovery followed by a very slow recovery after light was turned off.[45] According to their explanation, this unique recovery behavior begins with the generation of localized holes and oxygen vacancies by light illumination, which provide free electrons and interstitial O atoms The fast recovery is ascribed to the fast recombination of electron–hole pairs. On the other hand, the slow recovery might result from the structural change involving the recombination of electrons, oxygen vacancies, and O interstitials. For these non-passivated bottom-gate IGZO TFTs, we need to examine the environmental effect on the TFTs under light illumination as in the gate-bias-stress stability. For a ZnO film, UV light illumination induced oxygen desorption from the surface of ZnO film, which resulted in an increase in the electron density on the surface.[46] This phenomenon occurs exactly in the same manner as in a non-passivated TFT to cause a negative shift of V_{th} and the reverse reaction would occur immediately when the light is turned off. Immediate oxygen re-adsorption would happen simultaneously with the electron–hole recombination.

The second issue is the negative-bias-stress (NBS) enhanced light instability. For TFT-LCDs, the switching TFTs keep the off-state for a much longer time under a negative bias than the on-state under a positive bias, with backlight illumination. Therefore, we have to carefully investigate the light effect on an oxide TFT under negative bias stress for the application to TFT-LCDs. Our group reported the bias stability of a transparent ZnO TFT under visible light illumination.[42] While the ZnO TFT did not show any change in the transfer curve under positive bias stress with a 1-mW/cm^2 power density of green light illumination, it showed a dramatically shifted V_{th} in a negative manner under negative bias stress with light illumination. The authors ascribed this huge negative shift to the hole trap at the interface and/or in the gate insulator. The large negative shift of V_{th} under negative bias with light has been reported by an other group as well.[47] When we compare the V_{th} shift under a negative bias with and without light illumination for the top-gate IGZO TFT, the shift is much larger with light illumination, which confirms that NBS enhances the negative V_{th} shift under light illumination as shown in Fig. 11.

Generally, the negative V_{th} shift of an oxide TFT can be described in terms of the increase of a shallow donor or/and hole trapping in the gate insulator. Ha *et al.* reported the effect of thermal annealing on the 24 mW/cm^2 power of sun-light-enhanced negative-bias instability of an IGZO TFT.[47] Considering the negative V_{th} shift, decreased by thermal annealing, under NBS with and without light illumination, they attributed the improvement of stability to the reduction of oxygen-vacancy defects at the interface. Meanwhile, Lee *et al.* explained the acceleration of negative

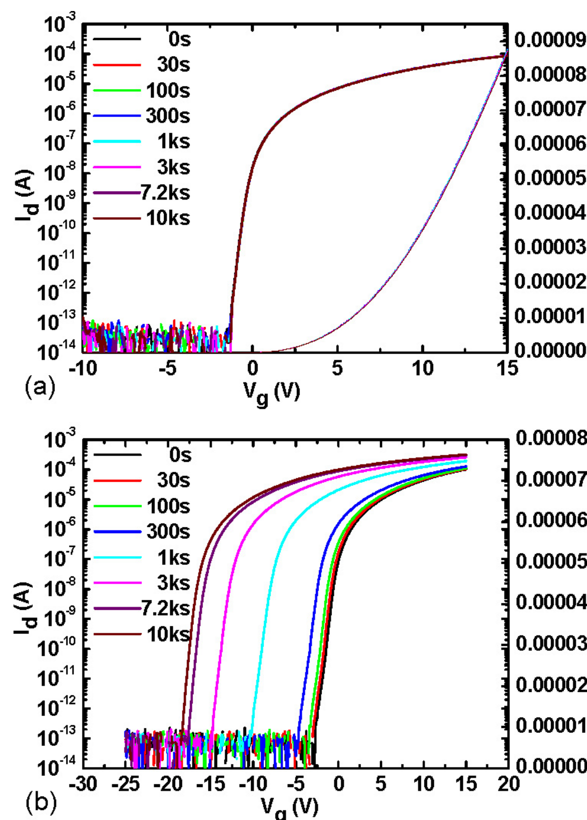

FIGURE 11 — The evolution of the transfer curves for the top-gate IGZO TFT as a function of the applied gate-bias-stress time (W/L = 40 μm/20 μm) at room temperature (V_{gs} = −20 V): (a) dark condition and (b) under illumination by halogen lamp (power: 100 μW/cm^2).

V_{th} shift under NBS with halogen-lamp illumination by the photo generation of carriers and subsequent positive-charge trapping in the gate insulator.[48] Especially, they suggested that environmental water generates metastable gap states, leading to an increase in hole carriers followed by the negative V_{th} shift due to the hole trap in the gate insulator. There could be another explanation for water effect on the NBS instability under light illumination. Water can transfer electrons to the holes generated by light, which induces the accumulation of positively charged water species in the channel to result in the negative V_{th} shift.[13] When we elucidate the mechanism of NBS-induced light instability, it would be very important to take into account together various characteristics of an oxide TFT such as bias stability, light stability under different wavelength illumination, and recovery behavior after the light is turned off. Sometimes electrically unstable device shows ostensibly better performance under light stress by trapping electrons at the interface and/or in the gate insulator. Apparent V_{th} shift under NBS with light may simply be explained by the increase of shallow donors or/and hole trapping. If the negatively shifted transfer curve would not be recovered without thermal annealing after long light stress, we may have to suspect any irreversible change in the active layer itself and look for the cause. If the recovery is made at room temperature, it may mean that a reversible change occurred in the active layer during the light and negative bias stress. Furthermore, when a device is sensitive even to red or green light, the origin of light instability could be inferred to be defects around or below the mid-gap related to oxygen vacancy or/and interface. Oxygen vacancies in the amorphous oxide semiconductor play as a deep and shallow donor.[19] A deep-level oxygen vacancy may transform into a shallow donor via the direct electron transition by green light irradiation, followed by the relaxation of positively charged oxygen vacancy. Therefore, the light response would be dependent on the amount of oxygen vacancies and the intensity of flux as explained previously.[43] Fortunately, the transition (excitation) by visible light could be minimized to result in a rather small negative shift with the reduction of oxygen vacancies or other density of states in the active layer, which can be achieved by the optimization of fabrication processes.

In the case of UV irradiation, however, the generation of holes occurs by the transition from the valence band of which the probability must be much higher than that of the transition from the defect level. Therefore, UV illumination induces much more negative V_{th} shift. What is the reason for the NBS-enhanced light instability of negative V_{th} shift? In the case of electrically stable TFTs, electrons and holes, newly generated by the light illumination under PGBS, recombine very quickly at high I_{ds} to result in less V_{th} shift. When the NGBS is applied under the same light illumination, however, electrons are mostly depleted and induce the accumulation of holes in the valence band. Some people think that these holes can be trapped at the interface or/and injected into the gate insulator directly. Meanwhile, another plausible explanation is that the hole capture by oxygen vacancy again induces the transformation of a deep donor oxygen vacancy into a shallow donor to result in a negative V_{th} shift. Considering the NBS-enhanced light instability of negative-V_{th}-shift dependency on the gate insulator material, however, both mechanisms shown above seem to work for oxide TFTs at the same time under NBS with the light illumination. We are still investigating the mechanism in detail.

The last issue in the light stability of oxide TFTs is the V_{th} shift under the constant current stress with the self-emitted light for the application to AMOLEDs. While the constant-bias-stress stability with and without light illumination has been intensively investigated, the constant current stress (CCS) stability with and without light illumination has been rarely reported. In view of CCS, oxygen-vacancy-related defects are regarded as the origin of instability, and stability can be improved by wet thermal annealing.[49] As mentioned above, the light instability under CCS is also related to the defects in the active layer and at the interface as well as the atmosphere. Therefore, for the careful evaluation of light effect, it is very important to control the ambient effect and to minimize the effect of electron trapping at the interface. We fabricated electrically stable top-gate oxide IGZO TFTs and investigated them under gate bias stress, current stress, and CCS with light illumination. Our TFT showed a positive V_{th} shift of 0.28 V without the change in mobility of 12.2 cm^2/V-sec and an S.S. of 0.21 V/dec under a 20-V stress, while the negative V_{th} shift under –20-V stress was almost negligible for 10,000 sec at dark. Under a CCS of 10 μA for 40 hours, the V_{op} change was less than +0.09 V, where V_{op} is defined as the potential between the gate electrodes connected with drain and source (we cannot monitor the change in SS in our measurement system). For AMOLEDs, the light intensity to which the TFT is exposed amounts to just about 1000 lumen/m^2 and UV comes just from outdoor daylight which can be cut off by proper design of device structure. Therefore, major concern would be the V_{th} shift due to the self-emitted light of OLED. To clarify the origin of V_{th} shift under CCS with light illumination, we used a UV-vis white light from a halogen lamp with an intensity of 100 μW/cm^2 and 531 nm of green/visible white light extracted from the halogen lamp. While the V_{op} change measured under dark condition was 0.081 V, those for UV-vis white light, visible white light, and green light illumination were –0.14, –0.05, and 0.022 V, respectively, for 21 hours of stress (with constant mobility) as shown in Fig. 12. Even UV of low intensity has a larger effect on the light/current stress than more intensive visible light. When we compare the change of V_{op} under white irradiation with that under the green irradiation, blue light appears to induce larger negative shift than green light. From Fig. 12, we can notice that there is a compensation of the negative shift by light stress with the positive shift by constant current stress. We examined the recovery behavior of transfer curve for the devices stressed under UV-vis white light and constant current for 40 hours. After fast recovery

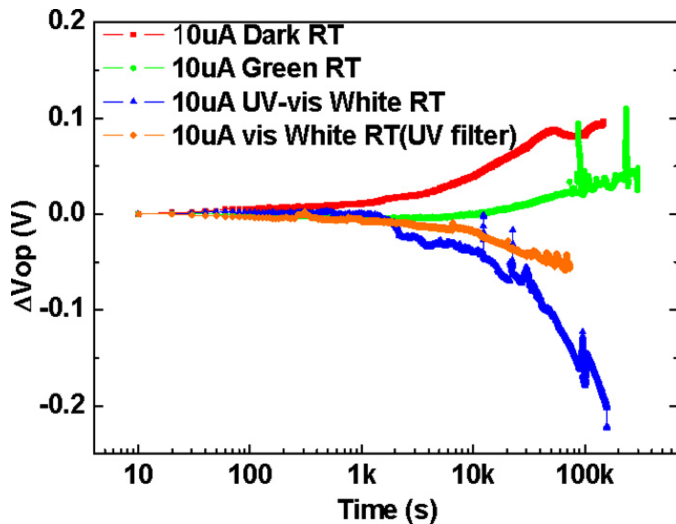

FIGURE 12 — Variation of V_{op} for the top-gate IGZO TFT as a function of an applied constant current of 10 µA (W/L = 40 µm/20 µm) at room temperature.

of just SS, it would not be recovered to the initial state without thermal annealing. If there is just the generation of electron–hole pairs and if trapped positive charges are completely de-trapped with the recombination of electrons and holes, the transfer curve should be recovered to the original condition. When light was turned off, however, the mobility remained the same, and just SS returned to the initial value of 0.16 V/decade to be apparently seen as recovered some portion. The result indicates that the long time current stress under white illumination seems to induce the creation of states near the Fermi level which is screened by an increase in Fermi level with a new generation of shallow donor right after the light turn-off, as well as the deep charge trapping or/and the generation of new shallow donor, but the amount is almost negligible. Since a top-gate oxide TFT tends to show relatively a small negative shift of V_{op} under visible light and CCS as shown earlier, we assure that our IGZO TFT is stable enough to drive AMOLEDs.

6 Summary

We have investigated several factors which affect the bias stability of oxide TFTs in terms of the device process and have presented a review on the stability. In addition, we have also presented the phenomena of light instability of oxide TFTs and have discussed the origin of light instability. Since the gate-bias stability is dependent on the degree of charge trapping at the interface or the injection into the gate insulator, the quality of gate insulator is of importance to achieve highly stable oxide TFTs. Due to the unique characteristics of oxide semiconductors of which the carrier density is increased by H incorporation, we have to carefully design the gate insulator process. In a top-gate structure, the gate insulator deposited by a plasma-free process has yielded much improved bias stability compared to that obtained by an oxygen plasma process due to the absence of charge trapping centers created from the oxygen anion bombardment during the plasma process. The decrease or increase of carriers with the adsorption or desorption of oxygen or water makes the passivation layer very important in a bottom-gate structure. The most required for high stability is a passivation layer which is dense and does not induce the H incorporation or any charge trap centers at the back channel. Device configuration is one of the variables for the total density of states which directly determines the bias stability. A top-gate device can have much improved stability compared to the bottom gate by virtue of the process sequence in which the gate insulator can be deposited on the active layer without introducing charge trapping centers. Light illumination affects the device characteristics in several ways. Despite wide band gap, oxide semiconductors show the response to light illumination. While a TFT with high electrical stability mostly shows little response to light, even to the one including UV, with and without positive bias stress, a dramatic change in the light response occurs in the presence of negative bias. We attribute the origin of NBS-enhanced light instability to increase of the shallow donors or/and hole trapping in the gate insulator. Oxygen vacancies play an important role not only in the bias stability but also in the light stability.

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