Channel-Shortening Effect Suppression of a High-Mobility Self-Aligned Oxide TFT Using Trench Structure

Junsung Kim, Do Hyung Kim, Seong-In Cho, Seung Hee Lee, Wooseok Jeong, and Sang-Hee Ko Park

***Abstract*— Channel-shortening effect (CSE) in oxide thin film transistors (TFTs) is a crucial issue that must be resolved for applications in ultra-high-resolution displays. One of the origins of the CSE is the diffusion of a shallow donor such as hydrogen from other layers into the channel. In this study, we investigated for the first time the CSE of self-aligned Al-doped In-Sn-Zn-O (Al-ITZO) TFTs with planar and trench structures. The TFTs with planar structures exhibited severe negative V_{ON} shifts after an annealing process, whereas the TFTs with trench structures were barely affected, thereby exhibiting excellent ON/OFF characteristics. The vertical channel in the trench TFT had higher resistance than the horizontal channel because of a back-sidewall roughness and thin channel. The high resistance of vertical channels played a significant role in determining the ON/OFF characteristics of Al-ITZO TFT, where V_{ON} remained constant until the diffused shallow donors made the resistive vertical channels become conductive. Based on these unique operation characteristics, the suppression of CSE in a trench TFT was demonstrated even under a high annealing temperature. Trench TFT exhibited higher mobility, higher drain currents, and higher stability than planar TFT, thus making it suitable for ultra-high-resolution displays.**

***Index Terms*— High current, high stability, suppressing channel-shortening effect, trench structure.**

I. Introduction

OXIDE thin film transistors (TFTs) are used as backplane devices for active-matrix (AM) displays because of their excellent electrical properties and a scalable process [1], [2]. However, to achieve the extended reality using current-driven displays, it is essential to utilize an ultra-high-resolution display driven by TFTs with a smaller size, higher mobility, higher drain currents, and higher stability than conventional TFTs [3]–[5].

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When the TFT is minimized by shortening the channel length, a channel-shortening effect (CSE) occurs because of the diffusion of shallow donors such as hydrogen (H) into the active layer, which deteriorates the on/off characteristics [6]. In particular, even a slight carrier diffusion causes an abrupt V_{ON} shift in high-mobility oxide TFTs [7], [8]. Therefore, the methodology for the suppression of CSE is essential.

In this study, we introduced a trench structure into an Al-doped In-Sn-Zn-O (Al-ITZO) self-aligned (SA) TFT to implement a high-current driving capability and well-behaved TFT by suppressing the CSE. Moreover, we simultaneously fabricated a planar SA TFT on the same substrate to compare the electrical characteristics of the two devices.

Finally, we fabricated trench TFTs whose switching characteristics are less affected by H diffusion and the high temperature annealing process compared to planar TFT. Trench TFT has higher mobility, higher stability, and higher drain currents than planar TFT, which makes it appropriate for next-generation ultra-high-resolution displays.

II. Experimental Procedure

Figure 1(a) shows the schematic diagrams of two different types of self-aligned TFTs: a planar structure (left) and trench structure (right). First, a 500 nm-thick SiO_2 buffer was thermally grown on a Si wafer. For the trench TFT, trench holes with a depth of 200 nm were patterned on SiO_2 and all processes of the two devices were carried out simultaneously, except for the hole etching process. A 30 nm-thick high mobility oxide semiconductor, Al-ITZO [9], was deposited on SiO_2 as an active layer using the RF sputtering method at room temperature. Next, a 100 nm-thick layer of SiO_2 using plasma-enhanced chemical vapor deposition (PECVD) was deposited at 300 °C as the gate insulator (GI) and 150 nm-thick sputtered molybdenum (Mo) was deposited as the gate electrode. Subsequently, the samples were pre-annealed under vacuum at 280 °C for 2 h. Pre-annealing process was performed to exclude the effect of H coming from the GI during the post-annealing process after device fabrication.

After sequentially patterning the gate electrode and GI using the gate electrode shape as a mask, the active layer was exposed to Ar plasma treatment for 60 s at 100 W. Ar plasma treatment was performed to reduce the contact resistance between the active layer and source/drain (S/D) electrodes by making n^+ S/D extension regions. Thereafter,

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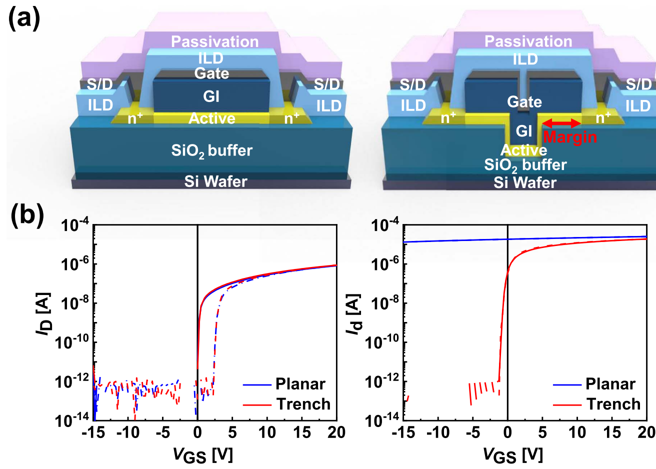

Fig. 1. (a) Schematic diagrams of planar SA TFT (left) and trench SA TFT (right). (b) Transfer curves of planar and trench TFTs before annealing (left) and after annealing at 270 °C (right). Gate voltage (V_{GS}) swept from −15 to 20 V (solid lines) and again swept from 20 to −15 V (dashed lines).

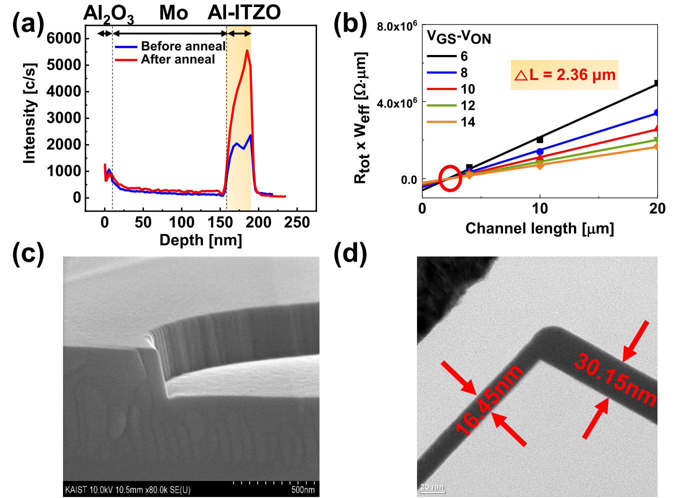

Fig. 2. (a) Depth profile of −OH element before and after annealing at 270 °C. (b) TLM analysis of planar TFT after annealing at 260 °C. (c) SEM image of trench hole. (d) TEM image of vertical and horizontal channels in trench TFT.

the 100 nm-thick PECVD SiO_2 was deposited at 270 °C as an interlayer dielectric (ILD). A 150 nm-thick molybdenum, which is a widely used S/D electrode material [10], [11], was deposited by sputtering method. Finally, a 10 nm-thick Al_2O_3 was deposited at 200 °C using atomic layer deposition (ALD) as a passivation layer. For Al_2O_3, trimethylaluminum and H_2O were used as Al and oxygen sources, respectively.

To compare the electrical performance of the planar and trench TFTs, they were both annealed at 260 and 270 °C under vacuum for 1 h after device fabrication. Subsequently, the transfer characteristics of the TFTs were measured at a drain voltage (V_{DS}) of 0.1 V. The measured width and length of the channel were 20 and 10 μm, respectively. The channel length of the trench TFT by combining the two vertical channels was 10.4 μm. We defined the length from S/D extension regions to the vertical channel as the "margin," shown in Fig. 1(a), and all measurements were performed on trench TFTs with a margin of 4 μm.

The roughness of the vertical part of the trench hole and thickness of the vertical and horizontal channels were observed by scanning electron microscopy (SEM) and transmission electron microscopy (TEM), respectively. The amount of −OH in Al-ITZO was detected using secondary ion mass spectroscopy (SIMS). For SIMS, 30 nm of Al-ITZO, 150 nm of Mo, and 10 nm of Al_2O_3 were sequentially deposited on the Si wafer. The amount of channel-shortening was measured by the transmission line method (TLM). Finally, the positive bias temperature stress (PBTS) stability and the negative bias temperature stress (NBTS) stability were measured at 60 °C for 1 h under a gate bias stress of 1 and −1 MV/cm, respectively.

III. Results and Discussion

Figure 1(b) shows the transfer curves of the planar and trench TFTs before (left) and after annealing at 270 °C (right). The transfer characteristics of both TFTs before annealing were almost identical and V_{ON} was 0 V with a hysteresis of 2.25 V for both TFTs. However, the trench TFT exhibited on/off characteristics with V_{ON} of −1.25 V and hysteresis of 0 V, whereas the planar TFT showed almost conductive behavior after annealing at 270 °C.

Jeong *et al.* reported the CSE caused by H diffusion from the Al_2O_3 passivation layer to the channel through S/D electrodes [7]. Therefore, we conducted a SIMS analysis to examine the CSE in planar TFTs. Figure 2(a) shows the depth profile of the −OH concentration at the position of the active layer in contact with the Mo S/D and Al_2O_3 passivation before and after annealing at 270 °C. The −OH concentration in Al-ITZO increased after annealing. The diffused H combines with oxygen in the channel to form −OH groups to release free electrons [12]. Finally, the diffused H decreases the channel resistance from the S/D extension regions and causes the CSE.

As shown in Fig. 2(b), we conducted a TLM analysis to determine the channel-shortening length. The effective channel length $L_{eff}(= L - \Delta L)$ can be obtained from the following equation:

$$R_{tot} = \frac{V_{DS}}{I_{DS}} = R_{Ch} + R_C = \frac{L - \Delta L}{W \mu C_{OX}(V_{GS} - V_T - \frac{V_{DS}}{2})} \quad (1)$$

where R_{tot}, R_{ch}, R_c, L, ΔL, W, μ, and C_{ox} are the total resistance, channel resistance, contact resistance, design channel length, channel-shortening length, channel width, mobility, and gate insulator capacitance, respectively. The value of ΔL was 0.30 μm before annealing and 2.36 μm after annealing at 260 °C, which indicates that ΔL increases during the annealing process.

However, the trench TFT exhibits much less negative shift of V_{ON} than the planar TFT after the annealing process. Figure 2(c) shows the SEM image of the SiO_2 buffer with a trench hole. We can observe a certain roughness in the vertical part of the trench hole, whereas the horizontal part has a smooth surface. Therefore, the vertical channel has a lower carrier mobility and higher resistance because of a carrier scattering effect [13].

Moreover, as shown in the TEM image in Fig. 2(d), the vertical channel thickness is 16.45 nm, which is approximately half the thickness of the horizontal channel owing to the step coverage of the sputtering method. As the channel thickness decreases, the resistance increases in oxide semiconductors [14], [15]. The higher resistance vertical channels play a significant role in determining the on/off characteristics of the trench TFT [5], [6]. Consequently, owing to the roughness

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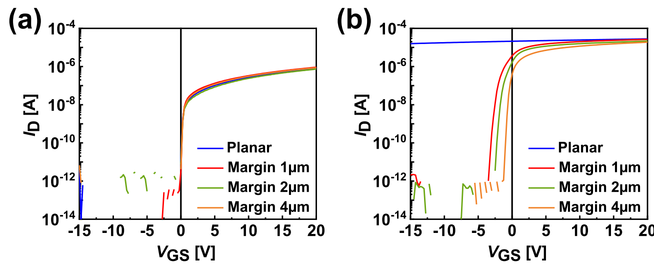

Fig. 3. Transfer curves of planar and trench TFTs with different margins (a) before annealing and (b) after annealing at 270 °C. V_{GS} swept from −15 to 20 V.

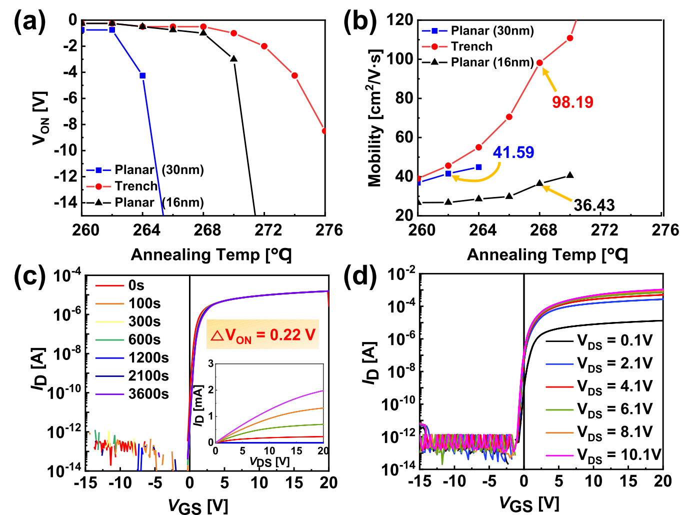

Fig. 4. (a) V_{ON} and (b) mobility of planar (T_{ch} = 16 nm, 30 nm) and trench (vertical T_{ch} = 16 nm) TFTs after annealing at 260 to 276 °C. (c) Transfer curves of trench TFT under PBTS condition after annealing at 268 °C. Inset in Figure 3 (c) illustrates the output characteristics of trench TFT after annealing at 268 °C. (d) Transfer curves of trench TFT after annealing at 268 °C for various V_{DS}.

of the back sidewall and thin thickness of the vertical channel, V_{ON} remains constant until the diffused H increases the carrier amount in the vertical channel to be conductive.

Figures 3(a) and (b) show the transfer curves of planar and trench TFTs with margins of 1, 2, and 4 μm before and after annealing at 270 °C, respectively. The diffusion length of H from S/D extension regions to the vertical channels increases with an increase in the margin. Therefore, the shift of the V_{ON} with a greater margin decreases after the annealing process.

In order to measure the TFT characteristics in smaller steps, we measured the transfer characteristics of planar and trench TFTs while increasing the annealing temperature from 260 to 276 °C in increments of 2 °C. Figures 4(a) and (b) show the V_{ON} and mobility of the TFTs after the annealing process, respectively. The optimum temperature at which the highest mobility is achieved with negligible V_{ON} shift and hysteresis is 262 °C for planar TFT and 268 °C for trench TFT. At each optimum temperature, the V_{ON}, mobility, and drain current of planar TFT are −0.75 V, 41.59 cm^2/Vs, and 5.05 μA (V_{GS} = 20 V), respectively, and those of trench TFT are −0.5 V, 98.19 cm^2/Vs, and 14.9 μA (V_{GS} = 20 V), respectively.

As shown in the SIMS and TLM analyses, the amount of −OH in the channel increases with rise in annealing temperatures. Because H acts as a shallow donor, the carrier concentration in the channel increases, resulting in increased mobility and current [16]. The decrease in the disorder of Al-ITZO film during the annealing process is also one reason for the increase in mobility and current [17]. Furthermore, the current and apparent mobility of the trench TFT could be enhanced by making the certain part of the channel conductive [5], [18]. As a result, trench TFT exhibits a high mobility close to 100 cm^2/Vs and high drain current after annealing at 268 °C.

To scrutinize the influence of Al-ITZO thickness and buffer layer roughness on TFT characteristics, we also fabricated planar TFT with a channel thickness (T_{ch}) of 16 nm. This is for the TFT with just the same channel thickness as that of vertical channel of trench TFT, but there is no back-sidewall roughness. As shown in Fig. 4(a), the V_{ON} shift of planar TFT (T_{ch} = 16 nm) is smaller than that of planar TFT (T_{ch} = 30 nm), but larger than that of trench TFT (vertical T_{ch} = 16nm). This is because the 16 nm-thick channel has higher resistance than the 30 nm-thick channel, but has lower resistance than the 16 nm-thick vertical channel with roughness.

Figure 4(c) shows the transfer curves of the trench TFT after annealing at 268 °C under a positive bias stress of 10 V (1 MV/cm) at 60 °C for 1 h. The trench TFT exhibited excellent PBTS stability with a V_{ON} of 0.22 V, whereas planar TFT showed poor PBTS stability with a V_{ON} of 2.34 V (data not shown) at the optimum temperature. In oxide TFTs, charge-trapping defect states in the channel and at the channel–GI interface are reduced during the annealing process [19]. Moreover, the defect in the channel is passivated when H diffuses into Al-ITZO [20]. Therefore, trench TFT, which exhibits switching characteristics even at higher annealing temperature, shows higher PBTS stability than planar TFT. In addition, the trench TFT showed high NBTS stability with a V_{ON} of 0.25 V (data not shown).

The inset in Fig. 4(c) shows the output characteristics of trench TFT after annealing at 268 °C for various V_{GS} (0, 5, 10, 15, and 20 V). There is no current crowding at low V_{DS}, which indicates that there is no contact issue between the S/D electrodes and Al-ITZO. Figure 4(d) shows the transfer curves of trench TFT after annealing at 268 °C for various V_{DS} (0.1, 2.1, 4.1, 6.1, 8.1, and 10.1 V). Trench TFT shows excellent transfer characteristics even at higher V_{DS}.

Consequently, we fabricated high-mobility trench TFT that suppresses the CSE during high-temperature annealing to simultaneously attain high stability and high current driving capability.

IV. Conclusion

In summary, CSE was investigated in the planar and trench structures of self-aligned Al-ITZO TFTs. The planar TFT exhibited a huge negative shift of V_{ON} after the post-annealing process because of CSE, whereas the V_{ON} of trench TFT was barely moved. The vertical channel in the trench TFT has a higher resistance than the horizontal channel because of the back-sidewall roughness and thin channel. Therefore, the vertical channel is dominant in determining the on/off characteristics, and V_{ON} remains constant until the channel-shortening affects the vertical channel. Based on these unique characteristics, we fabricated trench-structure TFTs with a high current driving capability and excellent PBTS stability, while maintaining stable on/off characteristics. These results demonstrate that high-mobility trench TFTs are suitable for next-generation ultra-high-resolution displays.

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