Applied Physics Letters

Transition of dominant instability mechanism depending on negative gate bias under illumination in amorphous In-Ga-Zn-O thin film transistor

Cite as: Appl. Phys. Lett. **98**, 033504 (2011); https://doi.org/10.1063/1.3540500
Submitted: 09 November 2010 . Accepted: 22 December 2010 . Published Online: 18 January 2011

Himchan Oh, Sung-Min Yoon, Min Ki Ryu, Chi-Sun Hwang, Shinhyuk Yang, and Sang-Hee Ko Park

Appl. Phys. Lett. **98**, 033504 (2011); https://doi.org/10.1063/1.3540500 **98**, 033504

APPLIED PHYSICS LETTERS **98**, 033504 (2011)

Transition of dominant instability mechanism depending on negative gate bias under illumination in amorphous In-Ga-Zn-O thin film transistor

Himchan Oh,[a)] Sung-Min Yoon, Min Ki Ryu, Chi-Sun Hwang, Shinhyuk Yang, and Sang-Hee Ko Park
Oxide Electronics Research Team, Electronics and Telecommunications Research Institute, Daejeon 305-700, Republic of Korea

(Received 9 November 2010; accepted 22 December 2010; published online 18 January 2011)

The gate bias dependence on the negative bias instability under illumination was examined. As the gate bias got more negative, dominant mechanism was changed from simple charge trapping to that accompanied by generation of subgap states. Degree of threshold voltage shift was not monotonously dependent on the magnitude of negative gate bias. It is strongly related with the corresponding instability modes for different gate bias regimes. The transition of instability mechanism depends on how much the gate bias stabilizes ionized oxygen vacancy states. © *2011 American Institute of Physics*. [doi:10.1063/1.3540500]

Reliability issues on the thin film transistors (TFTs) adopting amorphous oxide semiconductor (AOS) as the active layer have been intensively studied in recent years. As results, mechanisms of instabilities caused by applied gate bias stress only and that combined with temperature and/or environmental effects have been revealed.[1–4] Indeed, there have been reports on the fabrication of extremely stable devices under aforementioned stress conditions also.[7] Nevertheless, the device which is highly reliable under light exposure has not been achieved. Especially, negative bias instability (NBI) under illumination remains as one of the most severe problems in AOS TFTs.[5–8] This might be the last hurdle in AOS to realize AOS TFT-driven active matrix organic light emitting diode (AMOLED), liquid crystal display, and innovative transparent electronics, since TFTs are exposed to light during their operation. Thus, it is important to understand the mechanism of NBI under light illumination to resolve it.

From the previous studies on the NBI under illumination, three mechanisms responsible for the threshold voltage shift have been proposed: (i) environmental effects,[6,7] (ii) simple charge trapping of photogenerated holes at the gate insulator (GI)/semiconductor interface or injection of them into GI bulk[6,8] and (iii) that combined with defect state creation in the channel layer.[9] The environmental effects could accelerate the NBI. But they would be ruled out by proper passivation layer on the active layer.[7] Thus, the latter two mechanisms are the possible candidates for the degradation process.

The simple charge trapping of photogenerated holes has been mostly reported as the mechanism for the threshold voltage shift by negative bias stress (NBS) under illumination.[6,8] However, the rigid shift of transfer curve with insignificant changes in field-effect mobility (μ_{FE}) and subthreshold swing (SS) can be observed by the NBS with light exposure even accompanied with the generation of subgap states as reported in our previous publication.[9] Interestingly, we recently found that the instability behavior and dominant mechanism were changed from the charge trapping to that combined with the creation of sub-gap states as gate bias got more negative.

In this letter, we report the gate bias dependence on the NBI under illumination in amorphous In-Ga-Zn-O (a-IGZO) TFT. The shift in threshold voltage by the NBS under illumination is not monotonously dependent on the magnitude of applied gate insulator field (E_{ox}). It is strongly related with the instability mechanism which is changed along with the gate bias. The transition of NBI mechanism depending on the gate bias is discovered by measuring the channel capacitance characteristic which is more sensitive to the subgap defect state than the transfer characteristic.

The fabrication procedure of a-IGZO TFT has been reported in detail.[9] The fabricated TFT has a top gate and bottom contact configuration. The active layer was efficiently passivated by atomic layer deposition derived ~176 nm thick Al_2O_3 gate insulator. Therefore, we excluded the ambient effects on the NBI under illumination. The green light source was used of which intensity peaks at 530 nm and full-width-at-half-maximum at this point is 10 nm. Its photointensity is 0.2 mW/cm^2, as calibrated by photometry. The channel width/length of examined devices was 160/160 μm. All the electrical measurements were carried out at room temperature using Agilent B1500A precision semiconductor parameter analyzer and varying the gate bias from -5 to -30 V. A pristine device was used for each measurement.

Figures 1(a) and 1(b) show the evolutions of the transfer curves as a function of the same stress time under gate bias stresses of -10 and -20 V, respectively. Regardless of the applied electric field by the negative bias, parallel shifts in transfer curves with insignificant changes in μ_{FE} and SS were observed for both cases. The μ_{FE} was calculated from the maximum transconductance using $\mu_{FE}=Lg_m/WC_iV_{DS}$, where C_i and g_m are the gate capacitance per unit area and trans-conductance respectively. The subthreshold swing ($SS = dV_{GS}/d \log I_{DS}$) was extracted from the linear portion of the $\log(I_{DS})$ versus V_{GS} plot. The initial values of μ_{FE} and SS were 20 cm^2/Vs and 0.18 V/dec, respectively. After 1×10^4 s of stress time, μ_{FE} was not changed at all for both cases and SS values increased slightly to 0.22 and 0.23 V/dec for each case. Thus the instability mechanism seemed to be

---

[a)] Electronic mail: fullchan@etri.re.kr.

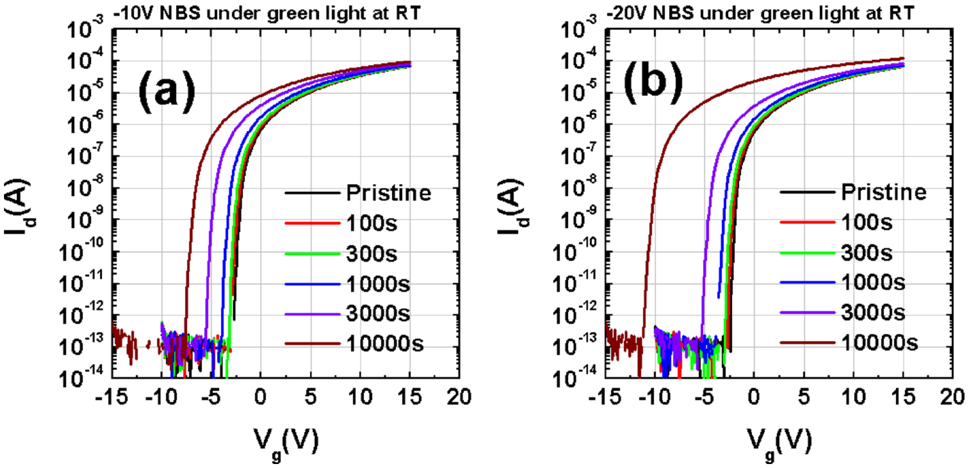

FIG. 1. (Color online) The evolutions of the transfer curves as a function of the same stress time under gate bias stresses of (a) −10 and (b) −20 V with green light exposure for 1×10^4 s.

simple charge trapping, regardless of the magnitude of electric field.

If the charge trapping causes the threshold voltage shift, higher applied electric field will induce more displacement in transfer curve. Strangely, shifts in threshold voltage were not different even the gate bias was doubled from −10 to −20 V until the stress time reached 3×10^3 s. After 1×10^4 s, the transfer curve of −20 V case shifted to negative direction drastically compared to that of −10 V case. This implies that there is another mechanism responsible for the high electric field regime, as will be discussed later. Note that, for the short term stress, low electric field causes similar degree of NBI under illumination as much as high electric field does.

Figures 2(a) and 2(b) show the evolutions of the channel capacitance-voltage (C-V) characteristics as a function of the same stress time under gate bias stresses of −10 and −20 V, respectively. Unlike the transfer curves, clear difference was observed. For the −10 V case, C-V curves shifted rigidly with little distortion. On the other hand, C-V curves for the −20 V case were largely stretched-out by the created subgap states as reported in our previous paper. Thus, it can be said that the charge trapping is dominant mechanism for the low gate bias stress and the creation of subgap state will be involved as the gate bias get more negative.

Figure 3 shows the shifts in V_{ON} (corresponding to the gate voltage that brings 10 pA of drain current with 10.1 V of drain voltage) with the same stress time under different gate bias stresses with illumination. For the small negative bias stress ($|V_G| \leq 10$ V, $|E_{ox}| \leq 0.57$ MV/cm), gate bias dependence on the ΔV_{ON} is clear, i.e., ΔV_{ON} under −10 V stress is about twice as large as that under −5 V stress for the entire stress duration. This means that the charge trapping is dominant mechanism in this gate bias regime. Time dependence of ΔV_{ON} in the low electric field regime is well described by the stretched-exponential equation which is defined as

$$|\Delta V_{ON}| = |\Delta V_{ON0}|\{1 - \exp[-(t/\tau)^{\beta}]\},$$

where ΔV_{ON0} is ΔV_{ON} at infinite time, τ represents the characteristic trapping time of carriers and β is the stretched-exponential exponent.[10] The fits to the stretched-exponential equation are shown in Fig. 3. Since this model is based on the charge trapping kinetics, excellent fit to this equation also supports that the charge trapping is dominant mechanism in the low electric field regime.

For the high electric field regime ($|V_G| \geq 15$ V, $|E_{ox}| \leq 0.85$ MV/cm), ΔV_{ON} is nearly independent on the gate bias, in contrast to the low electric field regime. We also attempted to fit the ΔV_{ON} data to stretched-exponential equation. However, discrepancy between the raw data and the fitted value was large. Before the stress time reached 3×10^3 s, time dependence and magnitude of ΔV_{ON} in high electric field regime are very similar to those of ΔV_{ON} induced by −10 V gate bias stress which follow stretched-exponential behavior well. However, deviation arisen after 1×10^4 s made the time dependence of ΔV_{ON} in high field not to follow the stretched-exponential model. It means that involving of subgap state creation plays an acceleration role for the long term NBI behavior under illumination.[9]

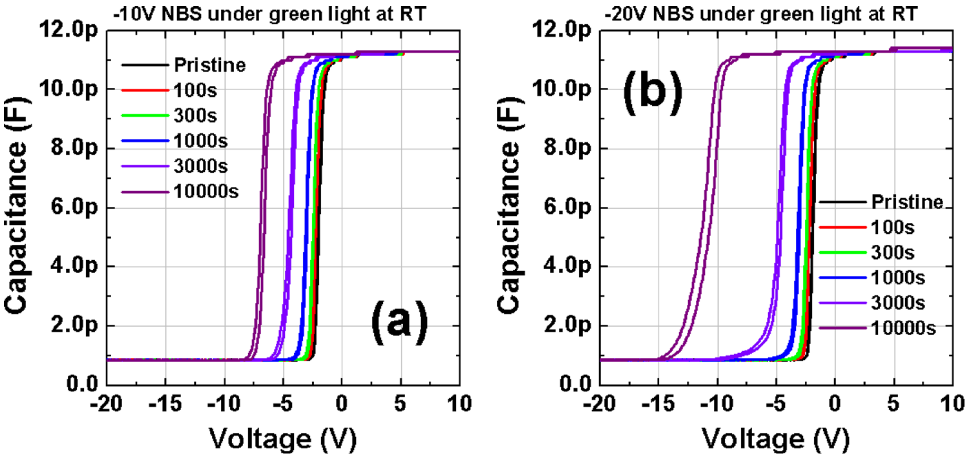

FIG. 2. (Color online) The evolutions of the channel C-V characteristics at 2 kHz frequency as a function of the same stress time under gate bias stresses of (a) −10 and (b) −20 V with green light exposure for 1×10^4 s.

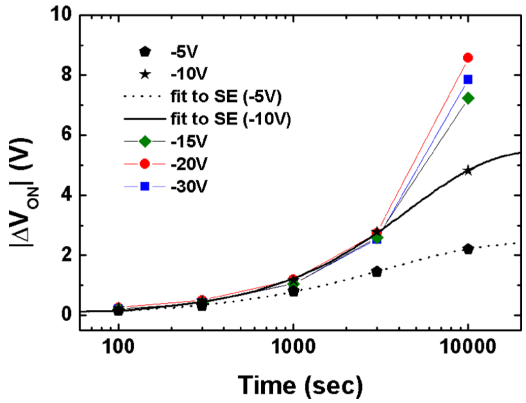

FIG. 3. (Color online) Turn-on voltage shift, ΔV_{ON} vs NBS time under green light exposure for gate bias stress voltages ranging from -5 to -30 V. The symbols represent the raw data and the curves the fits to the stretched-exponential (SE) equation.

The change in instability mechanism depending on the gate bias can be explained as follows. In spite of wider band gap than the visible light, subband photon-induced instability in a-IGZO TFT occurs via subgap states near the valence band maximum (VBM, from VBM to ~1.5 eV).[11] It has been reported that these defect-related gap states are originated from the oxygen vacancy (V_O).[12–15] Thus it can be said that the visible light induced instability starts from the photoexcitation of fully occupied neutral oxygen vacancy (V_O) to ionized V_O^+ or V_O^{2+}. For the small negative bias, Fermi level is not significantly lowered to keep the V_O^+ or V_O^{2+} states unoccupied. Thus they are unstable and neutralized soon. This neutralization is made by two possible ways as depicted in Fig. 4(a). The first way is the occupations of the photoexcited electrons from the valence band. This process yields the free holes in the valence band. Then the free holes drift toward the GI/semiconductor interface and are trapped at there or injected into GI bulk. The other way is the migration of holes in the ionized states to the adjacent V_O or V_O^+ states. If the density of V_O states is high enough, this can also be the fast pathway for the holes to move to the GI/semiconductor interface. Either way, drift velocity of photogenerated holes is dependent on the applied electric filed, resulting almost linear gate bias dependence on the ΔV_{ON} which was observed in low field regime.

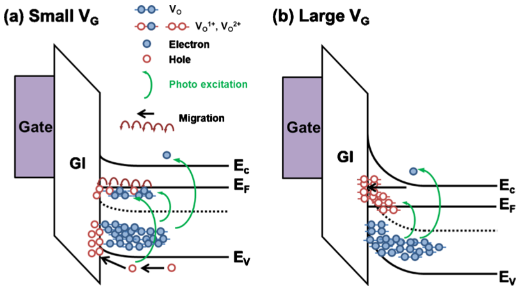

FIG. 4. (Color online) Schematic illustrations of corresponding instability mechanism for (a) small and (b) large negative bias stress. Note that, the charge trapping and the state creation occur together in different degrees for both regimes, though the more dominant mechanism between the two is depicted for each gate bias regime to avoid complexity.

If the large negative bias is applied, substantial portion of photoexcited V_O^+ or V_O^{2+} states can survive without neutralization by virtue of lowered Fermi-level. In this case, the holes are trapped in the stable V_O^+ or V_O^{2+} states. Thus the holes cannot move rather freely unlike the photon-induced holes under small negative voltage stress. This leads the nearly equal V_{ON} shift by -10 V stress compared to that by larger bias than -10 V in the initial stage of NBS test. However, much more shift was observed after long stress time. Since the migration of V_O^+ or V_O^{2+} by the applied electric field must be slower than the free holes, their effect comes late but accelerates the NBI dramatically together with the charge trapping as reported in our previous letter.[9]

In summary, we observed the change in NBI mode under illumination from the simple charge trapping to that combined with the generation of subgap states. The transition in NBI mode depends on how much the gate bias lowers the Fermi level to stabilize the ionized V_O^+ or V_O^{2++} states. If the small negative bias is applied, photoexcitation of subgap states yields free holes in valence band and/or in the group of sub-gap states. The induced holes drift toward the GI/semiconductor interface and then will be trapped at there by negative bias. For the large negative bias case, substantial portion of photogenerated holes are trapped in V_O^+ or V_O^{2++} states. Since the speed of free holes under applied negative bias is faster than V_O^+ or V_O^{2++}, the small negative bias can also cause significant ΔV_{ON} in a short time and the large negative bias brings huge ΔV_{ON} caused by accumulation of V_O^+ or V_O^{2++} at the GI/semiconductor interface after long stress time in addition to the charge trapping.

This work was supported by the Industrial Strategic Technology Development Program of MKE/KEIT. [10035225, Development of core technology for high performance AMOLED on plastic].

[1] R. B. M. Cross and M. M. De Souza, Appl. Phys. Lett. **89**, 263513 (2006).
[2] A. Suresh and J. F. Muth, Appl. Phys. Lett. **92**, 033502 (2008).
[3] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. **95**, 013502 (2009).
[4] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett. **93**, 123508 (2008).
[5] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. K. Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee, and H. Y. Chu, ETRI J. **31**, 62 (2009).
[6] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, and S. Lee, Appl. Phys. Lett. **95**, 232106 (2009).
[7] S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang, and J. K. Jeong, Appl. Phys. Lett. **96**, 213511 (2010).
[8] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon, W. Choi, M. K. Ryu, and S. Y. Lee, Appl. Phys. Lett. **96**, 262109 (2010).
[9] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. K. Park, Appl. Phys. Lett. **97**, 183502 (2010).
[10] F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).
[11] D.-Y. Cho, J. H. Kim, U. K. Kim, Y. J. Chung, J. Song, C. S. Hwang, J.-M. Lee, and S.-J. Oh, J. Phys. Chem. C **114**, 11962 (2010).
[12] H. Omura, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, J. Appl. Phys. **105**, 093712 (2009).
[13] T. Kamiya, K. Nomura, and H. Hosono, Phys. Status Solidi A **206**, 860 (2009).
[14] T. Kamiya, K. Nomura, M. Hirano, and H. Hosono, Phys. Status Solidi C **5**, 3098 (2008).
[15] B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, Appl. Phys. Lett. **97**, 022108 (2010).