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Polymeric ferroelectric and oxide semiconductor-based fully transparent memristor cell

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Abstract Employment of the memristor for the next-generation large-area electronics can be expected to release various devices with interesting functions. In this article, for the first time we proposed a fully transparent memristor cell, which was composed of one-memory thin-film transistor (TFT) and one-switch TFT using an oxide semiconducting active channel. A poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] was used as a gate insulator for the memory TFT and the channel conductance of the TFT was modulated by changing the quantity and direction of ferroelectric polarization. The fabrication procedures were designed so that the proposed transparent memristor cell could be implemented at process temperature below 200°C. It was successfully conformed that the fabricated memristor cell exhibited good TFT behaviors and modulated output characteristics programmed into the memory TFT.

1 Introduction

Since the memristor, which was initially postulated by Leon Chua as a fourth passive element [1], has been experimentally demonstrated [2, 3], various feasible applications have been energetically proposed for revolutionarily improving the conventional computing technologies. The history-dependent memory functionality of the memristor can provide us promising solutions to the high-density cross-bar memory array [4, 5], nonvolatile and reconfigurable logic elements for CMOS electronics [6, 7], programmable analog-like memory elements [8], or adaptive-learning synaptic devices for neuromorphic systems [8–11]. Among them, the artificial synaptic action for the adaptive-learning neural networks is one of the most suitable applications of the memristor, because the electrical conductance of a memristor can be incrementally modulated by controlling the quantity of charge flux flowing through it, which is very similar to a biological synapse in a human brain. The concept of the adaptive-learning means that some electrical characteristics at a specified time have adaptability according to the signals applied to the device at past moments, in which the characteristics and input signals correspond to the responses and stimuli in this artificial learning circuit.

We can find a feasible analog synaptic memory demonstration of solid-state thin-film memristor exploiting the electrochemical effect in WO_3 in early works [12]. Although the memristive functions have been reported in systems of various materials, such as binary oxides [13, 14], perovskite-type oxides [15, 16], conducting filament type alloys [17, 18], magnetic [19, 20] and organic [21, 22] thin films so far, oxide or organic thin films with ferroelectricity have also a great potential to implement the analog-like synapse devices. H. Ishiwara proposed an adaptive-learning neuron circuits with ferroelectric-based synaptic weights [23] and his concept was experimentally verified as the ferroelectric-based neuron circuit which was composed of the field-effect transistor (FET)-type synapse using an oxide ferroelectric gate insulator and the CMOS oscillator-type neuron [24]. This approach is very preferable to design the

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learning algorithm and to build the neuron circuit in a very simple manner, because the quantity of polarization reversal and corresponding field-effect-driven channel conductance are completely reversible and accurately defined. Although these memristor-based neuron computing methodologies were initially proposed for the breakthrough of conventional Si-based CMOS electronics facing many technological and physical limitations, they can be also expected to be a very useful component for the new paradigm of future electronics implemented on the flexible plastic and/or transparent glass substrates. In this article, we propose new method to realize the fully transparent memristor device by providing a memory thin-film transistor (MTFT) using an organic ferroelectric gate insulator and an oxide semiconductor active channel. Two-transistor (2T)-type memristor cell was newly proposed, which was composed of an MTFT and a switching transistor using an oxide channel. Fabrication process was developed to integrate the transparent memristor cell on the glass substrate and its feasibility was successfully demonstrated.

2 Ferroelectric-based memristor cell

The adaptive-learning function of the ferroelectric field-effect-based MTFT can be realized by controlling the polarization value of the ferroelectric gate insulator. The channel resistance of the memristor can be gradually changed by applying an adequate number of input pulses, in which the duration time (pulse width) should be sufficiently shorter than the switching time for polarization reversal of the employed ferroelectric material. The summation operation of the "synaptic weights" can be performed by parallel connection of the ferroelectric MTFTs. The ferroelectric polarization of each synapse is differently defined by accepting the pulse signals from different neurons in the previous layer and the total drain current summed up for all synapses gives the operated result. These adaptive-learning functions [25] and weighted-sum operations [26] were previously demonstrated for the ferroelectric-gate FET using oxide ferroelectric materials such as $SrBi_2Ta_2O_9$ fabricated on the Si substrate. However, the use of oxide ferroelectric materials may be critically unfavorable for the large-area electronics in such viewpoints as their high crystallization temperature (typically higher than 650°C) and the high dielectric constant (typically 100 or higher). The first issue is related to the undesirable interfacial reaction with the Si substrate during the thermal process, which seriously degrades the interface quality. The available substrate is also severely limited. Although the interface degradation can be suppressed by inserting an insulating buffer layer between the ferroelectric gate insulator and Si, in this structure, the mismatch of maximum induced charge between the ferroelectric and inserted buffer insulator layers should be considered [27]. That is, we cannot apply a sufficient program voltage to the ferroelectric layer before the buffer insulator experiences its dielectric breakdown owing to the high dielectric constant of oxide ferroelectric gate insulator. In these viewpoints, the organic ferroelectric materials can offer attractive solutions because their crystallization temperature and the dielectric constant are much lower than those of oxide ferroelectric materials. On the glass or flexible substrates, the ferroelectric MTFTs can be designed and fabricated, as shown in Fig. 1(a). Similarly, the remnant polarization of organic ferroelectric gate insulator can be so controlled as to have given partially reversed states by changing the numbers or total width of input pulses, as schematically shown in Fig. 1(b). The resultant programmed drain currents of the TFT are varied according to each polarization state. These operations are very suitable for the pulse frequency modulation (PFM)-type learning system.

Although most works on the fabrication and characterization for the MTFTs employing the organic ferroelectric materials have been focused for the all-organic devices using organic semiconducting active layers [28, 29], the employment of oxide semiconductor as an active channel can be a powerful approach for enhancing the device performances [30, 31]. We have previously characterized the memory TFT using a poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] gate insulator and a indium-gallium-zinc oxide (IGZO) active channel, which are typical materials of organic ferroelectric and oxide semiconductor, respectively [32]. For the case of MTFT with Al/150 nm P(VDF-TrFE)/4 nm Al_2O_3/10 nm IGZO structure, the variations in the drain current values initially programmed into the *on* and *off* states were demonstrated in Fig. 1(c) when the pulse widths of programming voltage were changed from 50 to 990 ms. The pulse amplitudes for *on* and *off* were fixed at 15 and −15 V, respectively, that correspond to excitatory and inhibitory signals for the adaptive-learning memristor application. The programmed currents of the *on* and *off* states gradually increased and decreased with the increase in applied pulse width, respectively. These results suggest that the channel resistance of this device can be dynamically modulated by controlling the total duration time and polarity of the input pulses. However, in exploiting the flux-controlled partial polarization of ferroelectric gate insulator, we have a critical drawback that the minor (unsaturated) hysteresis loops having partially reversed ferroelectric polarization fatally show a weak immunity against the depolarization field during the data retention period [27]. Eventually, the use of saturated ferroelectric hysteresis loop is absolutely desirable to obtain a sufficient retention time of stored information. The 2T-type memristor cell can effectively avoid this problem which is one of the most troublesome issues for the ferroelectric-based analog-like resistive

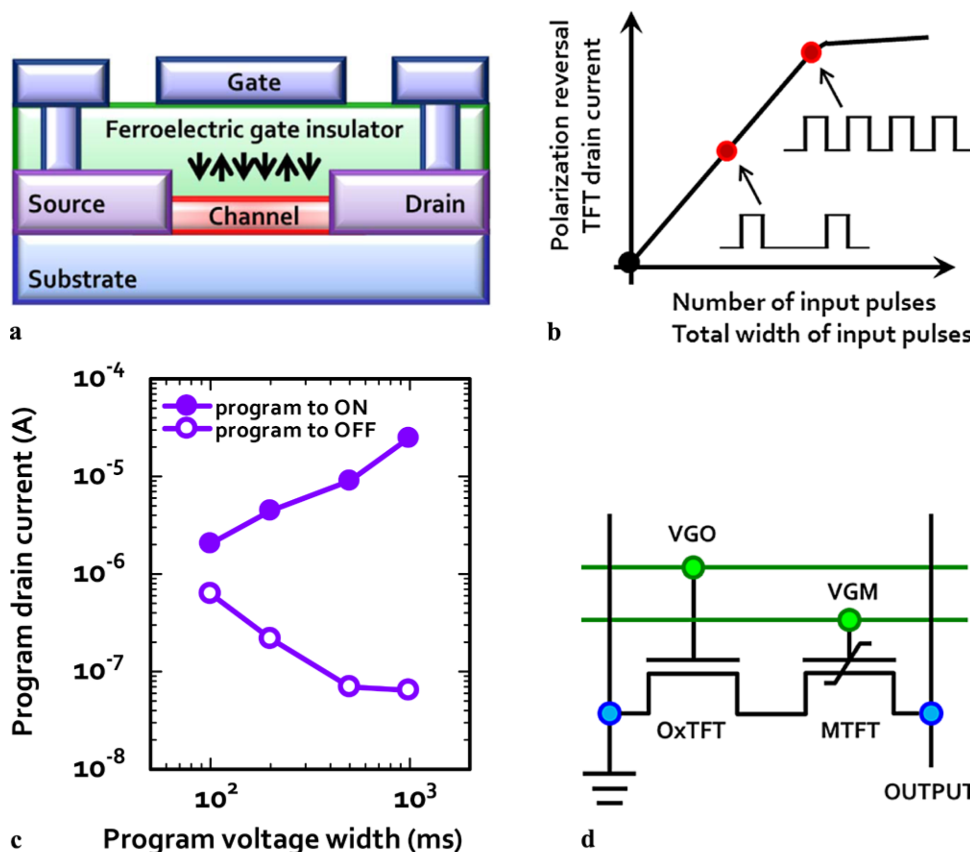

Fig. 1 (**a**) Schematic cross section of the ferroelectric-based memory thin-film transistor. The *arrows* indicate the given state of partially reversed polarization in the ferroelectric gate insulator. (**b**) For the PFM-type adaptive-learning system, the ferroelectric polarization reversal and resultant programmed drain currents of MTFT are incrementally modulated with the increase in total number or pulse-width of applied input pulses and reached the saturation point. (**c**) Typical example of gradually increasing and decreasing programmed currents for the ferroelectric MTFT with the variations in the applied pulse width, which was measured for the MTFT with Al/150 nm P(VDF-TrFE)/4 nm Al_2O_3/10 nm IGZO structure that was previously fabricated in Ref. [32]. (**d**) Two-transistor-type memristor cell structure composed of one ferroelectric MTFT and one switching oxide TFT. V_{GO} and V_{GM} correspond to the drive and programming gates for the memristor cell, respectively

memory devices. Figure 1(d) describes the schematic circuit diagram of the proposed memristor cell composed of one ferroelectric MTFT and one switching oxide channel TFT (OxTFT).

3 Cell fabrication

In order to fabricate the 2T-type transparent memristor cell on the glass substrate, the integration procedures should be carefully designed. Figure 2 provides the optimized process flow for fabricating the transparent memristor cell, in which OxTFTs can be also utilized to compose the driver peripheral circuitry for the integrated circuit. 150 nm thick indium-tin oxide (ITO) glass with the size of 10×10 cm^2 was used as a transparent substrate. At the first step, followed by the patterning of ITO for the formation of source and drain (S/D) electrode regions, a 10 nm thick oxide active channel of IGZO was deposited by radio-frequency magnetron sputtering system with a single target. Then 6 nm thick interface controlling layer of Al_2O_3 was prepared by atomic layer deposition (ALD) method using trimethylaluminium (TMA) and water vapor at 200°C, which can be termed as the first gate insulator [32, 33]. Active and interface layers were patterned into the channel regions by using dilute hydrofluoric acid solution [Fig. 2(a)]. The ferroelectric gate insulator was formed by spin-coating using a 2.5 wt% dilute solution of P(VDF-TrFE) (70/30 mol%) in methyl-ethyl-ketone. Resultant film thickness was observed to be approximately 150 nm. The prepared P(VDF-TrFE) film was crystallized by performing the thermal annealing process at 140°C for 1 hour in an ambient air. Then given areas of the P(VDF-TrFE) layer were removed to prepare the space of oxide gate insulator for the OxTFT parts and to form the via holes for the S/D contacts by O_2 plasma etching [Fig. 2(b)]. The next step was to prepare the oxide gate insulator and to pattern it into only channel region of OxTFT, in which 65 nm

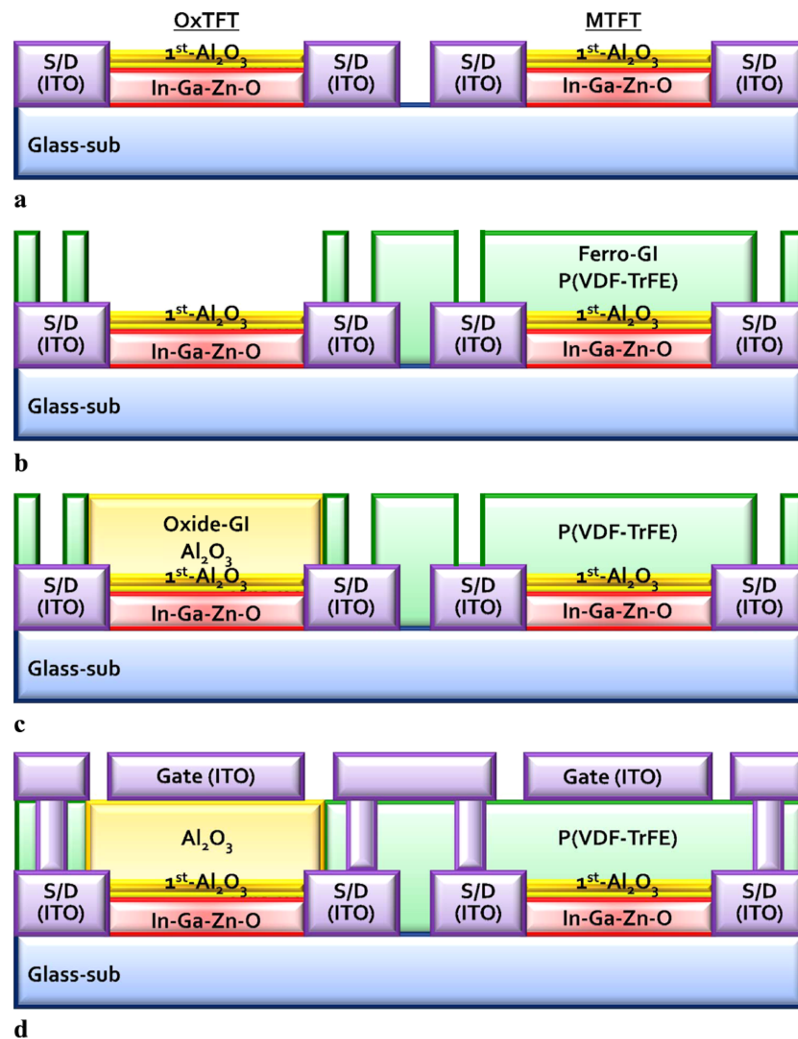

Fig. 2 Schematic diagrams of the fabrication procedures for the transparent memristor cell implemented on the glass substrate

ALD-grown Al_2O_3 was deposited at 150°C [Fig. 2(c)]. We have to remind that the process temperatures and deposition methods after defining the P(VDF-TrFE) layer should be carefully chosen, because the temperature of higher than 160°C and/or the plasma-induced process may deteriorate the physical and chemical properties of P(VDF-TrFE). The melting temperature of the P(VDF-TrFE) with a molar ratio of 70/30 was known as approximately 155°C [34]. Then, 150 nm thick ITO gate electrodes were deposited by using the sputtering system. The ITO deposition was so designed as to minimize the plausible physical damage by employing an off-axis geometry between the substrate and target in the sputtering system (manufactured by ULVAC). It was very difficult to clearly pattern the ITO on the P(VDF-TrFE) for the case of wet chemical etching owing to the poor adhesion of ITO on the P(VDF-TrFE). Furthermore, it was sometimes observed that the wet etchant permeated through the P(VDF-TrFE) and damaged the IGZO channel. From these reasons, the ITO gate patterns were formed by lift-off techniques in this proposed process flow [Fig. 2(d)]. Final thermal annealing at 150°C was performed in order to reduce the electrical resistance of ITO gates and to enhance the properties of IGZO channel. Because the temperature of overall process could be suppressed below 200°C, this procedure can be also compatible for the use of flexible plastic substrate. Figure 3(a) shows a photo-image of the transparent memristor cell fabricated on the glass substrate of the size 10 cm × 10 cm. The optical transmission spectra exhibited a high transmittance of approximately 86% at the wavelength of 550 nm, as shown in Fig. 3(b). Parts (c) and (d) of Fig. 3 show the microscopic photographs of the 2T-memristor cell region including each proving pad and its magnified view, respectively. As can be seen from the figure, the memristor cell was well patterned and fabricated without any physical damage.

4 Characterization and discussion

The fabricated devices and cell were characterized using a semiconductor parameter analyzer (Agilent B1500A) at

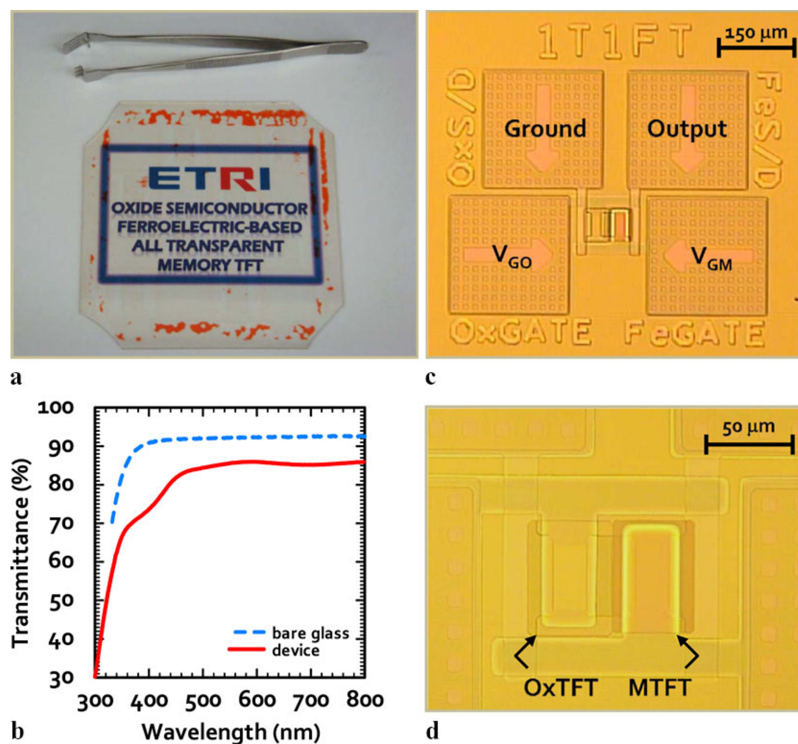

Fig. 3 (**a**) Photo-image of the fabricated transparent memristor cell. The size of glass substrate was 10×10 cm^2. (**b**) Optical transmittance spectra of the transparent memristor cell fabricated on the glass substrate. The transmittance of bare glass was also plotted in a *dotted line*. Microscopic photographs of the (**c**) 2T-type memristor cell region including the proving pads and (**d**) its magnified view

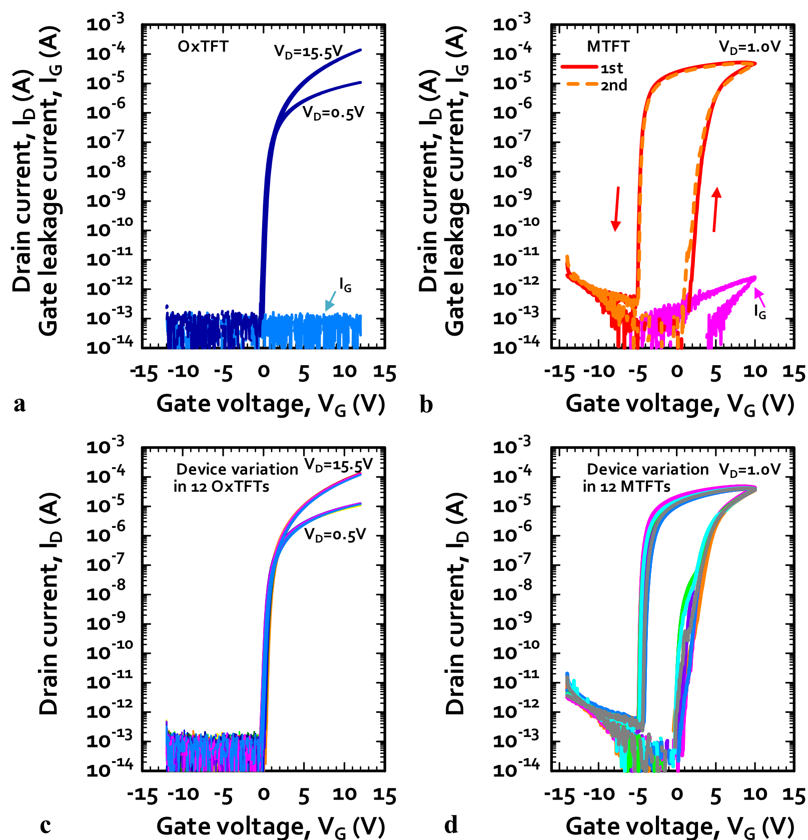

Fig. 4 I_D–V_G transfer characteristics and gate leakage currents of the fabricated (**a**) OxTFT and (**b**) ferroelectric MTFT. All measurements were performed in forward and reverse directions of V_G. For the OxTFT, the behaviors were repeatedly measured at two V_D of 0.5 and 15.5 V, and for the MTFT, they were repeated at the same V_D of 1.0 V. The gate width and length of both TFTs were 40 and 20 μm, respectively. Sets of transfer curves for (**c**) 12 OxTFTs and (**d**) 12 MTFTs at different positions identically spaced on the test vehicles with the size of 10×10 cm^2 were examined to verify the process uniformity

room temperature in a dark box. Parts (a) and (b) of Fig. 4 show the typical characteristics of drain current–gate voltage (I_D–V_G) transfer curves and gate leakage currents (I_G) for the fabricated OxTFT and the MTFT, respectively. All measurements were performed in a double sweep mode of V_G. The channel width (W) and length (L) of TFTs were 40 and

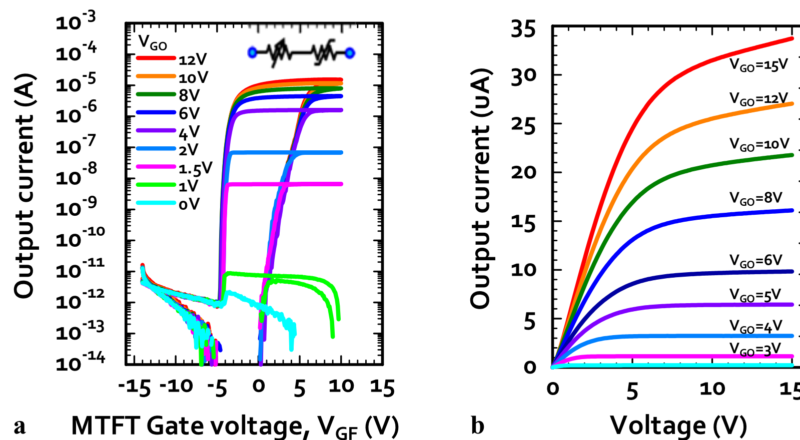

Fig. 5 (**a**) Variations in I_D–V_G transfer characteristics of the proposed memristor cell when the fixed bias condition of V_{GO} was varied from 0 to 12 V and V_{GM} was normally swept from −14 to 10 V. (**b**) Incremental modulation of output current by applying the various bias voltages of V_{GO} after programming the MTFT into the *on* state, for which the voltage pulse with 15 V and 990 ms was initially applied to the V_{GM}

20 µm, respectively. For the case of OxTFT, the field-effect mobility at the saturated regime (μ_{sat} at V_D of 15.5 V), subthreshold swing (SS), *on*/*off* I_D ratio, and I_G were obtained to be approximately 15.6 cm^2 V^{-1} s^{-1}, 180 mV/dec, 10^9, and 10^{-13} A, respectively. On the other hand, for the MTFT, those device parameters were obtained to be approximately 49.2 cm^2 V^{-1} s^{-1}, 340 mV/dec, 10^8, and 10^{-12} A, respectively. The field-effect mobility of the MTFT was calculated at the linear regime (μ_{lin} at V_D of 1.0 V) because the large I_D driven at the saturation region sometimes have some harmful effect on the electronic nature of the oxide active channel. The threshold voltages (V_{th})/turn-on voltages (V_{on}) for the OxTFTs and MTFTs were measured to be 2.4 V/−0.4 V and 3.1 V/1.6 V, respectively. The counterclockwise direction of hysteresis in I_D was clearly observed for the MTFT and the obtained memory window (MW) was approximately 7.5 V with a V_G sweep from −14 to 10 V. It was also confirmed for the MTFT that the transfer characteristics did not experience so much variation between the first and the second sweep in V_G. The obtained characteristics apparently reveal that the fabricated transparent individual OxTFT and MTFT exhibited excellent device behaviors. It can be found from these results that both TFTs composing the memristor cell were successfully integrated without any process damages even after the full fabrication processes. In verifying the feasibility of the proposed integration process, to guarantee the device uniformity is also very important for the memristor array configuration. Figure 4, (c) and (d), shows sets of transfer characteristics of twelve OxTFTs and twelve MTFTs, respectively, which were chosen from the identically spaced test devices located at different positions on the test vehicles of the size 10 × 10 cm^2. We could confirm that the variations among the devices were almost negligible for the OxTFT. For the MTFT, although some variations in V_{on} and MW were observed, the obtained characteristics among the devices were supposed to be sufficiently uniform.

Other characteristics such as switching time and retention behaviors for the programmed currents can be referred to our previously reported devices fabricated with the similar device structures [30, 32, 35]. The switching time of the P(VDF-TrFE)-based MTFT was typically observed to be longer than 100 ms. Furthermore, a slight reduction in programming voltage may markedly impede the switching event because the switching time is known to exponentially decay with $1/E$ [36], where E is the programming electric field applied across the P(VDF-TrFE) layer. The retention times for the MTFT were reported to be still in the range of two or three hours. Relatively long switching time and short retention time should be improved for the high-speed and reliable memristor operations.

Next, the electrical characterization for the transparent memristor cell was performed. As shown in Fig. 1(d), the V_{GO} and V_{GM} correspond to the drive and programming gates for the memristor cell, respectively. When the fixed bias condition of V_{GO} was varied from 0 to 12 V, the transfer characteristics of the memristor cell were continuously modulated without any changes in V_{on}, MW, and *off* current, as shown in Fig. 5(a). In this cell structure, the OxTFT serially connected to MTFT is expected to act as a resistor with variable channel resistance with the control of V_{GO}, as schematically shown in the inset of Fig. 5(a). Figure 5(b) shows the modulations in programmed output currents after the MTFT was initially programmed by applying the voltage pulse with 15 V and 990 ms to the V_{GM}. The saturated output current could be modulated in the range from 0.2 to 33.7 µA when the bias condition of V_{GO} was varied from 2 to 15 V and V_{GM} was fixed at 0 V. Although this result demonstrated well the working feasibility of the proposed transparent memristor cell, in order to suitably realize the nonvolatile multi-level memory states, initially programmed output currents with various resistance states of the MTFT should be accurately and reproducibly read out only by switching the OxTFT. As future works, if the reliable functions of multi-level memory states can be obtained for the memristor cell, they are expected to be very applicable for the analog-like synaptic weight and for the weighted-sum operation in the electrically modifiable synapse array [11, 26].

Strictly speaking, this memristor cell composed of two TFTs is not the flux-controlled device; to the contrary, the ferroelectric polarization of MTFT is always fully reversed for each programming event. The "storing" and"reading" operations can be separately performed so that more stable behaviors of intermediate memory states could be guaranteed. This cell structure provides a useful solution to select a designated cell within a crossbar memory array or synapse array configuration without any crosstalk problem. Complete *off* state can be also realized for this memristor cell by turning the OxTFT off, as shown in Fig. 5(a), which is very beneficial to save the power consumption at the standby status. Although this 2T-type cell structure may be undesirable to scale the cell size and to simplify the peripheral circuit, these issues are not so urgent for the large-area electronics featuring the flexibility and/or transparency unlike the Si-based electronics. The cell size can be additionally reduced by building the cell structure in a vertical direction with dual-gate configuration. We still have a feasibility that the PFM-type adaptive-learning operation can be also functionalized for the proposed transparent memristor cell, as demonstrated in Fig. 1. The improvement of retention behaviors, especially for the partially polarized intermediate memory states, is a very demanding factor.

5 Conclusion

A fully transparent memristor cell was proposed and demonstrated for the first time. This memristor cell was designed to be composed of one-memory TFT and one-switch TFT employing an oxide semiconductor thin film as an active channel layer. The gate insulator of the MTFT was chosen as a typical ferroelectric copolymer of P(VDF-TrFE) and the ferroelectric-based field-effect was the origin for the channel conductance modulation. The fabrication procedures were so carefully optimized as to obtain the excellent device characteristics even at low process temperature below 200°C. Good transistor behaviors and programmed output current modulations were successfully demonstrated for the transparent memristor cell. If the memory retention could be improved for the intermediately polarized memory states as future works, ultra-low power memristor cell having the PFM-type adaptive-learning function could be also provided. This prototype demonstration suggested that the proposed ferroelectric-based memristor cell can be expected to be very suitable for the nonvolatile memory array configuration and the future neuromorphic systems embedded in the intelligent transparent electronic applications.

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