Nonvolatile Charge-Trap Memory Transistors With Top-Gate Structure Using In–Ga–Zn-O Active Channel and ZnO Charge-Trap Layer

Jun Yong Bak, Min-Ki Ryu, Sang Hee Ko Park, Chi Sun Hwang, and Sung Min Yoon

***Abstract*— We proposed a charge-trap-type memory transistor with a top-gate structure composed of Al_2O_3 blocking/ZnO charge-trap/IGZO active/Al_2O_3 tunneling layer. The memory ON/OFF ratio higher than six-orders-of magnitude was obtained after the programming when the width and amplitude of program pulses were 100 ms and ±20 V, respectively. Excellent endurance was successfully confirmed under the repetitive programming with 10^4 cycles. The memory ON/OFF ratio higher than 10^3 was guaranteed even after the lapse of 10^4 s. Interestingly, the retention properties were affected by the bias conditions for read-out operations.**

***Index Terms*— In–Ga–Zn-O (IGZO), ZnO trap layer, oxide semiconductor, charge trap memory, top gate structure.**

I. INTRODUCTION

CHARGE-trap-type nonvolatile memory transistors (CTMs) have been widely researched thanks to their higher chip density, CMOS process compatibility, and multi-bit operations in conventional Si electronics [1], [2]. Another important paradigm in electronics is transparent and flexible system applications implemented on various substrates, in which nonvolatile memory devices are also essential components. Oxide-based CTM can be a promising candidate for this field owing to the transparency and low-temperature process compatibility of oxide semiconductor materials. According to previous works, for the realization of oxide CTM, the various charge-trap (CT) layers such as nanoparticles (Pt, Au, and Ag) [3], dielectrics (SiO_x, Si_3N_4, and Al_2O_3) [4], [5], and oxide semiconductors (In-Ga-Zn-O, ZnO) [6], [7] have been explored. However, there still remain technical issues of long program speed and short retention time, which can be improved by optimizing the gate-stack design including the employed materials and their thickness. The structure of an oxide CTM can be also an important concern to discuss for enhancing the device performance. The bottom-gate-structured thin film transistors (TFTs) have been mainly employed for the oxide CTMs, in which, however, the charge-trap, tunneling, and passivation layers that prevents adsorption and/or desorption of oxygen and/or water molecules in ambient should be individually prepared and patterned [6], [8]. In contrast, for the top-gate-structured TFTs, a CTM can be simply fabricated by one additional deposition for CT layer and one-step patterning process. The blocking layer can also be acted as a passivation layer. Consequently, in order to realize high-performance oxide CTMs, it is expected to be promising to employ the top-gate-structured gate-stacks by optimizing the material combinations and their process conditions such as film thickness. In this letter, we proposed a CTM device with a top-gate structure composed of all-oxide gate-stacks for the first time. Excellent nonvolatile memory characteristics and structural features of the proposed oxide CTMs were demonstrated.

Manuscript received January 6, 2014; accepted January 18, 2014. Date of publication January 29, 2014; date of current version February 20, 2014. This work was supported in part by the National Research Foundation of Korea through the Korean Government under Grant 2012011730 and in part by the Ministry of Science, ICT and Future Planning, Korea, in the ICT Research and Development Program 2013. The review of this letter was arranged by Editor M. Jurczak.

J. Y. Bak and S. M. Yoon are with the Department of Advanced Materials Engineering for Information and Electronics, Kyung-Hee University, Yongin 446-701, Korea (e-mail: sungmin@khu.ac.kr).

M.-K. Ryu, S. H. K. Park, and C. S. Hwang are with the Electronics and Telecommunications Research Institute, Daejeon 305-350, Korea.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2014.2301800

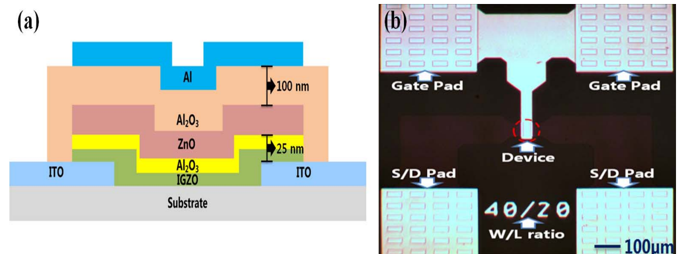

Fig. 1. (a) Schematic cross-sectional view and (b) top viewing microscopic image of the fabricated oxide CTM.

II. EXPERIMENT

The top-gate-bottom-contact CTM was fabricated on glass substrate, as shown in Fig. 1(a). A 150-nm In-Sn-O (ITO) deposited by dc sputtering method was patterned into source/drain (S/D) regions. The 20-nm IGZO channel layer was prepared by rf magnetron sputtering method. Then, 5-nm Al_2O_3 tunneling layer and 50-nm ZnO CT layer were successively deposited by atomic layer deposition (ALD). After the one-step patterning of triple layers of ZnO/Al_2O_3/IGZO, the 100-nm Al_2O_3 was formed by ALD as a blocking layer. The gate electrode was formed by the thermal evaporation of 100-nm Al. Finally, the fabricated devices were annealed at 200 °C in a vacuum for 2 h. Since the total thermal budget was controlled to be as low as 200 °C, which was much

0741-3106 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

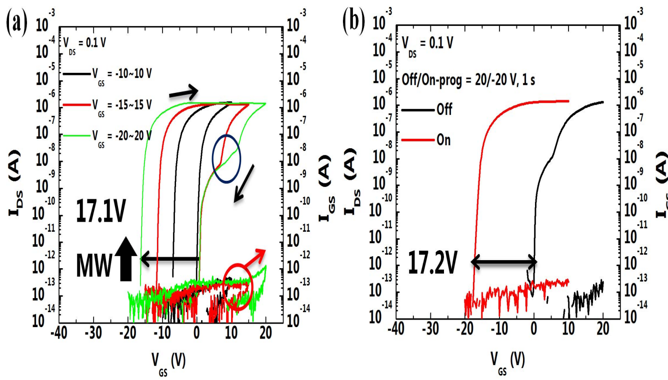

Fig. 2. I_{DS}–V_{GS} characteristics for the fabricated oxide CTM with (a) various V_{GS} sweep ranges of $-10\sim10$, $-15\sim15$, and $-20\sim20$ V and (b) with a single V_{GS} sweep after on and off programming events using the program pulse duration and amplitudes of 1 s and ±20 V, respectively.

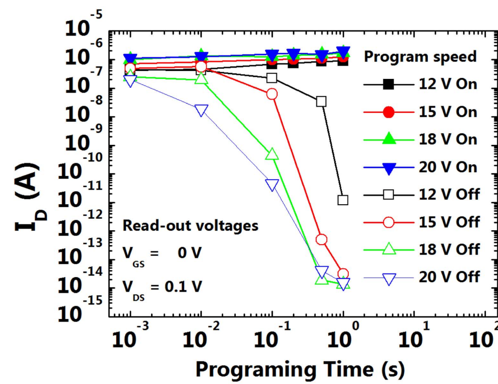

Fig. 3. Variations in the programmed I_{DS} of on and off states for the fabricated oxide CTM with varying the pulse duration of program voltage signal from 1 s to 1 ms. The program voltages for the memory on and off states were ±12, 15, 18 and 20 V.

lower than some previous reports [9], we surely expect that there was no marked interdiffusion after the post annealing process. Channel width and length of the evaluated devices were 40 and 20 μm, respectively, as shown in Fig. 1(b). The fabricated device was measured by the nonvolatile memory device evaluation system composed of a semiconductor parameter analyzer (Keithley 4200-SCS), a programmable pulse generator (HP 8110A), and a custom-made semi-automatic measuring software at room temperature in a dark box.

III. Results and Discussion

Fig. 2(a) shows the drain current (I_{DS})–gate voltage (V_{GS}) characteristics of the fabricated CTM device. The values of the field-effect saturation mobility (μ_{sat}) and the subthreshold swing (SS) were obtained to be approximately 0.2 cm^2 $V^{-1}s^{-1}$ and 0.35 V/decade, respectively. The hysteretic behaviors of I_{DS} originated from the nonvolatile memory characteristics when on- and off-programming were performed under the static V_{GS} sweep conditions. The shift in the turn-on voltage between the forward and reverse sweeps of V_{GS} was defined as a memory window (MW), with which the nonvolatile bistability could be exploited at a given read-out voltage. The widths of MW were obtained to be 6.9, 12.3 and 17.1 V when the sweep ranges of V_{GS} were varied from -10 to 10 V, from -15 to 15 V, and from -20 to 20 V, respectively. The shift in the turn-on voltage was also confirmed in single sweeps of V_{GS} after on and off programming using 1 s and ±20 V program pulses, respectively, as shown in Fig. 2(b), which guarantees the nonvolatile memory actions with bi-stabilities of programmed currents. These results suggest that the proposed oxide CTM exhibited clear memory operations supported by charge-trapping/detrapping behaviors, and that the amounts of trapped charges could be successfully controlled by changing the gate biases. It was also confirmed that the obtained memory characteristics of TFT were very stable during ten times continuous measurements, which was resulted from the optimized gate-stack structure without undesirable environmental effects. Anomalous shoulder observed in the transfer curve, as illustrated by blue circle, was supposed to be due to the surface degradation of ZnO CT layer during the patterning process via conventional photo-lithography using chemicals [10]. To solve this problem, improvements of device design and fabrication process are under progress.

In most practical memory applications, it would be important to examine the memory performances such as program speed, endurance, and data retention characteristics under the condition that dynamic pulse signals are applied to the CTM. Fig. 3 shows the variations in the programmed I_{DS} of fabricated oxide CTM when the pulse widths of program voltages applied for on and off programming were varied from 1 s to 1 ms at various voltage amplitudes of ± 12, 15, 18 and 20 V, respectively. It was found that the off-programmed I_{DS} and resulting memory on/off ratios were sensitively dependent on measurement conditions, Asymmetric switching behaviors can be explained as follows. Since the shallow states of n-type ZnO semiconductor would almost be occupied with electrons during the off-programming event, the carriers accumulated in the IGZO channel should be trapped into the deep levels of ZnO trap layer, and hence longer time for programming would be needed. On the contrary, for the case of on-programming, the electrons in the shallow level of ZnO can be quickly provided to the IGZO channel and the electrons trapped in deep levels are subsequently de-trapped [11]. While pulse width longer than 500 ms was required to obtain one-order-of magnitude on/off ratio at 12-V-programming, two-orders-of magnitude on/off ratio was confirmed with only 10-ms-width pulse at 20-V-programming. The maximum on/off ratio of eight-orders-of magnitude was obtained when the width and amplitude of program pulses were chosen as 1 s and 20 V, respectively. With the program voltage of -20 V, the off-programming was sufficiently initiated even at the pulse width of 1 ms. These obtained program speed for our proposed oxide CTM can be evaluated to be far better than those for the previously reported devices [12], [13].

To estimate program endurance characteristics, the widths and amplitudes of program pulses were fixed at 100 ms and ±20 V. The repeated programmed I_{DS}'s were measured at a V_{GS} of 0 V and a V_{DS} of 0.1 V during 10^4 cycling events, as shown in Fig. 4(a). The memory on/off ratio of the fabricated CTM was approximately 2.6 × 10^6. Consequently, it can be said that the program endurance for the proposed device was

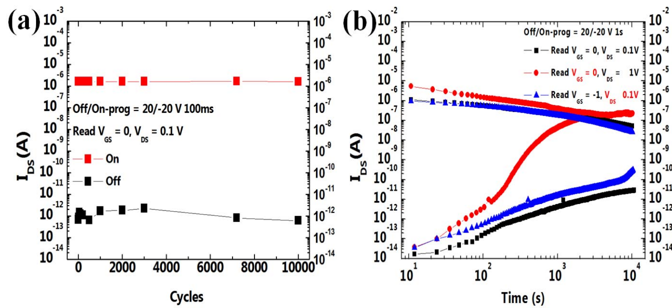

Fig. 4. (a) Variations in the programmed I_{DS} for the fabricated oxide CTM when the program voltage signals were repeatedly applied with 10,000 cycles. The amplitude and width of program pulses were fixed at ±20 V and 100 ms, respectively. (b) Variations in I_{DS}'s programmed with the lapse of retention time for 10,000 s. The amplitude and width of program pulses were fixed at ±20 V and 1 s, respectively. The read-out V_{GS} and the V_{DS} were varied to $V_{GS} = 0$ and $V_{DS} = 0.1$ V (indicated in black square), $V_{GS} = -1.0$ and $V_{DS} = 0.1$ V (indicated in blue triangle), and $V_{GS} = 0$V $V_{DS} = 1.0$ V (indicated in red circle), respectively.

quite excellent. The data retention characteristics were also investigated. The variations in the programmed I_{DS}'s were measured after the programming during the lapse of retention time for 10^4 s, as shown in Fig. 4(b), in which the program and read-out bias conditions were chosen as the same that those employed in the endurance test. The memory on/off ratio was retained to be 1.8×10^3 after 10^4 s. In addition, the SS value did not show any marked degradation during the retention and/or endurance tests. Because of wider band gap of Al_2O_3 (8.9 eV) compared with those of channel and CT layers [14], [15], the charge trapping/de-trapping processes via Fowler-Nordheim tunneling process as well as strong endurance and long term stability were successfully confirmed. To examine the relationship between structural features of proposed top-gate IGZO CTM and its memory properties, the retention characteristics were evaluated with two different bias conditions for read-out operations. (1) When the V_{DS} increased from 0.1 to 1.0 V at a fixed V_{GS} of 0 V, the resulting memory on/off ratio was severely degraded to be only 84 after 10^4 s. On the other hand, (2) when the V_{GS} was changed from 0 to -1.0 V at a fixed V_{DS} of 0.1 V, the memory on/off ratio were not markedly reduced with time evolution compared to the case when V_{GS} was 0 V. These remarkable differences between two bias conditions were supposed to originate from the device structure. While the gate electrode was designed to be 100 nm from the ZnO CT layer with intervening Al_2O_3 blocking layer, the drain electrode was located from the CT layer with only 25-nm-thick channel and tunneling layer, as indicated in arrow shown in Fig. 1(a). Owing to this feature, detrapping event at a higher bias condition of V_{DS} can occur in a more sensitive way to the case when the V_{GS} is deviated from the reference value. Therefore, it is very interesting to note that the bias conditions for read-out operations would have critical impact on the retention characteristics.

IV. Conclusion

An all-oxide-type nonvolatile memory transistors using charge-trap phenomenon was proposed and its memory behaviors were investigated. The top-gate-stack structure was optimized to be 100-nm Al_2O_3 blocking/50-nm ZnO charge-trap/20-nm IGZO active/5-nm Al_2O_3 tunneling layer. The width of MW for the fabricated CTM was as large as 17.1 V. When the program pulses with 100 ms width and 20 V amplitude of were applied, the memory on/off ratio as high as 10^6 was obtained and 10^4 times repetitive on/off programming was successfully confirmed. The memory margin higher than 10^3 was guaranteed even after the lapse of 10^4 s and the retention time was found to be sensitively influenced by the bias conditions for read-out operations. From these characteristics, it was concluded that the proposed all-oxide top-gate CTM exhibited excellent nonvolatile memory behaviors by carefully controlling the device structure and fabrication process.

References

[1] H.-B. Chen, Y.-C. Wu, L.-C. Chen, *et al.*, "High-reliability trigate poly-Si channel flash memory cell with Si-nanocrystal embedded charge-trapping layer," *IEEE Trans. Electron. Devices*, vol. 33, no. 4, pp. 537–539, Apr. 2012.

[2] Y.-C. King, T.-J. King, and C. Hu, "Charge-trap memory device fabricated by oxidation of Si_{1-x} Ge_x," *IEEE Trans. Electron. Devices*, vol. 48, no. 4, pp. 696–700, Apr. 2001.

[3] Y.-S. Park, S. Y. Lee, and J.-S. Lee, "Nanofloating gate memory devices based on controlled metallic nanoparticle-embedded InGaZnO TFTs," *IEEE Electron. Dev. Lett.*, vol. 31, no. 10, pp. 1134–1136, Oct. 2010.

[4] W.-T. Chen and H.-W. Zan, "High-performance light-erasable memory and real-time ultraviolet detector based on unannealed indium-gallium-zinc-oxide thin-film-transistor," *IEEE Electron. Devce Lett.*, vol. 33, no. 1, pp. 77–79, Jan. 2012.

[5] E. Kim, Y. Kim, D. H. Kim, *et al.*, "SiNx charge-trap nonvolatile memory based on ZnO thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 11, pp. 112115-1–112115-3, Sep. 2011.

[6] H. Yin, S. Kim, C. J. Kim, *et al.*, "Fully transparent nonvolatile memory employing amorphous oxides as charge trap and transistor's channel layer," *Appl. Phys. Lett.*, vol. 93, pp. 172109-1–172109-3, Oct. 2008.

[7] F. B. Oruç, F. Cimen, A. Rizk, *et al.*, "Thin-film ZnO charge-trapping memory cell grown in a single ALD step," *IEEE Electron. Device Lett.*, vol. 33, no. 12, pp. 1714–1716, Dec. 2012.

[8] J. Jang, J. C. Park, D. Kong, *et al.*, "Endurance characteristics of amorphous-InGaZnO transparent flash memory with gold nanocrystal storage layer," *Appl. Phys. Lett.*, vol. 58, no. 11, pp. 3940–3947, Nov. 2011.

[9] X. Lan, X. Ou, Y. Cao, *et al.*, "The effect of thermal treatment induced inter-diffusion at the interfaces on the charge trapping performance of HfO_2/Al_2O_3 nanolaminate-based memory devices," *J. Appl. Phys.*, vol. 114, pp. 044104-1–044104-7, Jul. 2013.

[10] S.-H. K. Park, D.-H. Cho, C.-S. Hwang, *et al.*, "Channel protection layer effect on the performance of oxide TFTs," *ETRI J.*, vol. 31, pp. 653–659, Dec. 2009.

[11] T. Kamiya and H. Hosono, "Electronic structures and device applications of transparent oxide semiconductors: What is the real merit of oxide semiconductors," *Int. J. Appl. Ceram. Technol.*, vol. 2, pp. 285–294, Aug. 2005.

[12] I.-S. Kang, Y.-S. Kim, H.-S. Seo, *et al.*, "High-performance and room-temperature-processed nanofloating gate memory devices based on top-gate transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 98, pp. 212102-1–212102-3, May 2011.

[13] B. Park, K. Cho, S. Kim, *et al.*, "Nano-floating gate memory devices composed of ZnO thin-film transistors on flexible plastics," *Nanosc. Res. Lett.*, vol. 6, p. 41, Sep. 2011.

[14] D. Yeom, J. Kang, M. Lee, *et al.*, "ZnO nanowire-based nano-floating gate memory with Pt nanocrystals embedded in Al_2O_3 gate oxides," *Nanotechnology*, vol. 19, p. 395204, Jul. 2008.

[15] S. Chen, X.-M. Cui, S.-J. Ding, *et al.*, "Novel Zn-doped Al_2O_3 charge storage medium for light-erasable In-Ga-Zn-O TFT memory," *IEEE Electron. Device Lett.*, vol. 34, no. 8, pp. 1008–1010, Aug. 2013.