Experimental Analysis on the Interaction Between Interface Trap Charges and Polarization on the Memory Window of Metal–Ferroelectric–Insulator–Si (MFIS) FeFET

Giuk Kim, *Graduate Student Member, IEEE*, Hyojun Choi, *Graduate Student Member, IEEE*, Sangho Lee, *Graduate Student Member, IEEE*, Hunbeom Shin, *Graduate Student Member, IEEE*, Sangmok Lee, Yunseok Nam, Hyunjun Kang, Seokjoong Shin, Hoon Kim, Youngjin Lim, Kang Kim, Il-Kwon Oh, Sang-Hee Ko Park, Jinho Ahn, and Sanghun Jeon, *Senior Member, IEEE*

***Abstract*— In this study, we investigated the impact of unstable and stable interface trap charges (Q_{it}) on P_S switching in metal–ferroelectric–insulator–Si (MFIS) ferroelectric field-effect transistors (FeFETs), which vary with the thickness of the insulator. We also examine how these variations ultimately affect the various performance metrics of MFIS FeFETs. To achieve this, we varied the thickness of the insulator (t_{IL}) in MFIS FeFETs to 1.5, 2.0, and 2.5 nm, thereby controlling the amount of Q_{it} injected from the channel into the ferroelectric (FE)/insulator interface. As t_{IL} decreases, the amount of Q_{it} increases, which amplifies the electric field across the FE layer. As a result, P_S switching enhances, and consequently, the MW characteristics of MFIS FeFETs improve. Furthermore, to analyze this in detail, we employed P_S–Q_{it} measurements on MFIS FeFETs to simultaneously extract unstable and stable Q_{it} as well as P_S and MW. The results show that as t_{IL} increases to 1.5, 2.0, and 2.5 nm, Q_{it} during program/erase (PGM/ERS) operations decreases to 100%, 61%, and 54%, respectively. This leads to a corresponding decrease in P_S to 100%, 59%, and 52%. Additionally, after sufficient delay following the PGM/ERS operations, we observe that the proportion stable Q_{it} compared to P_S is 91%, regardless to t_{IL} and the remaining 9% of P_S contributes to the MW property. Consequently, as t_{IL} increases to 1.5, 2.0, and 2.5 nm, the net charge decreases to 100%, 61%, and 54%, resulting in MW values of 1.85, 1.05, and 0.85 V, respectively. Finally, we analyzed the impact of Q_{it} generation as a function of t_{IL} on the variability and endurance characteristics of MFIS FeFETs.**

***Index Terms*— Ferroelectric field-effect transistor (FeFET), interface trap charges, memory window, polarization.**

I. Introduction

HAFNIA-BASED ferroelectric field effect transistors (FeFETs) have recently attracted significant interest as a promising nonvolatile memory (NVM) device for the next generation [1], [2], [3], [4]. This is due to their advantageous features, including compatibility with complementary metal–oxide–semiconductor (CMOS) technology, scalability, and nonvolatility [5], [6], [7]. In particular, FeFETs have become crucial components in neuromorphic computing and in-memory computing applications due to their exceptional reliability, high operational speed, and utilization of multilevel cell (MLC) technology [8], [9], [10]. In addition, FeFETs can be utilized in different configurations, including metal–ferroelectric–insulator–Si (MFIS) structure, metal–ferroelectric–metal–IL–Si (MFMIS) gate stacks with floating metal gate, and metal–IL–ferroelectric–IL–Si (MIFIS) structures that make use of both charge trapping and ferroelectric (FE) switching behavior [11], [12], [13]. The wide range of applications of FeFETs offers limitless possibilities for study.

Given that the MFIS gate-stack is the foundational structure of FeFETs, it is crucial to develop accurate models for different attributes in order to facilitate further study on a wide range of FeFETs [14], [15]. Considerable study has been focused on developing an analytical model of MW because of its critical role in the NVM device [16], [17],

Received 28 March 2024; revised 5 August 2024; accepted 6 August 2024. This work was supported in part by the Technology Innovation Program under Grant RS-2023-00231985 and Grant RS-2023-00235655 and in part by the National Research Foundation (NRF) grant funded by Korean Government [Ministry of Science and ICT (MSIT)] under Grant RS-2023-00260527. The review of this article was arranged by Editor J. Xu. *(Giuk Kim and Hyojun Choi contributed equally to this work.*) *(Corresponding authors: Jinho Ahn; Sanghun Jeon.)*

Giuk Kim, Hyojun Choi, Sangho Lee, Yunseok Nam, Hunbeom Shin, Sangmok Lee, Hyunjun Kang, Seokjoong Shin, Hoon Kim, and Sanghun Jeon are with the School of Electrical Engineering, and K. Kim, SHK. Park are with the School of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 34141, South Korea (e-mail: jeonsh@kaist.ac.kr).

Youngjin Lim and Il-Kwon Oh are with the Division of Electrical and Computer Engineering, Ajou University, Suwon 16499, South Korea.

Jinho Ahn is with the Division of Materials Science and Engineering, Hanyang University, Seoul 04763, South Korea (e-mail: jhahn@hanyang.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2024.3442163.

Digital Object Identifier 10.1109/TED.2024.3442163

[18]. Yoo et al. [19] presented a new explanation for MW behavior of MFIS FeFET using an analytical model. However, Lim et al. [20] introduced an alternative numerical model of MFIS FeFET, which is described in the following equation:

$$\mathrm{MW} = \left| V_{\mathrm{th,PGM}} - V_{\mathrm{th,ERS}} \right| = \left| \frac{2(P_{\mathrm{S}} - Q_{\mathrm{it}})}{C_{\mathrm{FE}}} \right| \quad (1)$$

where P_{S}, Q_{it}, and C_{FE} are the spontaneous polarization, interface trap charges, and capacitance of FE layer, respectively.

On the other hand, Ichihara et al. [21], [22] have stated that Q_{it} within the MFIS gate-stack can be divided into two distinct components: stable Q_{it} and unstable Q_{it}. These components refer to the interaction between the IL and the FE layer [23]. The stable Q_{it} is the component that is highly correlated with P_{S} (about 90% of P_{S}, as stated in [21]) and the maintenance of the MW after the detrap of the unstable Q_{it} attributed to the minor change of the net charge. However, the unstable Q_{it} has no significance to P_{S} and can be quickly released from its trapped state after the program/erase (PGM/ERS) operation. It is widely accepted that the presence of Q_{it} degrades the MW of FeFETs. However, Q_{it} can instead play a positive role in enhancing P_{S} switching by increasing the electric field across the FE layer [24], [25], [26], [27], [28], [29], [30], [31]. Specifically, a sufficient amount of Q_{it} (electrons) injected during the program (PGM) operation can stabilize P_{S} switching, leading to an expansion of the MW in MFIS FeFETs. Furthermore, Shin et al. [32], [33] have demonstrated that electrons located at the FE/IL interface during the PGM operation contribute to the improvement of MW in MFIS FeFETs, though they also introduce issues, such as variability, using low-frequency noise spectroscopy.

In this study, we experimentally analyze the relationship between Q_{it} and P_{S} during and after the PGM/ERS operations of MFIS FeFETs. We fabricated MFIS FeFETs with t_{IL} of 1.5, 2.0, and 2.5 nm, which allowed us to alter the amount of Q_{it} trapped at the interface between the IL and FE layer during the operation. Subsequently, we conducted a detailed comparison of the P_{S} switching and MW characteristics based on the Q_{it} values for each FeFET. To achieve this, we employed P_{S}–Q_{it} measurements that can simultaneously extract stable and unstable Q_{it}, P_{S}, and MW properties specific time after the PGM/ERS operations of MFIS FeFETs. Based on these findings, we analyzed not only the MW but also the variability and endurance characteristics of MFIS FeFETs in relation to the interaction between Q_{it} and P_{S}. Meanwhile, it should be noted that bulk traps within the IL and FE layers also impact the performance of MFIS FeFETs [32], [33]. However, the P_{S}–Q_{it} measurement technique is specialized for directly obtaining and comparing Q_{it}, P_{S}, and MW. Therefore, this study focuses on the impact of the interaction between P_{S} and Q_{it} on the performance of MFIS FeFETs, rather than bulk traps.

The experimental results show that, when subjected to the same electric field, the FeFET with a 1.5-nm-thick IL has a higher Q_{it} compared to the FeFETs with 2.0- and 2.5-nm-thick ILs on PGM/ERS, with reductions of 61% and 54%, respectively. As a result, this causes a reduction in P_{S} switching to 59% and 52%, respectively. The rise in the quantity of Q_{it} generated during PGM/ERS is directly proportional to the decrease in the thickness of the IL. At the same time, the electric field applied to the FE layer spontaneously increases, leading to an improvement in P_{S} switching. After a sufficient amount of time has passed since the PGM/ERS procedure, the very easily released and unstable Q_{it} fades, but the stable Q_{it} persists, accounting for 91% of the P_{S} compensation. Furthermore, the remaining 9% of P_{S}, in other words, the net charge, influences the MW of MFIS FeFET. Remarkably, the proportion of the uncompensated P_{S} remains consistent regardless oft_{IL} of the MFIS FeFETs. As a result, MFIS FeFETs with a relatively thin t_{IL} of 1.5 nm demonstrate easy Q_{it} injection, yielding a significant net charge and a wide MW of 1.85 V. In contrast, MFIS FeFETs with a thick t_{IL} of 2.5 nm encounter difficulties in Q_{it} injection, resulting in a reduced net charge and a narrow MW of 0.85 V.

Typically, in MFIS FeFETs, unstable Q_{it} detraps immediately after PGM/ERS operations, while stable Q_{it} compensates for approximately 90% of P_{S}, with the remaining 10% of P_{S} contributing to the MW [21], [22], [23]. To maintain a high uncompensated 10% P_{S} value even after a sufficient delay following PGM/ERS operations, excellent P_{S} switching characteristics are essential, enabling the achievement of a wide MW in MFIS FeFETs. Consequently, as t_{IL} decreases, Q_{it} injection becomes more active, improving P_{S} switching and thereby enhancing the MW characteristics of MFIS FeFETs. However, increased Q_{it} injection exacerbates variability characteristics. Furthermore, as t_{IL} increases, the voltage distributed across the insulator during PGM/ERS operations increases, leading to the degradation of endurance characteristics. We emphasize that our experimental findings validate the impact of the interaction between Q_{it} and P_{S} on the performance of MFIS FeFETs. Additionally, our results establish a foundation for future research on FeFETs.

II. Experimental Detail

The detailed fabrication procedures of MFIS FeFET device are described as follows. The 1.5-, 2.0-, and 2.5-nm-thick SiO_2 is formed on the p-type Si wafer by rapid thermal oxidation (RTO) under 700 °C, 800 °C, and 900 °C, respectively, after diluted HF dipping and SPM cleaning. Then, rapid thermal annealing (RTA) process was performed at 1000 °C under N_2 atmosphere to enhance the Ch. IL quality. The thickness of each device is carefully measured by spectroscopic ellipsometer. Subsequently, the Zr-doped HfO_2 ($Hf_{0.5}Zr_{0.5}O_2$) film of 18 nm is formed via plasma-enhanced atomic layer deposition (PEALD) at 320 °C chamber temperature. The precursors used in this step are TEMA-Hf and TEMA-Zr. Lastly, the 50-nm-thick TiN gate metal was formed, and subsequently, the RTA at 600 °C in N_2 ambient was carried out for the crystallization of FE layer. Keithley-4200A pulse generator and Keysight CX-3324A current analyzer are employed for the electrical analysis.

Fig. 1(a) presents the gate-stack of each device with the key fabrication processes. The MW of each device was assessed under various gate voltage with pulsewidths of 100 μs, as shown in Fig. 1(b). The maximum MW of each MFIS

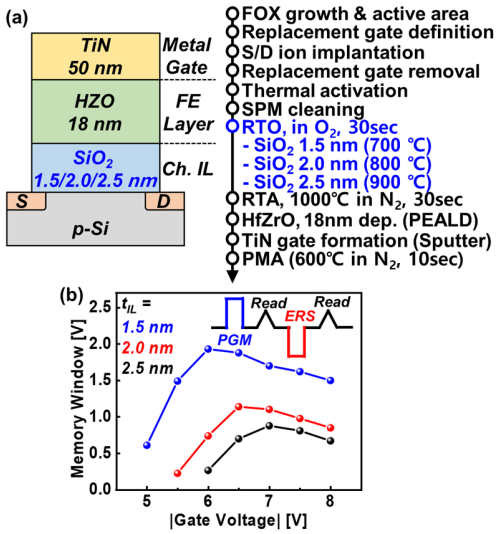

Fig. 1. (a) Schematic of the fabricated device with fabrication process. (b) Measured MW of device with Ch. IL of SiO_2 1.5, 2, and 2.5 nm for various applied gate voltages.

FeFET device with 1.5-, 2.0-, and 2.5-nm-thick IL was attained at gate voltages of 6.0, 6.5, and 7.0 V, respectively. The further electrical measurements and analyses conducted in this study were conducted under the aforementioned gate voltage conditions.

III. Results and Discussion

The pulse scheme of P_S–Q_{it} measurement is illustrated in Fig. 2, and the detailed process for deriving Q_{it}, P_S, and MW is described elsewhere [21]. Fig. 3(a)–(c) presents the MW, ΔP, and ΔQ_{it} data of FeFETs with t_{IL} of 1.5, 2.0, and 2.5 nm, respectively, as a function of delay time. These data were extracted through P_S–Q_{it} measurements. As t_{IL} decreases, the amount of ΔQ_{it} formed between the FE and the IL during the PGM operation increases, and a significant amount of Q_{it} can amplify E_{FE}. This large E_{FE} contributes to an improvement in P_S switching behavior. As a result, right after the PGM operation, ΔP increases as t_{IL} decreases. Subsequently, during the delay time, unstable Q_{it} is detrapped, resulting in a decrease in ΔQ_{it}. As a result, the net charge, derived by subtracting ΔQ_{it} from ΔP, gradually increases, ultimately leading to the emergence of MW. Following a sufficient delay time of 10^3 s, the comparison of MW characteristics among MFIS FeFETs reveals that MW increases as t_{IL} decreases, as presented in Fig. 3(a)–(c).

In our devices, the saturated MW was observed after 10^3 s, which is known as read-after-write delay (RAWD). However, this study focuses on elucidating the impact of the interaction between Q_{it} and P_S on the performances of the FeFETs. Although our research does not propose a direct solution to the RAWD problem, such challenges can be mitigated by adopting a unique operational scheme involving detrap pulses [22].

Interestingly, as shown in Fig. 4(a), after a sufficient delay time, approximately 90% of ΔP is compensated by ΔQ_{it} and the remaining ΔP contributes to MW. Specifically, unstable Q_{it}, which does not compensates P_S, is detrapped, leaving

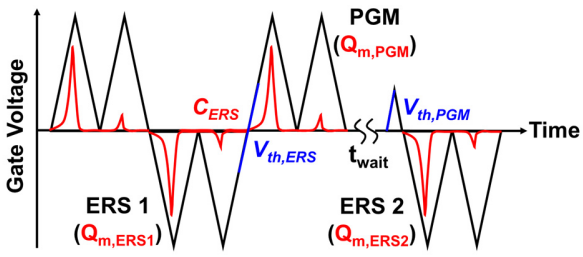

Fig. 2. Measurement pulse scheme (black) with the gate current (red) responding to the applied biasing voltage for P_S–Q_{it} separation.

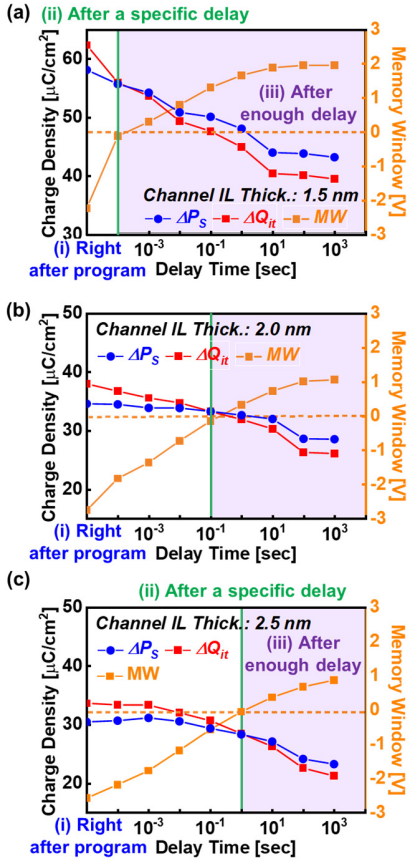

Fig. 3. Calculated ΔP_S, ΔQ_{it}, and MW of devices with IL of SiO_2 (a) 1.5, (b) 2.0, and (c) 2.5 nm with respect to the delay time after PGM operation.

stable Q_{it} coupled with P_S at the interface. Fig. 4(b) presents the net charge density values along with the corresponding MW properties with respect to t_{IL} in MFIS FeFETs after 10^3 s following PGM. In our devices, about 9% of ΔP is consistently observed as the net charge density, but as t_{IL} decreases, the value of ΔP increases, thereby increasing both the net charge density and MW.

The diagrams in Fig. 5 illustrate the three stages of interaction between Q_{it} and P_S, as well as the formation of MW, during the PGM operation of MFIS FeFETs with t_{IL} values of 1.5 and 2.5 nm, respectively. Fig. 3(a) and (c) provides a description for each stage. Immediately following program operation (i), the generation of $-Q_{it}$ becomes active within the MFIS gate structure with a 1.5-nm IL. This leads to

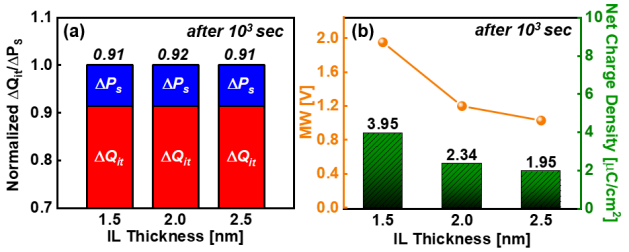

Fig. 4. (a) Normalized value of ΔQ_{it} compared to P_S of each devices. (b) Net charge induced on FE/IL interface and the MW characteristics with respect to the IL thickness.

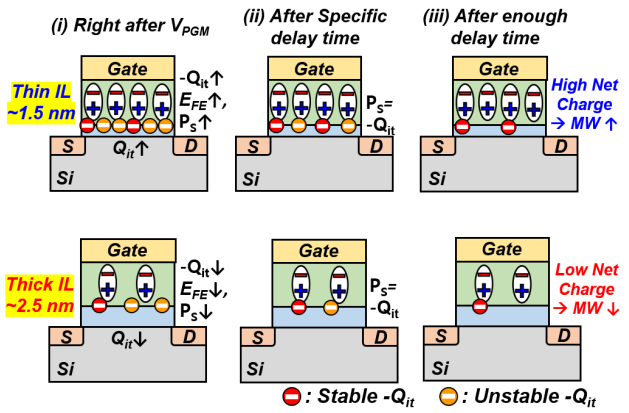

Fig. 5. Schematic of the dynamic alteration of P_S and Q_{it} for the MFIS FeFET after the PGM operation for IL thickness of 1.5 and 2.5 nm.

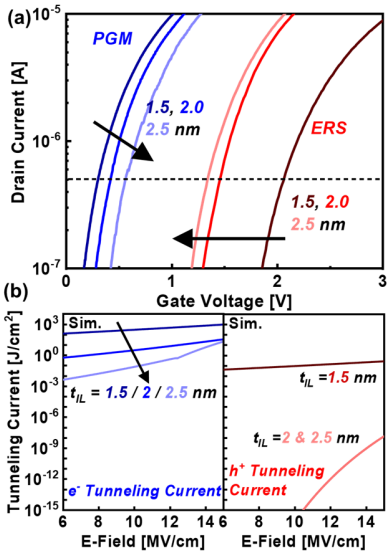

Fig. 6. (a) Transfer curve of each device after the PGM and ERS operation. (b) FN tunneling simulation with the modification for direct tunneling of the SiO_2 thickness of 1.5, 2.0, and 2.5 nm.

an amplified electric field across the FE layer, hence improving P_S switching. In contrast, when considering a FeFET with an IL thickness of 2.5 nm, neither the emergence of $-Q_{it}$ nor the switching of P_S is active. Following a designated period of time (ii), every MFIS FeFET demonstrates an MW value that is higher than 0. During this stage, the unstable $-Q_{it}$ gradually becomes annihilated, resulting in a reduction in the overall Q_{it}. As a result, the net charge density changes from negative to positive when the entire Q_{it} is subtracted from P_S. Significantly, as the thickness of the IL increases, the necessary delay time for MW also increases. This indicates that the increase in t_{IL} not only impedes the injection of Q_{it} but also hampers its detrapping. Eventually, following a sufficient period of delay (iii), the unstable $-Q_{it}$ is entirely eliminated, resulting in the presence of just the stable $-Q_{it}$ combined with P_S. As t_{IL} decreases, the high P_S switching results in a significant net charge density, equivalent to 9% of P_S, allowing for the attainment of a broad MW range.

As t_{IL} increases from 1.5 to 2 nm, an abrupt decrease in the MW is observed, as depicted in Fig. 4(b). This is ascribed to a reduction in Q_{it} during the PGM/ERS operation. It is important to note that the amount of electrons injected from the channel during the PGM operation is significantly higher than the amount of holes injected during the erase (ERS) operation [24], [25], [26], [27], [28], [29], [30], [31]. Fig. 6(a) depicts the measured transfer curve of each device following the PGM/ERS operation. It is worth mentioning that, during PGM operation, V_{th} consistently changes in relation to the rise in t_{IL}. However, an apparent decrease in V_{th} is notably observed for the device with a t_{IL} of 2 nm during the ERS operation. The decrease in V_{th} during the ERS operation leads to a significant deterioration in MW. Fig. 6(b) depicts the calculated tunneling current density for SiO_2 IL with thicknesses of 1.5, 2.0, and 2.5 nm. The calculation is based on the Fowler–Nordheim tunneling theory, including the adjustment for direct tunneling [34], [35], [36]. It should be noted that the current density due to tunneling is probably larger, since the effects of trap-assisted tunneling are not taken into account in this specific calculation [37]. The tunneling current density for holes is smaller than that of electrons due to a difference in conduction band and valence band offset [38], [39], [40]. Notably, there is a significant decrease in the density of hole tunneling current when the SiO_2 thickness is 2 nm, whereas the reduction in electron tunneling current density is proportionate across all thicknesses. Since the carrier injected during the ERS operation is a hole, the injected Q_{it} during the ERS process is greatly reduced. This results in P_S being uncompensated and causing low P_S switching behavior in the FE layer. As a result, this leads to a low V_{th}, which in turn causes the width of the MW to be narrow.

To investigate the impact of the interplay between Q_{it} and P_S on the variability of FeFETs, we extracted the V_{th} variability from 25 individual FeFET devices, as shown in Fig. 7(a)–(c). Interestingly, the V_{th} variability increased as t_{IL} decreased, and it was greater in the PGM state compared to the ERS state. This phenomenon is closely related to Q_{it}. As t_{IL} decreases, Q_{it} formation becomes active, leading to an increase in MW. However, variation in Q_{it} formation within each device can contribute to overall device variability [31], [32]. Additionally, as shown in Fig. 6, the amount of electrons injected from the channel during PGM is greater than the amount of holes injected during ERS, exacerbating the V_{th} variation. These results demonstrate that while active Q_{it} formation enhances P_S switching and MW, there is a tradeoff with device variability.

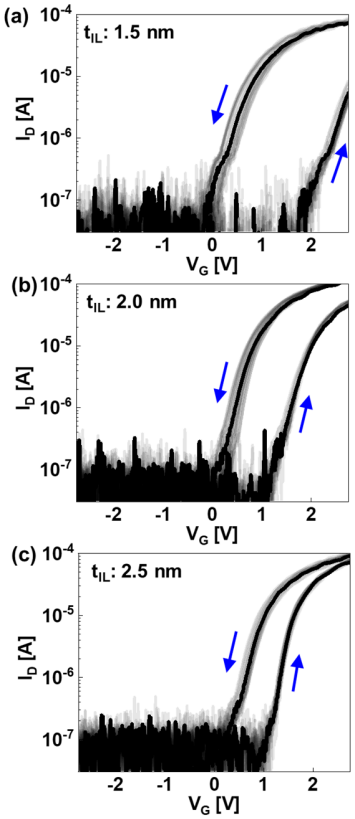

Fig. 7. Measured pulse *I*–*V* data and variability of MFIS FeFETs (25 devices) with IL thicknesses of (a) 1.5, (b) 2.0, and (c) 2.5 nm.

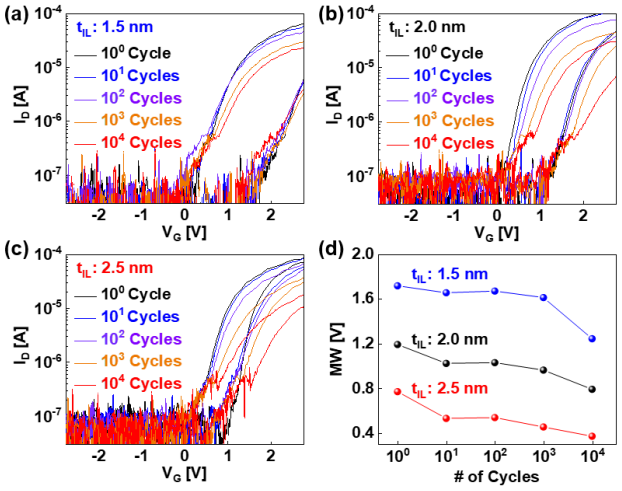

Fig. 8. Measured endurance data of MFIS FeFETs with IL thicknesses of (a) 1.5, (b) 2.0, and (c) 2.5 nm and (d) summarized MW characteristics with respect to the number of cycles.

Finally, we analyzed the impact of the interaction between Q_{it} and P_S on the endurance characteristics of FeFETs as shown in Fig. 8(a)–(d). This is because a thicker t_{IL} results in reduced capacitance of the IL (C_{IL}), leading to an increased electric field across the IL during PGM/ERS operations. The greater the wear of the IL during PGM/ERS, the more pronounced the degradation of the subthreshold swing and endurance becomes as the number of cycles increases. Consequently, in terms of the endurance characteristics, it is desirable to minimize the IL thickness in MFIS FeFETs.

IV. Conclusion

This study demonstrates how both unstable and stable Q_{it} affect P_S in an MFIS gate-stack, impacting the MW, variability, and endurance characteristics. To this end, we adjusted t_{IL} in MFIS FeFETs to 1.5, 2.0, and 2.5 nm, thereby controlling Q_{it} injected from the channel. Using the P_S–Q_{it} measurement technique, we thoroughly analyzed the generation of Q_{it} and its effects on P_S as a function of t_{IL}. According to the results, as t_{IL} increases, Q_{it} is not actively generated, leading to a decrease in the MW of MFIS FeFETs and an increase in the detrap time of trapped Q_{it}, exacerbating the RAWD issue. Additionally, as t_{IL} increases, the voltage distributed across the insulator at the gate voltage increases, degrading the endurance characteristics. However, a thinner t_{IL} increases the amount of Q_{it}, which enhances the variability of the FeFET device. Finally, we believe that our significant experimental findings establish a foundation for future research on adaptable hafnia FE memory devices.

References

[1] M. Jung, V. Gaddam, and S. Jeon, "A review on morphotropic phase boundary in fluorite-structure Hafnia towards DRAM technology," *Nano Converg.*, vol. 9, no. 1, p. 44, Oct. 2022, doi: 10.1186/s40580-022-00333-7.

[2] M. Kobayashi, J. Wu, Y. Sawabe, S. Takuya, and T. Hiramoto, "Mesoscopic-scale grain formation in HfO_2-based ferroelectric thin films and its impact on electrical characteristics," *Nano Converg.*, vol. 9, no. 1, p. 50, Nov. 2022, doi: 10.1186/s40580-022-00342-6.

[3] A. H.-T. Nguyen et al., "Impact of Pt grain size on ferroelectric properties of zirconium hafnium oxide by chemical solution deposition," *Nano Converg.*, vol. 9, no. 1, p. 45, Oct. 2022, doi: 10.1186/s40580-022-00334-6.

[4] J. Hwang, Y. Goh, and S. Jeon, "Physics, structures, and applications of fluorite-structured ferroelectric tunnel junctions," *Small*, vol. 20, no. 9, Mar. 2024, Art. no. 2305271, doi: 10.1002/smll.202305271.

[5] S. Dunkel et al., "A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond," in *IEDM Tech. Dig.*, Dec. 2017, p. 19, doi: 10.1109/IEDM.2017.8268425.

[6] S. Kubicek et al., "Low V_T CMOS using doped Hf-based oxides, TaC-based metals and laser-only anneal," in *IEDM Tech. Dig.*, vol. 89, Dec. 2007, pp. 49–52, doi: 10.1109/IEDM.2007.4418860.

[7] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 24.5.1–24.5.4, doi: 10.1109/IEDM.2011.6131606.

[8] T. Kim et al., "The opportunity of negative capacitance behavior in flash memory for high-density and energy-efficient in-memory computing applications," *Adv. Funct. Mater.*, vol. 33, no. 7, Feb. 2023, Art. no. 2208525, doi: 10.1002/adfm.202208525.

[9] F. Müller et al., "Multilevel operation of ferroelectric FET memory arrays considering current percolation paths impacting switching behavior," *IEEE Electron Device Lett.*, vol. 44, no. 5, pp. 757–760, May 2023, doi: 10.1109/LED.2023.3256583.

[10] H. Mulaosmanovic et al., "Novel ferroelectric FET based synapse for neuromorphic systems," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T176–T177, doi: 10.23919/VLSIT.2017.7998165.

[11] S. Lee, G. Kim, T. Kim, T. Eom, and S. Jeon, "Vertical-pillar ferroelectric field-effect-transistor memory," *Phys. Status Solidi (RRL) Rapid Res. Lett.*, vol. 16, no. 10, Oct. 2022, Art. no. 2100532, doi: 10.1002/pssr.202100532.

[12] S. Yoon et al., "QLC programmable 3D ferroelectric NAND flash memory by memory window expansion using cell stack engineering," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2023, pp. 1–2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185294.

[13] G. Kim et al., "In-depth analysis of the Hafnia ferroelectrics as a key enabler for low voltage & QLC 3D VNAND beyond 1K layers: Experimental demonstration and modeling," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2024, pp. 1–2.

[14] J. D. Anderson, J. Merkel, D. Macmahon, and S. K. Kurinec, "Evaluation of Si: HfO_2 ferroelectric properties in MFM and MFIS structures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 525–534, 2018, doi: 10.1109/JEDS.2018.2826978.

[15] B. Zhang, P. Hong, J. Hou, Z. Huo, and T. Ye, "Doped HfO_2-based ferroelectric-aided charge-trapping effect in MFIS gate stack of FeFET," *J. Appl. Phys.*, vol. 133, no. 16, pp. 4103.1–4103.8, 2023, doi: 10.1063/5.0141082.

[16] G. Kim et al., "High performance ferroelectric field-effect transistors for large memory-window, high-reliability, high-speed 3D vertical NAND flash memory," *J. Mater. Chem. C*, vol. 10, no. 26, pp. 9802–9812, Jul. 2022, doi: 10.1039/D2TC01608G.

[17] G. Kim et al., "Power-delay area-efficient processing-in-memory based on nanocrystalline Hafnia ferroelectric field-effect transistors," *ACS Appl. Mater. Interface*, vol. 15, no. 1, pp. 1463–1474, Jan. 2023, doi: 10.1021/acsami.2c14867.

[18] M. Saitoh et al., "HfO_2-based FeFET and FTJ for ferroelectric-memory centric 3D LSI towards low-power and high-density storage and AI applications," in *IEDM Tech. Dig.*, Dec. 2020, pp. 18.1.1–18.1.4, doi: 10.1109/IEDM13553.2020.9372106.

[19] S. Yoo et al., "An analytical interpretation of the memory window in ferroelectric field-effect transistors," *Appl. Phys. Lett.*, vol. 123, no. 22, pp. 2902.1–2902.7, 2023, doi: 10.1063/5.0168515.

[20] S. Lim et al., "Comprehensive design guidelines of gate stack for QLC and highly reliable ferroelectric VNAND," in *IEDM Tech. Dig.*, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413820.

[21] R. Ichihara et al., "Re-examination of V_{th} window and reliability in HfO_2 FeFET based on the direct extraction of spontaneous polarization and trap charge during memory operation," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265055.

[22] R. Ichihara et al., "Accurate picture of cycling degradation in HfO_2-FeFET based on charge trapping dynamics revealed by fast charge centroid analysis," in *IEDM Tech. Dig.*, Dec. 2021, pp. 6.3.1–6.3.4, doi: 10.1109/IEDM19574.2021.9720516.

[23] Z. Wang et al., "Depolarization field induced instability of polarization states in HfO_2 based ferroelectric FET," in *IEDM Tech. Dig.*, Dec. 2020, pp. 4.5.1–4.5.4, doi: 10.1109/IEDM13553.2020.9372098.

[24] M. Si et al., "Ferroelectric polarization switching of hafnium zirconium oxide in a ferroelectric/dielectric stack," *J. Electron. Mater.*, vol. 1, no. 5, pp. 745–751, 2019, doi: 10.1021/acsaelm.9b00092.

[25] K. Toprasertpong, M. Takenaka, and S. Takagi, "Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and Hall techniques: Revealing FeFET operation," in *IEDM Tech. Dig.*, Dec. 2019, p. 23, doi: 10.1109/IEDM19573.2019.8993664.

[26] K. Toprasertpong, Z. Y. Lin, T. E. Lee, M. Takenaka, and S. Takagi, "Asymmetric polarization response of electrons and holes in Si FeFETs: Demonstration of absolute polarization hysteresis loop and inversion hole density over 2×1013 cm^{-2}," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265015.

[27] K. Lee, S. Kim, M. Kim, J.-H. Lee, D. Kwon, and B.-G. Park, "Comprehensive TCAD-based validation of interface trap-assisted ferroelectric polarization in ferroelectric-gate field-effect transistor memory," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1048–1053, Mar. 2022, doi: 10.1109/TED.2022.3144965.

[28] S. Kuk, S. Han, B. H. Kim, S. Baek, J. Han, and S. Kim, "An investigation of HZO-based n/p-FeFET operation mechanism and improved device performance by the electron detrapping mode," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2080–2087, Apr. 2022, doi: 10.1109/TED.2022.3154687.

[29] K. Toprasertpong, M. Takenaka, and S. Takagi, "On the strong coupling of polarization and charge trapping in HfO_2/Si-based ferroelectric field-effect transistors: Overview of device operation and reliability," *Appl. Phys. A, Solids Surf.*, vol. 128, no. 12, p. 1114, Dec. 2022, doi: 10.1007/s00339-022-06212-6.

[30] D. Kleimaier et al., "Demonstration of a p-type ferroelectric FET with immediate read-after-write capability," *IEEE Electron Device Lett.*, vol. 42, no. 12, pp. 1774–1777, Dec. 2021, doi: 10.1109/LED.2021.3118645.

[31] N. Tasneem, Z. Wang, H. Chen, S. Yu, W. Chern, and A. Khan, "Immediate read-after-write capability in p-type ferroelectric field-effect transistors and its evolution with fatigue cycling," *IEEE Trans. Device Mater. Rel.*, vol. 23, no. 1, pp. 142–146, Mar. 2023, doi: 10.1109/TDMR.2023.3240319.

[32] W. Shin et al., "Effects of high-pressure annealing on the low-frequency noise characteristics in ferroelectric FET," *IEEE Electron Device Lett.*, vol. 43, no. 1, pp. 13–16, Jan. 2022, doi: 10.1109/LED.2021.3127175.

[33] W. Shin et al., "Variability analysis of ferroelectric FETs in program operation using low-frequency noise spectroscopy," *Appl. Phys. Lett.*, vol. 121, no. 16, pp. 3501.1–3501.4, 2022, doi: 10.1063/5.0111309.

[34] H. Bachhofer, H. Reisinger, E. Bertagnolli, and H. von Philipsborn, "Transient conduction in multidielectric silicon-oxide-nitride-oxide semiconductor structures," *J. Appl. Phys.*, vol. 89, no. 5, pp. 2791–2800, Mar. 2001, doi: 10.1063/1.1343892.

[35] A. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultra-thin gate dielectrics," *J. Appl. Phys.*, vol. 81, no. 12, pp. 7900–7908, Jun. 1997, doi: 10.1063/1.365364.

[36] R. Clerc, P. O'Sullivan, K. G. McCarthy, G. Ghibaudo, G. Pananakakis, and A. Mathewson, "A physical compact model for direct tunneling from NMOS inversion layers," *Solid-State Electron.*, vol. 45, no. 10, pp. 1705–1716, Oct. 2001, doi: 10.1016/s0038-1101(01)00220-9.

[37] H.-T. Lue et al., "Modeling of barrier-engineered charge-trapping NAND flash devices," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 2, pp. 222–232, Jun. 2010, doi: 10.1109/TDMR.2010.2041665.

[38] J. R. Schrieffer, "Theory of electron tunneling," *Rev. Modern Phys.*, vol. 36, no. 1, pp. 200–204, Jan. 1964, doi: 10.1103/revmodphys.36.200.

[39] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366–1373, Jul. 2001, doi: 10.1109/16.930653.

[40] R. Guo et al., "Interface-engineered electron and hole tunneling," *Sci. Adv.*, vol. 7, no. 13, 2021, Art. no. eabf1033, doi: 10.1126/sciadv.abf103.