Low-Temperature Processed Flexible In–Ga–Zn–O Thin-Film Transistors Exhibiting High Electrical Performance

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***Abstract*—In–Ga–Zn–O thin-film transistors processed at 150 °C on laminated polyethylene naphthalate substrates exhibiting high electrical performances such as a saturation mobility of 24.26 $cm^2/(V \cdot s)$, a subthreshold slope of 140 mV/dec, a turn-on voltage V_{on} of −0.41 V, and an on–off ratio of 1.8×10^9 were fabricated. Cool-off-type adhesive was adopted to easily detach the plastic substrate from the carrier holder. Devices also showed highly uniform characteristics with a variation of 0.09 V in turn-on voltage. Stability characteristics under the positive gate bias stress can be enhanced by increasing the annealing time at 150 °C.**

***Index Terms*—Oxide, sputtering, thin-film transistor (TFT), transparent.**

I. Introduction

FLEXIBLE devices based on plastic substrate are expected to find variety of future applications because of their rugged, lightweight, and bendable characteristics [1]. There are some reports on the flexible display with various substrate types and thin-film transistors (TFTs). To realize flexible displays, some of key features such as the choice of plastic substrate, the glasslike process, and the good electrical performance have to be guaranteed [2]. The first requirement is that the good electrical performance and stability characteristics in the TFTs must be needed under the low-temperature process. Since amorphous silicon TFTs (a-Si:H) exhibited low mobility and instability characteristics under the gate bias stress, it is difficult to adopt these TFTs in flexible applications. Although low-temperature poly-silicon (LTPS) TFTs shows high mobility and good stability characteristics, it is also difficult to apply in flexible devices due to a higher crystallization temperature than the glass transition temperature T_g of plastic substrates [3], [4]. Recently, oxide TFTs such as In–Ga–Zn–O (IGZO), Ga–Sn–Zn–O, and Al–Sn–Zn–In–O have received much attention because of their higher mobility and stability characteristics than a-Si:H TFTs, better uniformity characteristics than LTPS TFTs, and lower process temperature than other conventional Si based TFTs [5]–[8]. Particularly, oxide TFTs could be fabricated at low-temperature with high electrical performance [9]. Considering the electrical properties and the process temperature, we believe that oxide TFTs are a suitable backplane for flexible displays.

The second requirement is the glasslike process that limits misalignment problems due to the large coefficient of thermal expansion (CTE) and shrinkage of plastic substrate, and adhesive films for easy lamination and delamination processes. [10]. Generally, polyimide (PI) substrate is widely considered and used as a flexible substrate because of its high glass transition temperature T_g and low CTE. However, PI films show the higher permeability of water molecules than polyethylene naphthalate (PEN) films and lower transmittance in the visible light than other plastic substrate [10]. In spite of low T_g of the PEN substrate (120 °C), it can be used as a flexible substrate with a maximum temperature of 200 °C due to the enhanced dimensional stability by using a heat stabilization process. The delamination of plastic substrate is one of the important processes in the fabrication of the flexible device. Since physical and chemical damages can occur in flexible devices during the detachment process, a damage-free and easy detachment process is necessary. In this paper, we fabricated low-temperature flexible oxide TFTs with high performance and high stability characteristics using PEN substrate and cool-off-type adhesive films.

II. Experimental

We fabricated flexible oxide TFTs with a staggered structure on the PEN substrate. One of the important factors in the fabrication of flexible device is how we can easily attach and detach the flexible substrate to the carrier substrate for the glasslike process. To solve this difficult problem, we adopt the cool-off-type adhesive (Intelimer) that was supported by Nitta Corporation in Japan. Since adhesive properties of intelimer could be switched by controlling the temperature, it can be

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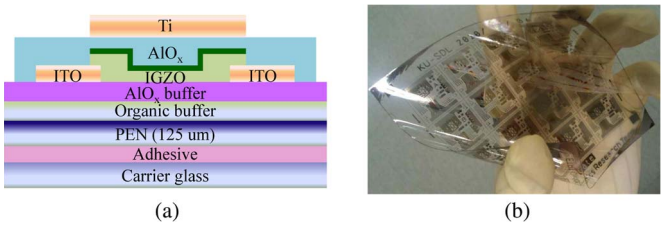

Fig. 1. Device structure and images of flexible oxide TFTs (a) side-view of flexible TFTs with carrier glass and adhesive layer, and (b) bending images of flexible device after detach process.

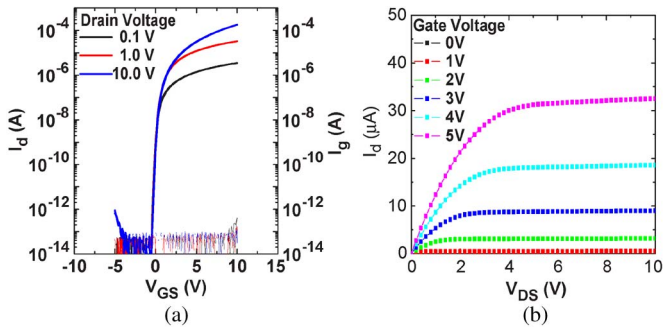

Fig. 2. Electrical characteristics of flexible oxide TFTs (a) transfer curves, and (b) output curves ($W = 40$, $L = 20$ um, maximum process temperature of 150°C)

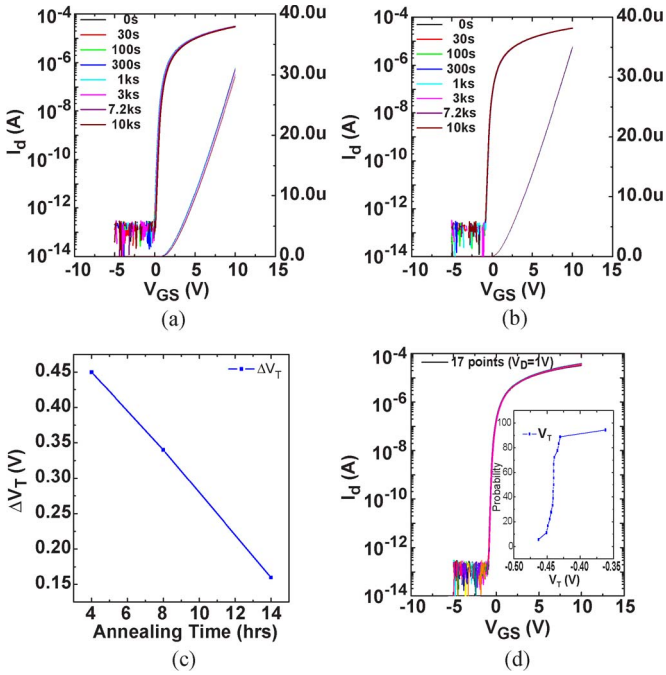

Fig. 3. Stability and uniformity characteristics of flexible oxide TFTs: (a) $V_{GS} = 10$V, (b) $V_{GS} = -10$V measured at room-temperature for 10 ks, (c) variation of V_T under the positive gate bias stress with various anneal time, and (d) uniformity characteristics in 50 × 50 mm ($V_{DS} = 1$V), inset of figure (d) show the variation of V_T

easily peeled off from the carrier substrate at low temperatures (below 10 °C). Fig. 1(a) shows the device structure with carrier glass and adhesive layer. The PEN substrate was laminated using this adhesive film on the carrier glass (100×100 mm^2) for the ease handling of the substrate. The hybrid buffer layers were coated to obtain flat substrate and low water permeability, and to prevent surface scratches. The 150-nm-thick In–Sn–O and 25-nm-thick IGZO active layers (RF power of 200 W) were deposited at room temperature (RT) by RF magnetron sputtering. To preserve the clean interface, a 9-nm-thick protection layer (PL) was grown at 150 °C with the atomic layer deposition (ALD) method by using trimethyl aluminum and water as the Al and oxygen precursors, respectively [11]. Al_2O_3 that is 60 nm thick was also grown by the ALD method as the gate insulator using the same precursors. The 100-nm-thick Ti electrodes were deposited by RF magnetron sputtering as gate electrodes. After the fabrication process, the flexible device was detached from the carrier substrate by decreasing the temperature (below 10 °C). Fig. 1(b) shows the image of a delaminated flexible device. Since it can be easily detached from the carrier glass, we cannot see any cohesive and adhesive failures in the flexible device from the delamination process. Finally, the flexible device was annealed at 150 °C in the vacuum condition (1.0×10^{-2} torr) for 4 h. [9] All patterns were formed by using conventional photolithography and wet etching. All measurements were carried out in the dark box using Agilent B1500A semiconductor parameter analyzer. Positive and negative gate bias stresses were applied for 10 ks in the dark and RT condition to measure the stability characteristics (S/D electrodes are grounded during the gate bias stress).

III. Results and Discussion

Fig. 2(a) and (b) show the transfer and output characteristics of flexible TFTs at the maximum temperature of 150 °C. In spite of the low-temperature process, the device showed high performance and negligible hysteresis behavior (about 0.01 V) in the transfer characteristics. Since the plasma process can induce the charge trap sites at the interface of active/PL that can degrade the electrical performances of TFTs and need high temperature annealing for the curing of the defect state, the superior hysteresis characteristics are strongly related to the PL process, which is a plasma-free process [12]. The flexible device exhibited the saturation mobility of 24.26 cm^2/(V · s), the subthreshold slope (SS) of 140 mV/dec, the threshold voltage V_T of 1.77 V, the turn-on voltage $V_{\rm on}$ of −0.41 V, and the on–off ratio of 1.8×10^9. The high-mobility and low-temperature processes of flexible TFTs with oxide semiconductors have been already reported by several groups. However, these devices have the low on–off ratio due to their high off current state, and the device stability is not yet proven. To study the gate bias stability characteristics of flexible TFTs, we applied positive and negative gate bias stresses ($V_{GS} = 10; V_{GS} = -10$ V), the gate field of which is around 1.6 MV/cm, to the device at RT in the dark condition. The flexible TFTs showed the ΔV_T variation of 0.45 V under the positive gate bias stress. voffset="-3pt" Because the maximum annealing temperature is limited due to the lower T_g and higher CTE than the glass substrate, cumulative annealing was performed at 150 °C in the vacuum oven to enhance the stability characteristics. Fig. 3(a) and (b) shows the results of positive and negative gate bias stress characteristics with an annealing time of 14 h at 150 °C. In spite of low-temperature annealing, devices show highly stable characteristics under the negative gate bias stress regardless of the cumulative annealing time at 150 °C. We cannot see any

change of transfer characteristics, as shown in Fig. 3(b). In the case of oxide TFTs, the stability characteristics are strongly affected by environmental condition due to the oxygen and/or water molecules, which could be enhanced by adopting the dense passivation layer [13], [14]. Because our flexible device was protected from environmental condition by dense Al_2O_3 layers, it can be minimized in this experiment. The highly stable characteristics of flexible IGZO TFTs under the negative gate bias stress could be explained by the wide band gap of semiconductors and Fermi level pinning effects in the deep level state [15]. Meanwhile, the results of positive gate bias stress could be enhanced by increasing the annealing time, as shown in Fig. 3(c). The variation of the ΔV_T value under the same stress was decreased from 0.45 to 0.16 V (annealing time of 4 and 14 h, respectively). There are two possible reasons in this experiment: The first ones are decreased interfacial trap states at the active/insulator interface and electron injection sites in gate insulators, which can shift the V_T values in the positive direction under the positive gate bias stress. Since interface trap state and injection sites in the gate insulator can be cured or minimized by thermal energies, gate bias stability characteristics could be enhanced by the cumulative annealing process. The second is the enhanced bonding state in the IGZO active layer that can reduce the generation of defect state by gate bias stress. In the case of a-Si:H TFTs, acceptor-like state creation occurs by Si–Si bond break under gate bias stress that is highly depend on the temperature and shifts the V_T in the positive direction [16]. Since state creation effects in oxide TFTs (how they can act in the TFTs (donorlike or acceptor-like) and what is directly related to that phenomenon) are still not yet proven, it cannot be considered as a reason of enhanced stability characteristics. We believe that the improved bias stability characteristics under the cumulative annealing process is more closely related to the decrease in interface trap state and injection sites until now, but state creation effects cannot be excluded in the instability phenomena of oxide TFTs. Fig. 3(d) shows the uniformity characteristics of flexible oxide TFTs in the dimension of 50 mm $\times$ 50 mm. Each TFT (17 points) exhibited the variation of 0.1 V in the turn-on voltage $V_{\rm on}$ without any changes in the SS values, which is strongly recommended in the application of flexible devices.

IV. Conclusion

We have fabricated flexible oxide TFTs on the PEN substrate using the IGZO semiconductor and the cool-off-type adhesive film with a maximum process temperature of 150 °C. The flexible oxide TFTs exhibited the saturation mobility of 24.26 $\rm cm^2/(V \cdot s)$, the SS of 140 mV/dec, the threshold voltage V_T of 1.77 V, the turn-on voltage $V_{\rm on}$ of -0.41 V, and the on–off ratio of 1.8×10^9. Flexible devices also showed negligible hysteresis behavior (0.01 V) and good uniformity characteristics (0.09 V). We can obtain highly stable characteristics under the positive and negative gate bias stresses that can be enhanced by the cumulative annealing process at 150 °C. We believe that both reduced trap sites at the gate insulator/active layer and enhanced bonding states in IGZO active layer are reasons for the enhanced stability characteristics.

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